

QUICK GUIDE

# Constraint Manager

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## Introduction

The Constraint Manager in Altium Designer is a powerful tool that simplifies and streamlines the complex task of PCB design. Central to this is a unified table-based editor that consolidates all your design rules and constraints, whether they are electrical or physical in nature. This brings everything into one place, saving you the time and effort of navigating through multiple menus and settings.

One of the significant advances offered by this feature is the unified access to nets, classes, and rules, both from the schematic level and the PCB editor. Now, with this integrated approach, designers can effortlessly input and modify constraints at both the schematic and layout levels, which enhances workflow and ensures design cohesiveness. The Constraint Manager also allows you to redefine rules flexibly, meeting the shifting requirements of your design as it evolves. Added to this is the Class-to-Class Clearance Matrix, an intuitive interface that helps you specify clearances between various component classes, thereby aiding in compliance with industry standards.

Overall, the Constraint Manager is a key enhancement in Altium Designer. It not only makes rule and constraint management simpler but also significantly improves your design workflow by integrating rule management across different stages of the design process.

## Benefits of the Altium Designer Constraint Manager

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#### **Unified Access to Constraints**

With the Constraint Manager, you can access and modify design rules and constraints from both the schematic and PCB editor. This reduces the time spent toggling between different design stages, improving your overall workflow.

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#### **Table-Based Editor**

The feature offers a table-based editor that brings all your design rules and constraints into one place. This centralized location aids in quick rule verification and modification, reducing the chances of design errors.

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#### **Class-to-Class Clearance Matrix**

This tool allows you to specify clearances between different classes of components through an intuitive interface. This helps in meeting compliance requirements with ease, thereby improving the reliability of the final product.

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#### **Redefinable Constraints**

The ability to easily redefine rules gives you the flexibility to adjust to the changing requirements of your design project. This ensures that your design stays aligned with both technical and business goals, without having to rework your constraints from scratch.

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#### **Physical and Electrical Constraints**

The Constraint Manager allows you to set both electrical and physical constraints within the same framework. This enables a more holistic approach to design, ensuring that all aspects, from signal integrity to mechanical fit, are accounted for.

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#### Improved Productivity

The feature's unified and table-based approach allows for easier and quicker constraint management. This leads to improved productivity as designers spend less time managing constraints and more time on actual design work.

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#### Streamlined Workflow

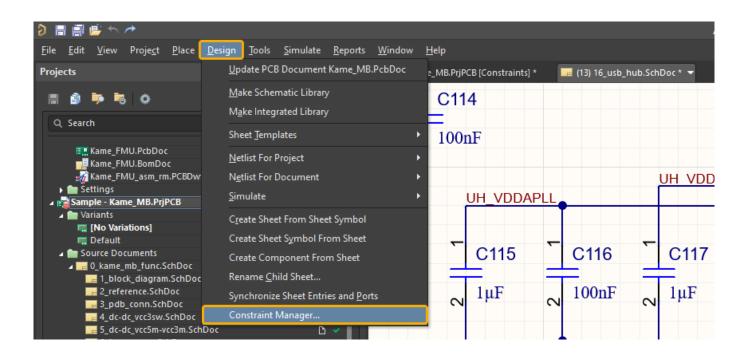
The feature's ability to manage constraints from both schematic and PCB design stages in one place streamlines the design process. This results in a faster time-to-market for the product.

## **Constraint Manager Use Case**

Constraint Manager simplifies the PCB design process by letting you manage all your design rules in one place. It connects the schematic and PCB layout, making sure that what you plan is what you get. This makes it easier to communicate design intent and ensures that your board is made right the first time.

Here is one example that illustrates the capabilities of Constraint Manager in a real-world application:

1. Starting in the schematic editor, go to Design and open Constraint Manager



- 2. After opening the **Constraint Manager document**, we can easily manage rules for all nets in the project. The interface, accessible from the schematic editor, is divided into three tabs:
  - 2.1. Clearances for defining minimum distances between Net Classes,

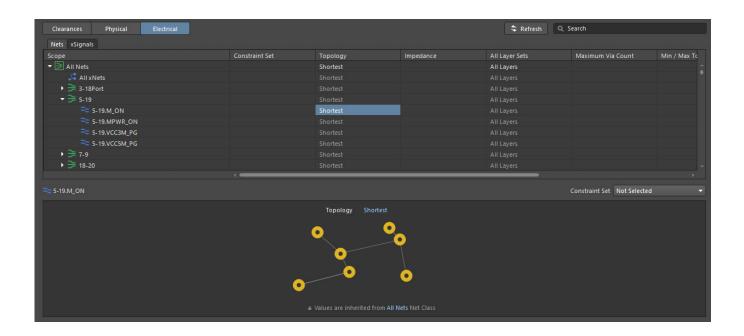
Clearances	Physical	Electrical	Ĩ			S Refresh	Q Search	
+ Add	All Net (	Classes	All Nets	🗦 RPI_GPIO				
All Net Classes				-				
🗦 All Nets								
🗦 RPI_GPIO								
🗦 RPI_GPIO / 📄 AII	Net Classes	Constra	aint Set Not Selected	<ul> <li>Values by Layers</li> </ul>				
					Track	SMD Pad	TH Pad	
				Track				
				SMD Pad				
			Clearance	TH Pad				
			0-0.15mm	Via				
. 2				Copper				
				Hole				

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2.2. Physical for setting physical constraints such as Track Width, Differential Pairs details, Clearance, Via Style, and Polygon Connects,

cope	Constraint Set	Min Width	Preferred Width	Preferred Dif	f Pair Gap	Clearand		Via	Style	
All Nets		0.1mm	0.125mm	0.254mm		0.12mm			- 7mm, 0.7112	mm
🝷 😂 All Differential Pairs								1.2	7mm, 0.7112	mm
🕨 😂 CAN		0.1mm	0.1mm	0.4mm						
🕨 📚 csi		0.1mm	0.1mm	0.13mm						
► @ BMC_USB_D								1.2	7mm, 0.7112	mm
► 🗢 @EXP1_USB_D								1.2	7mm, 0.7112	mm
🕨 🗢 @USBA1_D								1.2	7mm, 0.7112	mm
▶ 🗢 @USBA2_D								1.2	7mm, 0.7112	mm
		n 1	0.105							
	Width	Gap		0.1mm	0.254mm	0.1mm	0.4mm	0.7mm	0.7mm	📕 [1] T
	14P 10			Min Widt	Min Gap	Preferred	Preferred	Max Widt	Max Gap	Layer
									0.7mm	[2] 8
	Min 0.1mm	Min 0.254mm		0.1mm	0.254mm	0.1mm	0.4mm	0.7mm	0.711111	[4]
	Min 0.1mm Pref 0.1mm	Min 0.254mm Pref 0.4mm		0.1mm	0.254mm	0.1mm	0.4mm	0.7mm	0.711111	
				0.1mm	0.254mm	0.1mm	0.4mm	0.7mm	0.711111	[2]
	Pref 0.1mm	Pref 0.4mm	Δ	0.1mm	0.254mm	0.1mm	0.4mm	0.7mm	0.71111	[2] (
	Pref 0.1mm Max 0.7mm 	Pref 0.4mm	م_	0.1mm	0.254mm	0.1mm	0.4mm	0.7mm	0.71111	
Max Uncoupled Lengt	Pref 0.1mm Max 0.7mm 	Pref 0.4mm		0.1mm	0.254mm	0.1mm	0.4mm	0.7mm	0.711111	(L) (
Max Uncoupled Lengt 12.7mm ——	Pref 0.1mm Max 0.7mm 	Pref 0.4mm		0.1mm	0.254mm	0.1mm	0.4mm	0.7mm	0.711111	(L) (
	Pref 0.1mm Max 0.7mm 	Pref 0.4mm		0.1mm	0.254mm	0.1mm	0.4mm	0.7mm	0.71111	
	Pref 0.1mm Max 0.7mm 	Pref 0.4mm		0.1mm	0.254mm	0.1mm	0.4mm	0.7mm	0.71111	

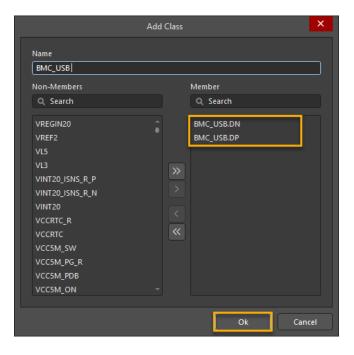
2.3. Electrical for specifying electrical constraints like Topology, Impedance, Maximum Via Count, Min/Max Total Length, Max Stub Length, and Max Via Stub Length.



- 3. All **Nets** can be easily grouped into classes, differential pairs or xNets. To do this, you should select the nets you want to add to group , and then **right-click** then choose the desired type:
  - 3.1. Classes

BMC_USB.DN				0.1mm	0.12
BMC_USB.DP		Remove rules from scope		0.1mm	0.12
→ -E1_USB_LED_A_R		Remove rule		0.1mm	0.12
→ -E1_USB_LED_B_R		Copy/Paste Values	•	0.1mm	0.12
→ -E2_USB_LED_A_R				0.1mm	0.12
→ -E2_USB_LED_B_R		Save as Constraint Set		0.1mm	0.12
→ -E3_USB_LED_A_R		Select Constraint Set	•	0.1mm	0.12
← -E3_USB_LED_B_R		Classes	•	Add Selected to Class	
-E3_USB_LED_B_R -E4_USB_LED_A_R					
		Classes Differential Pairs	•	Add Selected to Class Add Class	•
≈ -E4_USB_LED_A_R					•
-E4_USB_LED_A_R -E4_USB_LED_B_R		Differential Pairs xNets	•	Add Class	•
<ul> <li>-E4_USB_LED_A_R</li> <li>-E4_USB_LED_B_R</li> <li>FMU_SYS_USB_DN</li> </ul>	ġ	Differential Pairs	•	Add Class Class Explorer	•

Then, in the appearing window, you can name the new class, add '>>' or remove '<<' signals to a member of the class. After setting all options, click '**OK**'.



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The newly created **Class** will immediately appear in the tabs.

Clearances	Physical	Electrical	]
Scope			Constrair
7-9 关 🔸			
18-20 岸			
🕨 🏓 вмс_	2C2		
🔹 🏓 ВМС_	USB		
🔫 в	MC_USB.DN		
🚬 🔁 в	MC_USB.DP		
► ≓ CAM1			
🕨 🏓 сама			
🕨 🕨 🗦 ESC_N	1[16]		
🕨 🏓 EXP1			
▶ 🗦 EXP1_			

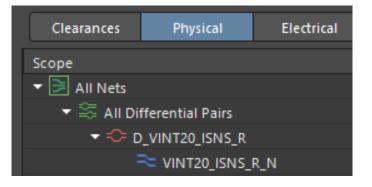
#### 3.2. Differential Pairs

Clearances Physical Electrical				
Scope	Constraint Set	Min Widt	h Pref	erred Width
→ -E3_USB_LED_B_R		0.1mm	0.12	5mm
→ -E4_USB_LED_A_R		0.1mm	0.12	5mm
→ -E4_USB_LED_B_R		0.1mm	0.12	5mm
THU_SYS_USB_DN		0.1mm	0.12	5mm
THU_SYS_USB_DP		0.1mm	0.12	5mm
FMU_USB.DN		0.1mm	0.12	5mm
FMU_USB.DP	Remove rules from sco	pe	0.12	5mm
← FMU_USB_VBUS			0.12	5mm
PMUX_USBC_PWR_SHDN			0.12	5mm
➤ STUSB.ALERT#	Copy/Paste Values	•	0.12	5mm
🔁 STUSB.ATTACH#	Save as Constraint Set	:	0.12	5mm
🔁 STUSB.FAULT#	Select Constraint Set	•	0.12	5mm
← STUSB.RST	<i>C</i> 1	•	0.12	5mm
STUSB_ALERT#_R	Classes		0.12	5mm
➡ STUSB_ATTACH#_R	Differential Pairs	•	Create Differential F	Pairs From Nets
STUSB_FAULT#_R	xNets	•	Remove Differential	Pair
← STUSB_SCL			0.12	5mm
← stusb_sda	View Options	•	0.12	5mm
≈ sys_usb.dn	🕻 CrossProbe		0.12	5mm

either change or leave the **differentiating suffixes** (\_P and N) and the **prefix** (D\_) that will be used to create the differential Pair Name. After making your selections, click 'Execute'.

Create Differential Pairs From Nets						
Use nets from class All Nets	✓ differing by _P or _	N to create differential pair	r with prefix D			
Create differential pairs in class	All Differential Pairs 🔹					
Differential Pair Name	Positive Net	Negative Net	Create			
D_VINT20_ISNS_R	VINT20_ISNS_R_P	VINT20_ISNS_R_N	Image: A start and a start			

The newly created **Differential Pair** will immediately appear in the tabs.



#### 3.3. xNets

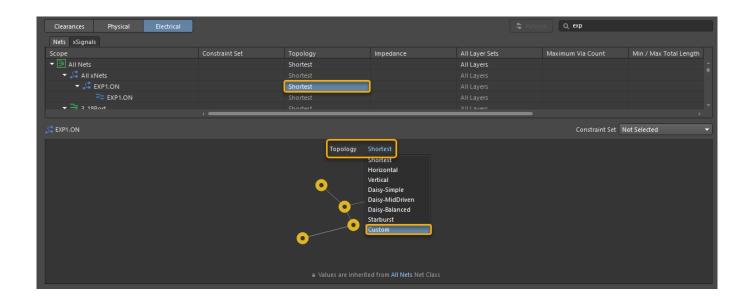
Clearances Physical	Electrical			
Nets xSignals				
Scope	Constraint Set		Topology	Impedance
≃ EXP1_IMON3			Shortest	
≃ EXP1_IMON5			Shortest	
≈ EXP1_PG_R			Shortest	
≈ EXP1_SS3			Shortest	
≈ EXP1_SS5			Shortest	
VCC3_EXP1_PG			Shortest	
EXP1.ON			Shortest	
🔁 EXP1.PG			Shortest	
🔁 EXP2.ON			Shortest	
🔁 EXP2.PG	Copy/Paste Values		Shortest	
← EXP2A			Shortest	
≈ ехр2в	Save as Constraint Set		Shortest	
← EXP2DN	Select Constraint Set	•	Shortest	
➡ EXP2DP	Classes	•	Shortest	

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The newly created **xNet** will immediately appear in the tabs.

Clearances	Physical	Electrical	
Nets xSignal	s		
Scope			Con
🔻 📄 All Nets			
🔻 🔎 👻 👻	Nets		
- S	EXP1.ON		
	≃ EXP1.ON		
_			

4. In the added **xNets**, you can set individual **xSignal** rules. To do it go to the '**Topology**' column. In the bottom panel, then near the topology menu, select '**Custom**' from the dropdown list



Then, in the topology window, add all the nodes by right-click at empty window then Add node then add all nodes.

💭 EXP1.ON				Constraint Set Not Selected 👻
		Topology Custom		
			xSignals	
_				
<b>_</b>	Add node  V18-1 U29-1			

Next, check the checkbox for the xSignal you want to define.

💭 EXP1.ON			Constraint Set Not Selected 🔹
	Topology Custom		
		- xSignals	
<b>S</b> U18-1	 		

Now, in the xSignal sub-tab, the previously selected pairs will appear.

Clearances	Physical	i	Electrical	
Nets xSignal	s			
Scope			Tolerance	
🔹 🏓 All xSign	als			
🔍 EXP	EXP1.ON_U18-1_U29-1			
≃ EXP	1.ON_U29-1_U31-	-1		

To define length Tolerances and Marching Target, each xSignal should be added to the class.

Clearances Physical Elec	trical	
Nets xSignals		
Scope	Tolerance	Matching Target
▼ ⇒ xs_exp1_a	0.1mm	EXP1.ON_U18-1_U29-1
≃ EXP1.ON_U18-1_U29-1	-	-
▼ ⇒ xS_EXP1_B	0.1mm	EXP1.ON_U29-1_U31-1
➡ EXP1.ON_U29-1_U31-1	-	

5. The new feature is the ease of defining a **Constraint Set**, which is a defined set of parameters that we can later conveniently assign to nets or classes. To define such a Set, **right-click** on the row of rules you desire, then choose the option **Save as Constraint Set**.

Scope	Constraint Set	Min Width	Preferred Width	Preferred Diff Pair Gap	Clearance	Via Style	Polygon Connect
🔁 _FMU.EN						1.27mm, 0.7112mm	Relief connect, 0.254mm, 0.254mm, 4, 90
🚬 _FMU.PG						1.27mm, 0.7112mm	Relief connect, 0.254mm, 0.254mm, 4, 90
≈ 1R8_AGND						1.27mm, 0.7112mm	Relief connect, 0.254mm, 0.254mm, 4, 90
≈ 1R8_MODE						1.27mm, 0.7112mm	Relief connect, 0.254mm, 0.254mm, 4, 90
1R8_ON		0.1mm	0.15mm		0-0.254mm	1mm, 0.5mm	TH Pad: Relief connect, 0.254mm, 0.254mm, 4, 90; SMD
🔁 ЗМ_СОМР	Remove rules from scope					1.27mm, 0.7112mm	Relief connect, 0.254mm, 0.254mm, 4, 90
Regional Skipsel						1.27mm, 0.7112mm	Relief connect, 0.254mm, 0.254mm, 4, 90
≈ 5M_COMP	Copy/Paste Values					1.27mm, 0.7112mm	Relief connect, 0.254mm, 0.254mm, 4, 90
SM_SKIPSEL						1.27mm, 0.7112mm	Relief connect, 0.254mm, 0.254mm, 4, 90
🔁 BAT_PWR17	Save as Constraint Set					1.27mm, 0.7112mm	Relief connect, 0.254mm, 0.254mm, 4, 90
RAT_PWR17_CN	Select Constraint Set					1.27mm, 0.7112mm	Relief connect, 0.254mm, 0.254mm, 4, 90
RAT_SCL	Classes >					1.27mm, 0.7112mm	Relief connect, 0.254mm, 0.254mm, 4, 90
🔁 BAT_SDA	Differential Pairs					1.27mm, 0.7112mm	Relief connect, 0.254mm, 0.254mm, 4, 90
BMC.GPIO_INT1#	Differential Pairs	0.1mm	0.125mm			1.27mm, 0.7112mm	Relief connect, 0.254mm, 0.254mm, 4, 90



New Constraint Set 🔞		
Main		
	Create	Cancel

7. Now, we can assign our constraint set to any class or net by clicking on the cell in the **Constraint Set** column and selecting our set from the **dropdown list**.

Scope	Constraint Set
≃ _FMU.EN	
imu.pg	
≈ 1R8_AGND	Not Selected 🔹
≈ 1R8_MODE	Not Selected
≈ 1R8_ON	Main
≈ зм_сомр	
≈ 3M_SKIPSEL	
≈ 5м_сомр	
≈ 5M_SKIPSEL	
RAT PWR17	

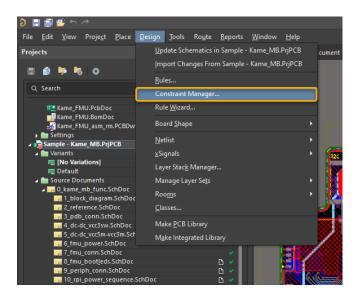
or select more than one and right-click>Select Constraint Set>'Constraint Set Name'

Clearances Physical Elec	trical					
Scope	Constraint Set	Min Width	Preferred Width	Preferred Diff Pair Gap	Clearance	Via Style
🔁 _FMU.EN						1.27mm, 0.7112m
← _FMU.PG						1.27mm, 0.7112m
TR8_AGND		0.1mm	0.15mm		0-0.254mm	1mm, 0.5mm
← 1R8_MODE		0.1mm	0.15mm		0-0.254mm	1mm, 0.5mm
← 1R8_ON	Main	「0.1mm	「0.15mm		「0-0.254mm	៍1mm, 0.5mm
≈ зм_сомр						1.27mm, 0.7112m
≈ 3M_SKIPSEL						1.27mm, 0.7112m
≈ 5м_сомр		0 1mm				1.27mm, 0.7112m
← 5M_SKIPSEL	Remove r	ules from scope				1.27mm, 0.7112m
The BAT_PWR17	Remove rul					1.27mm, 0.7112m
RAT_PWR17_CN	Copy/Pas	ha Maluara 🛛 🖒				1.27mm, 0.7112m
The BAT_SCL	COpy/Pas					1.27mm, 0.7112m
➡ BAT_SDA	Save as C	onstraint Set				1.27mm, 0.7112m
RMC.GPIO_INT1#	Select Co	nstraint Set 🔹 🕨	✓ Not Selected			1.27mm, 0.7112m
RMC.GPIO_INT2#	Classes	,	Main			1.27mm, 0.7112m
RMC.I2C1_SCL	The BMC.12C1_SCL		0.125mm			1.27mm, 0.7112m
≈ BMC.I2C1_SDA	RMC.12C1_SDA Differential F					1.27mm, 0.7112m
≈ BPWR_ON	Reference Service Serv					1.27mm, 0.7112m
RUZZ_DRV	The BUZZ_DRV View Optio					1.27mm, 0.7112m
≈ BUZZ_H						1.27mm, 0.7112m
≈ BUZZ_L	🙋 CrossProl	be				1.27mm, 0.7112m
← -E1_USB_LED_A_R		0.1mm	0.125mm			1.27mm, 0.7112m

6. In the appearing window, you should enter the desired name of the constraint set.

ا ج الح 🗐 🗐 🕄 🖇		
<u>F</u> ile <u>E</u> dit <u>V</u> iew Proje <u>c</u> t <u>P</u> lace	<u>Design T</u> ools <u>S</u> imulate <u>R</u> eports <u>W</u> indov	w <u>H</u> elp
Projects	Update PCB Document Kame_MB.PcbDoc	b_hub.SchDoc 👻 🋄 Kame_MB.PcbD
III 🕼 Þ 🍋 🔿	Make Schematic Library	C114
Q Search	M <u>a</u> ke Integrated Library	
	Sheet <u>T</u> emplates	100nF
Kame_FMU.PcbDoc	Netlist For Project	•
Kame_FMU_asm_rm.PCBDv	w N <u>e</u> tlist For Document	•
Settings	Simulate	UH VDDAPLL
Sample - Kame_MB.PrjPCB		
Variants	Create Sheet From Sheet Symbol	
In the second se	Create Sheet Symbol From Sheet	
✓ Image: A second s	Create Component From Sheet	C115 C
Image: Ame_mb_func.SchDoc		
1_block_diagram.SchDo	oc Rename <u>C</u> hild Sheet	
2_reference.SchDoc	Synchronize Sheet Entries and Ports	$\sim$ <sup>1µF</sup> $\sim$ <sup>10</sup>
4 dc-dc vcc3sw.SchDoc	Constraint Manager	
5 dc-dc vcc5m-vcc3m.Sc		
6_fmu_power.SchDoc		•
7_fmu_conn.SchDoc	✓	
🔚 8_fmu_bootleds.SchDoo	c 🗅 🗸	
9_periph_conn.SchDoc		

 In the PCB editor, similarly to the Schematic, you can access the Constraint Manager by selecting Design > Constraint Manager.  After finishing the editing in the Constraint Manager, you need to transmit all the information to the PCB by selecting the command **Design > Update PCB Document**.



10. The Constraint Manager, accessible from the PCB level, is also divided into tabs. However, in addition to the Clearances, Physical and Electrical tabs available in the schematic, in the PCB there is also an All Rules tab, which is a compilation of all rules and is inspired by the old version of the Rules Manager.

Clearances Physical Electrical	All Rules				
Nets xSignals					
Scope	Constraint Set	Topology	Impedance	All Layer Sets	Maximum
▼ All Nets		Shortest		All Layers	
- → _FMU				All Layers	
≂ _FMU.EN				All Layers	
≈ _FMU.PG				All Layers	
▼ 🗦 3-18Port				All Layers	
Report.BMC_GPIO_B3				All Layers	
Report.BMC_GPIO_B5				All Layers	
3-18Port.BMC_I2C3_SCL				All Layers	
Report.BMC_I2C3_SDA				All Layers	
3-18Port.BMC_I2C4_SCL				All Layers	
3-18Port.BMC_I2C4_SDA				All Layers	
Report.ESC_EN				All Layers	
Report.ESC_PG				All Layers	
→  →  5-19				All Layers	
≈ 5-19.M_ON				All Layers	
≈ 5-19.MPWR_ON				All Layers	
≈ 5-19.VCC3M_PG				All Layers	
≈ 5-19.VCC5M_PG					
- 7-9				All Layers	
₹ 7-9.FMU_BUZZ				All Layers	

#### All rules:

Clearances Physical Electrical	All Rules				Q, Search
Rule Class	Priority	Name	Object Match	Second Object Match	
Electrical	🚊 🔻 Advan	ced Rules			
Clearance (16)	1	Outline/NPTH clearance	(IsThruPin and (PadisPlated = 'False')) or IsBoardCutoutRegion or IsBoardOutline		0.25mm
Short-Circuit (1)	2	L5 clearance	OnLayer('L5')		0.15-0.2mm
Un-Routed Net (1)	3	Polygon clearance 18um	InPolygon and (OnLayer('Top') or OnLayer('Bottom') or OnLayer('L3') or OnLayer('L6'))		0.15-0.2mm
	4	Polygon clearance 35um	InPolygon and OnLayer('L5')		0.2mm
Modified Polygon (1)	5	CSI via clearance	InDifferentialPairClass("CSI") and IsVia	InDifferentialPairClass('CSI') and IsVia	0.15mm
	6	USB via clearance	InDifferentialPairClass('USB') and IsVia	InDifferentialPairClass('USB') and IsVia	0.1mm
<ul> <li>High Speed</li> </ul>	7	CAN via clearance	InDifferentialPairClass('CAN') and IsVia	InDifferentialPairClass('CAN') and IsVia	0.7mm
	8	CSI clearance	InDifferentialPairClass('CSI')		0.6mm
	9	USB clearance	In Differential Pair Class ('USB')		0.5mm
Matched Lengths (2)	10	CAN clearance	InDifferentialPairClass('CAN')		0.7mm
		Top clearance	OnLayer('Top')	OnLayer('Top')	0.1mm
		GND1 clearance	OnLayer('GND1')		0.2mm
		Power clearance	OnLayer('Power')		0.15mm
		GND2 clearance	OnLayer('GND2')		0.2mm
		Bottom clearance	OnLayer('Bottom')	OnLayer('Bottom')	0.1mm
<ul> <li>Routing</li> </ul>	Basic F	Rules			
Width (2)		Clearances Matrix 🗹	Matrix	Matrix	0-0.7mm
Routing Topology (2)					
Routing Priority (1)					
Routing Layers (2)					
Routing Corners (1)					
Routing Via Style (552)					
Fanout Control (5)					
Differential Pairs Routing (7)					
▲ Plane					
Power Plane Connect Style (3)					
Power Plane Clearance (2)					

## Conclusions

**Centralized Rule Management:** Constraint Manager serves as a one-stop hub for rule definition and management, streamlining the design workflow for increased productivity. This centralized approach eliminates the need to jump between multiple tools or panels, making it easier to maintain a consistent set of rules across the design.

**User-Friendly Tabs:** With user-friendly tabs like Clearances, Physical, and Electrical, Constraint Manager makes it easy to focus on specific design aspects. This targeted approach allows designers to more efficiently optimize various elements, such as spacing between traces or electrical properties, without getting overwhelmed by the full complexity of the project.

**Intuitive Navigation:** Intuitive navigation within Constraint Manager promotes quicker learning curves for new designers and greater efficiency for seasoned professionals. Its layout is designed to be easily understood, minimizing the time needed to get acquainted with its functions and capabilities. **Comprehensive 'All Rules' Tab:** The All Rules tab offers a comprehensive view of all constraints, making it easier for engineers to identify conflicts or inconsistencies. With all the rules listed in one place, designers can quickly assess the status of their design rules, which saves time and reduces the risk of errors.

**Continuous Improvement:** Ongoing improvements and feature rollouts for Constraint Manager demonstrate its value as an indispensable tool in electronics design. Its continual evolution ensures that it stays aligned with industry needs, making it a reliable tool for both current projects and future advancements in electronics.