Altium

High Speed Design and XSignals

Michael Doyon
Sr. Field Application Engineer

HIGH SPEED DESIGN AND XSIGNALS

High Speed design is one of the most challenging tasks that an electrical engineer can take on. There are any number of factors that can affect the way a high speed signal will respond. A common misconception is that High Speed Design is a function of the System Clock Frequency. This is not the case. Rather, high speed is determined by Rise Time, Impedance Control with PCB Stack-up, Trace Width, and Terminations.

Faster switching speeds essentially mean two things for engineers and PCB designers:

Signal Integrity Issues

- Reflections, crosstalk, etc.
- Signal Integrity goals are met through controlled impedance routing, terminations, and PCB stack-up.

Timing Constraint

- Ensuring that multiple signals reach their destination pins at approximately the same time
- Matching route lengths of signal paths

Timing integrity is important in many applications including DDRx and SDRAM designs, which have become some of the most common. Currently these types of designs contain one or more of the following; DDR, DDR2, DDR3, or DDR4. DDR designs come with a long list of timing rules, including:

- Address/Command lines matched to +/- 20mils of clocks
- Address/Command lines matched to +/- 10mils of each other
- Data strobe pairs routed as diff pairs
- Data strobe pairs matched to +/- 1mil of each other
- Data nets matched to +/- 10mils
- And many more, all while maintaining impedance, clearance, etc.

When routing for high speed it's also extremely important to apply a Routing Topology. The topology of a net is the arrangement or pattern of the pin-to-pin connections. By default, pin-to-pin connections of each net are arranged to give the shortest overall connection length. A topology can be applied to a net for a variety of reasons. For high speed designs where signal reflections must be minimized, the net is arranged with a daisy chain topology. However, for ground nets, a star topology could be applied, to ensure that all tracks come back to a common point.

DDR2 (and some situations in DDR3) can employ "balanced-T" or "branch matched" topology. While DDR3 and DDR4 introduced "fly-by" topology. In "fly-by" topology, Address/Control/Clock signals are routed sequentially from one SDRAM to the next, which eliminates reflections. This routing topology is much simpler. The memory controller compensates for the inherent delay (read/write leveling). However, address/control lines still need to be matched chip-to-chip.

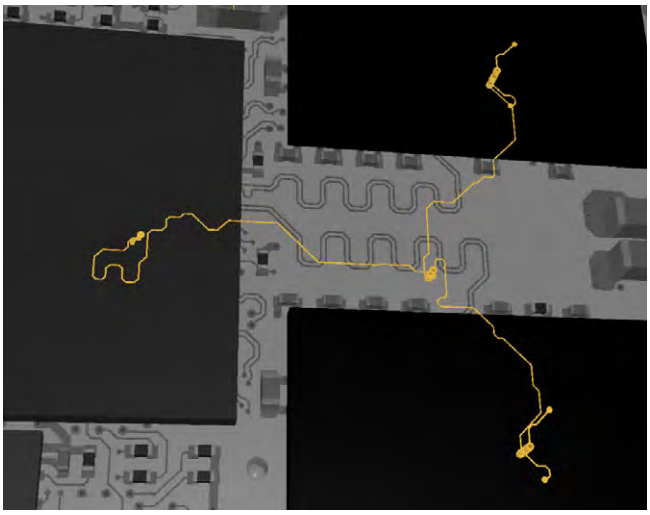

Figure 1: ADDR15 xSignal consists one source pin (left) connected to two destinations pins forming two unique paths

The data lines pose a different problem. All data lines must be tuned in parallel to a target length plus or minus a tolerance. They must also pass through termination resistors, and often multiple vias between the starting pad and the final destination pads. The multiple segments and termination resistors make it very difficult to tune the overall net length of all the data lines. In addition, in designs of very high speeds you also need to account for the individual pin delays that are built into the components from pad to substrate. So as you can see, there are many factors for the engineer or PCB designer to consider when doing high speed routing. It's nothing if not a challenge.

The Old Way

In the past, engineers were forced to deal with length tuning by keeping track of everything in spreadsheets. This allowed them to keep track of each individual segment length for a net, via depths, resistor lengths, and pin lengths. After adding them all up for each net, then adding signal length wherever needed, this enabled them to equalize the lengths of all the nets in the group. This is an antiquated method of length matching, which is both cumbersome and time-consuming.

INTRODUCING XSIGNALS AND THE XSIGNAL WIZARD

XSignals

What is a XSignal? A XSignal is essentially a designer-defined signal path between 2 nodes. These can be two nodes within the same net, or they can be two nodes in associated nets, separated by a component. Once the nodes are established, the XSignal can then be used to scope relevant design rules such as Length and Matched Length. These rules will then be obeyed during interactive length tuning and other design tasks.

- XSignals are used to control timing by matching routed lengths
- XSignals combine nets into a logical path
- XSignals ignore intermediate passives
- XSignals break continuous nets into physical subnets
- XSignals support both Balanced-T and Fly-by topologies
- The XSignal Wizard can be used to create and assign XSignals to XSignal Classes automatically
- Design rules ensure length matching during the interactive tuning process.
- Differential pair length tuning is supported for XSignals
- XSignals support length tuning across terminators, such as serial resistors in the track with e.g. 34 ohm tracks.

XSignal Wizard

The Technology-Aware XSignals Wizard helps to automate the creation of XSignals. One of the first technology families supported by the wizard was DDR3 or DDR4 memories.

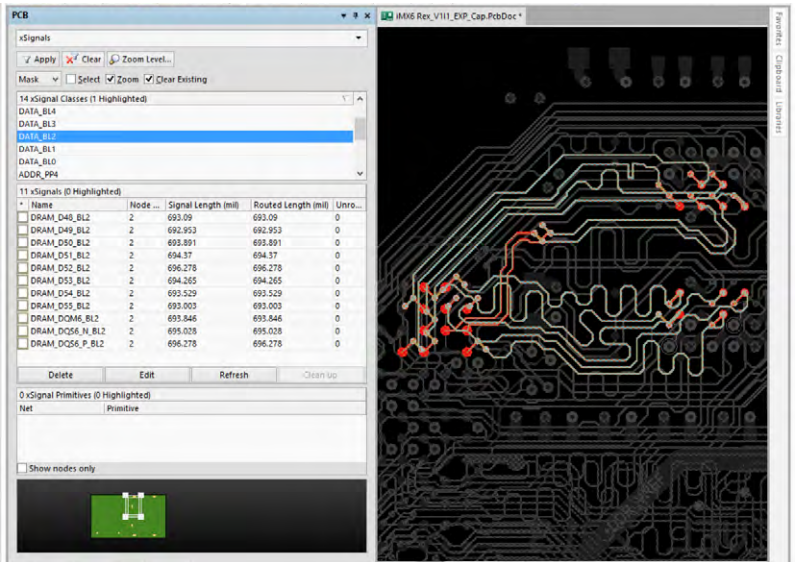

Figure 2: Automatically generated xSignal Class of all Byte Lane 2 specific Data xSignals

In these modes, the wizard will automatically create the XSignals, XSignal Classes, Matched Length Groups, Diff Pair Matched Lengths Rules, and Fly-By topology for on-board DDR3/4.

The Wizard assumes that a fly-by routing topology will be used. The wizard also includes settings for the width of the data bus, in each byte-lane. It also includes settings for the tolerance of the Matched Net Length rules, which will be created for the:

- Address/Command/Control nets
- Data Byte-Lanes
- Clocks

Managing Pin-Package Delays in Altium Designer

In every high speed design over 500 MHz, the connection medium, or bond wire to the die, introduces a delay to the signal. This in-device delay is referred to as the pin-package delay.

These delays need to be accounted for. Pin package lengths can be defined as an attribute of the schematic component pin. The length value is transferred to PCB layout, where it becomes the Pin/Pkg Length of the footprint pad. The Pin/Pkg Length is automatically included in Signal length calculations as part of the XSignal definition.

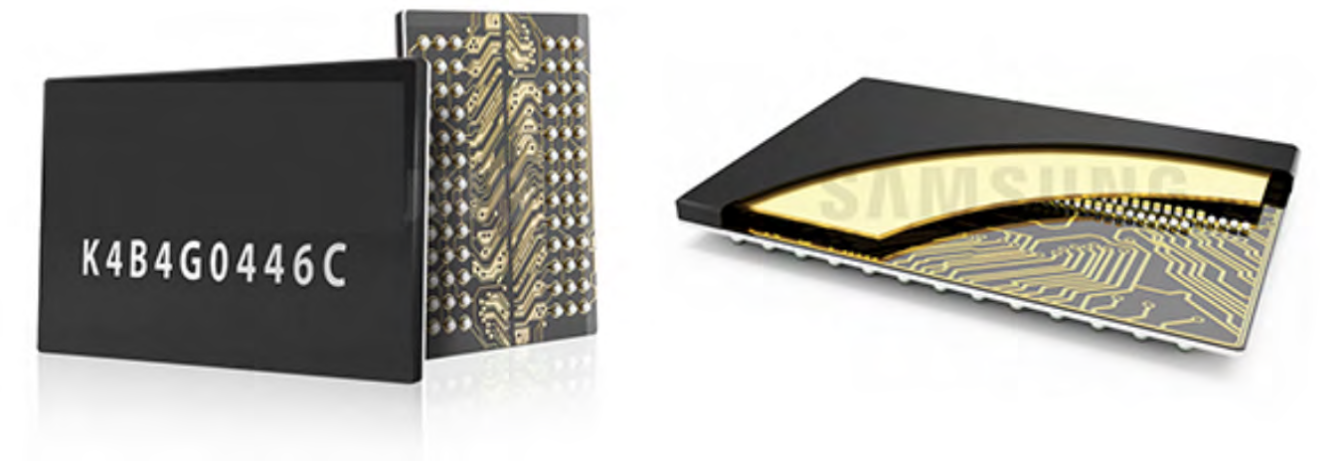

Figure 3: Pin/Package distances can be specified as an attributes of the component's schematic symbol (reference image: Samsung)

More information on Xsignals in Altium Designer