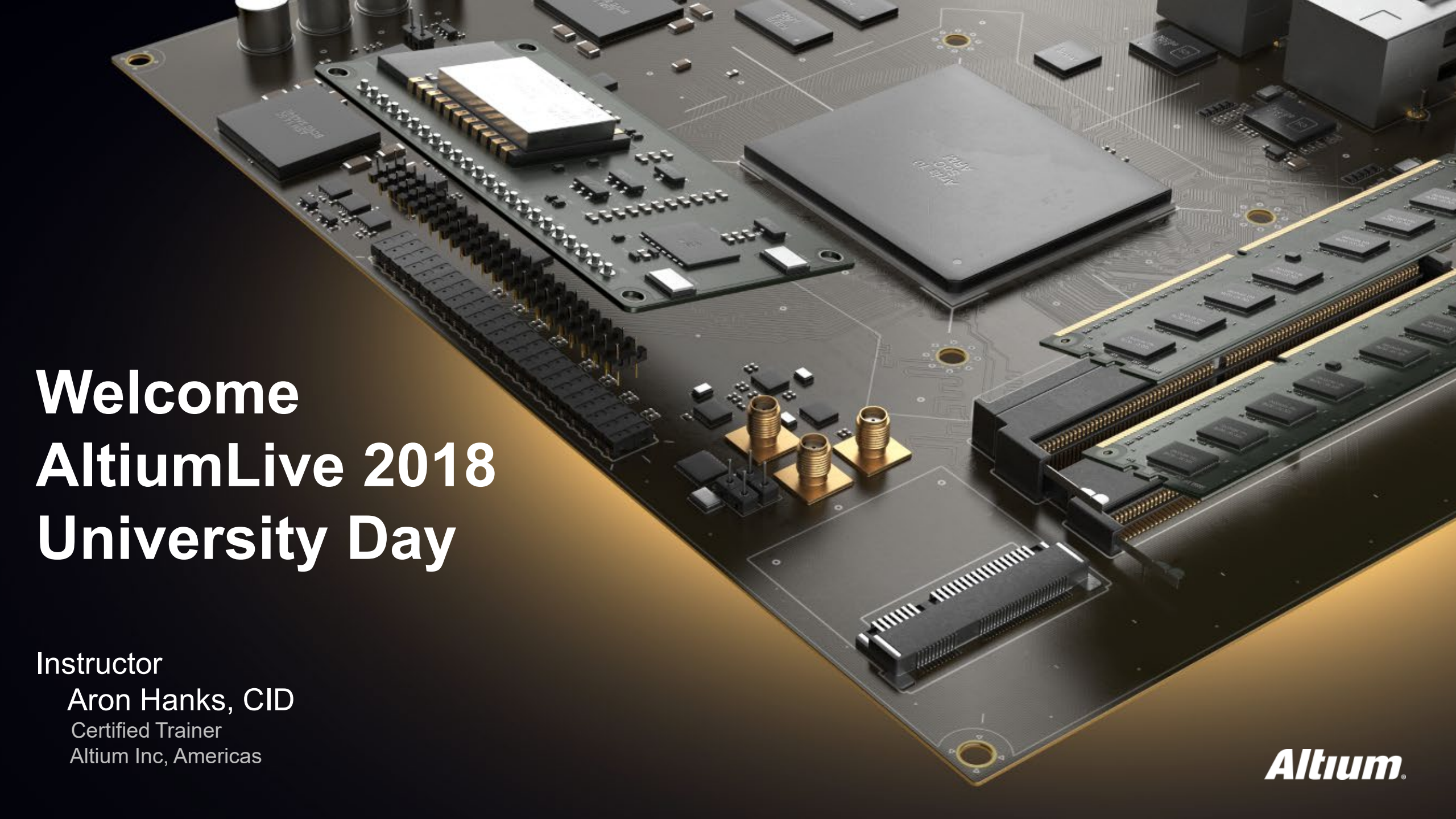


# Welcome
# AltiumLive 2018
# University Day

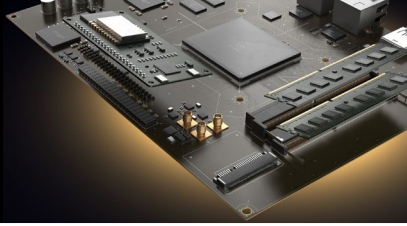

Instructor

Aron Hanks, CID

Certified Trainer

Altium Inc, Americas


Altium



# Agenda

**General BGA and PCB Layout Overview**

- Pitch Size
- BGA Landing Pads

**Layer Count Estimation / Optimization**

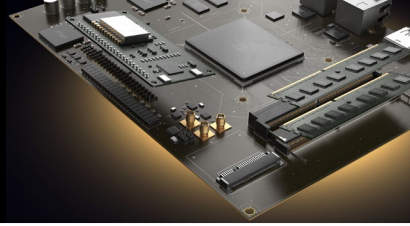
- Layer Count Est / Opt
- Maximum Board Thickness

**Recommended Layout Dimensions within BGA for 1.0mm Pitch**

- BGA Ball and Via Dimensions
- Trace Widths Dimensions inside the BGA Area
- Trace Routing Between Vias

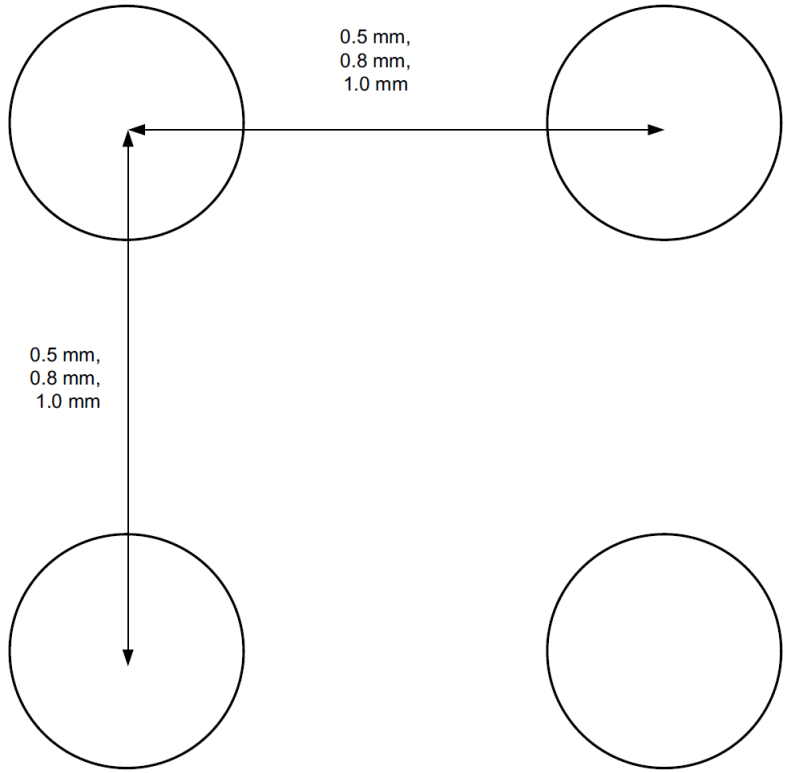
**Altium Tools and Fanout Automation**

- Design Rules (Rooms, Clearance, Width, Via size, Fanout) for Fanout automation
- Signal Identification for Blind Via Routing Layer assignment.
- Selection methods for fine tuning
- Demonstration



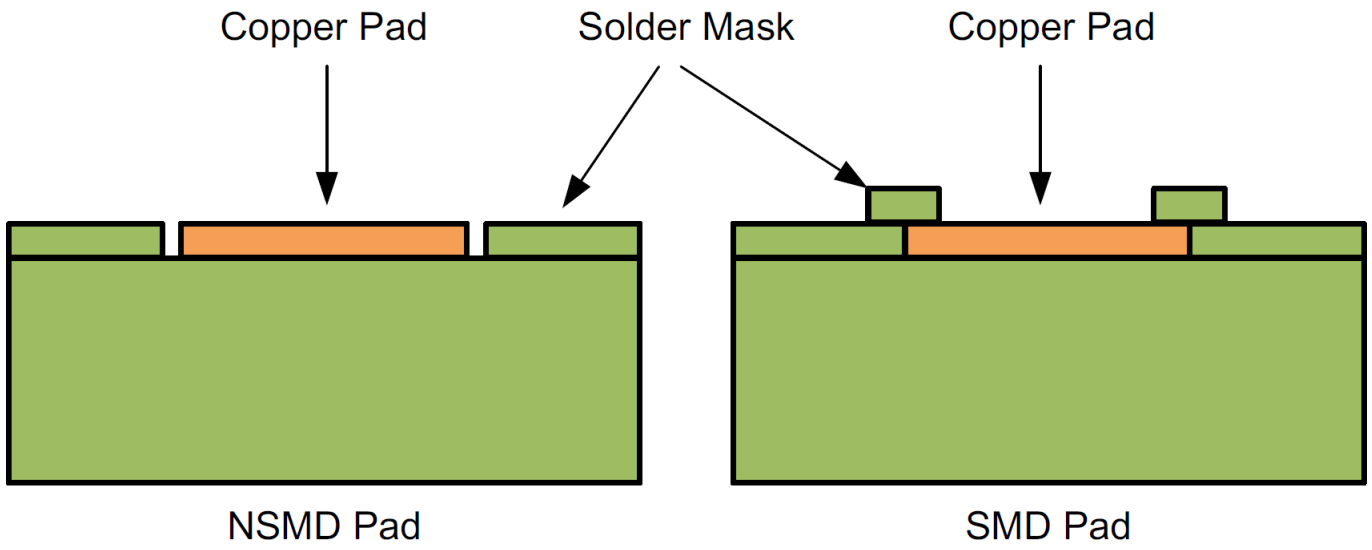
# Pitch Size

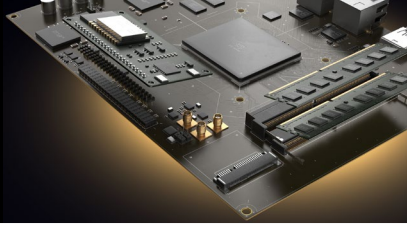
Pitch size is defined as the distance between the consecutive balls on a BGA package measured from center to center.



# BGA Landing Pads

Recommendations have been the use of Non Solder Mask Defined (**NSMD**) copper BGA landing pads for optimum board design. **NSMD** pads are pads that are not covered by any solder mask, as opposed to Solder Mask Defined (SMD) pads in which a small amount of solder mask covers the pad landing.





# Layer Count Estimation

A quick way to estimate the number of routing layers required to fully break out signal pins from the FPGA would be to use this equation

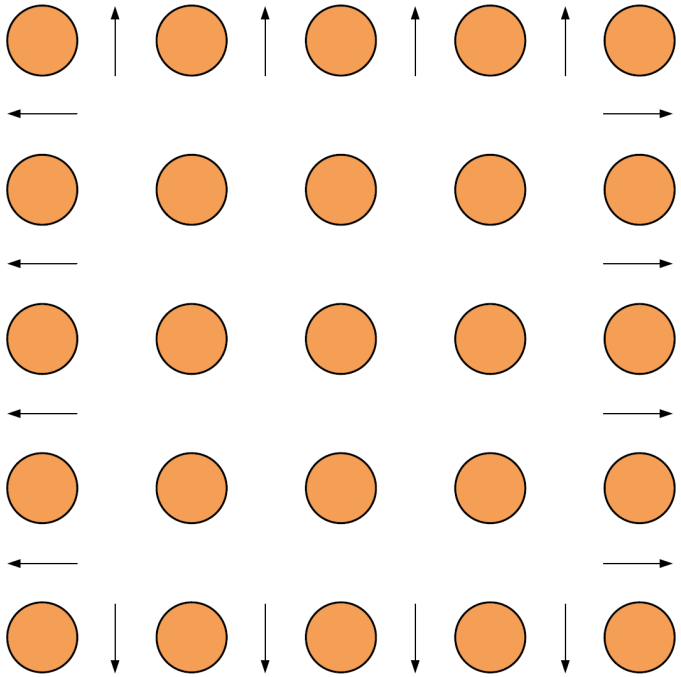
$$Layers = \frac{Signals}{Routing\ Channels \times Routes\ Per\ Channel}$$

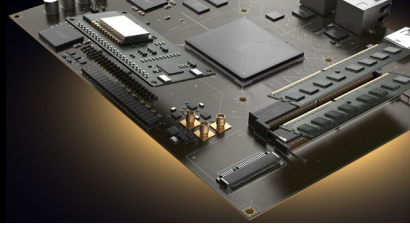
For most FPGAs, the amount of signals is approximately 60% of the number of BGA balls. The other 40% are power and ground signals that are most often routed directly down to planes by vias. This is assuming full I/O utilization. If fewer I/Os are used, then the number of signals to route goes down accordingly.

Routes per channel is either one or two, depending on whether one or two signals are routed between BGA pads.

# Routing Channels

Routing channels are the number of available routing paths out of the BGA area (the number of BGA pins on one side minus one, times four sides). Below shows a 5x5 grid with sixteen total routing channels (four routing channels per side times four sides).





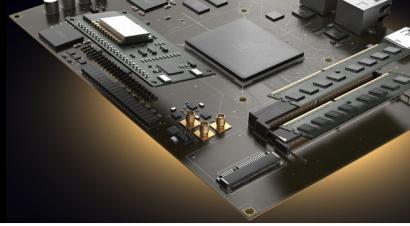
# Layer Count Optimization

The number of layers required for effective routing of BGA's is dictated by a variety of factors, including:

- BGA Size (amount of Pins)
- Pad Size, Pad Pitch, and Trace Width
- Fixed Pinouts

## BGA Size

The amount of pins in a BGA indicates the amount of signals to route. Because of physical space constraints, the amount of signals required to route is proportional to the amount of signal layers required.

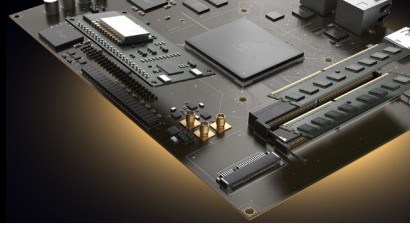


# Pad Size, Pad Pitch and Trace Width

The pad size and pitch determines the available space between adjacent balls for signal escape. Based on the chosen trace width, one or two signals can be routed between adjacent pads. If one signal escapes between adjacent pads, then one signal row can be routed on a single metal layer. The exception to this is the outermost row, which allows two routes per layer.

To facilitate routing in the ball grid area, *necking down* the trace width in the critical space between the BGA pads/vias (the breakout area) is allowable. This then allows for two signal rows to be routed on a single metal layer (or three if routing the outermost row).

The traces can then be widened after they escape the breakout area. Changes in width over very short distances can cause small impedance changes. Validate these issues with the board vendor and signal integrity engineers responsible for the design.



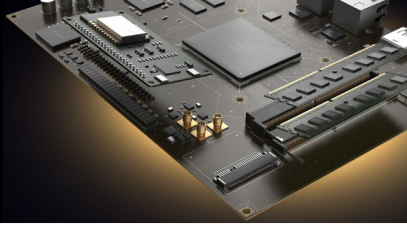
## Fixed Pinouts

FPGA pinouts are designed with maximum flexibility in mind. However, certain FPGA signals, such as JTAG, transceiver inputs and outputs, and Interlaken signals (among others) have fixed locations, which means routing of these signals is limited compared to other signals that can be swapped as needed. Fixed locations lead to layout trade-offs that can have an impact on the number of required signal layers.

## Fabrication Technologies

Several advanced fabrication technologies can be used to reduce the amount of layers required to route a design, although each of these technologies increase fabrications costs of the board:

# BGA and DDR Routing Best Practices



**Blind Vias (+20% to +40% fabrication cost)** – As opposed to a through-hole via, a blind via does not travel from the top layer to the bottom layer. A blind via travels either from the top or bottom layer to an inner signal layer, freeing up room above or below for other routing.

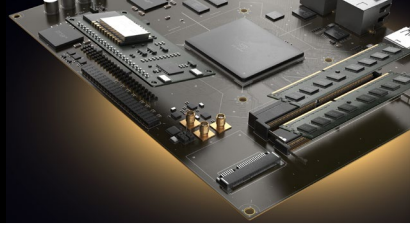
**Buried Vias (+25% to +60% fabrication cost)** – A buried via is located entirely inside the printed circuit board and does not touch the top or bottom layers.

**Micro Vias (+30% fabrication cost)** – A micro via is either a blind or buried via, only much smaller. Micro Vias are most often used in small, high density applications such as cell phones.

**Back-drilled Vias (+10% fabrication cost)** – A back-drilled via is a through-hole via that has a portion of its length *drilled out* such that it is no longer conductive. This improves signal integrity as it removes an unneeded stub from the route.

**Via-In-Pad (+30% fabrication cost)** – A via-in-pad is a via drilled directly beneath a pad. This removes the need for a separate metal trace to be drawn to drop down a via. This can result in improved signal integrity because of lower inductance, but the trade-off is a much higher board fabrication cost.

**Extra Layers (+20% fabrication cost (per every two layers)** – It might be such that the cost to add two (or more) extra signal layers is lower than the cost to add an advanced technology, so adding layers is not always to be considered a negative alternative.



## Maximum Board Thickness

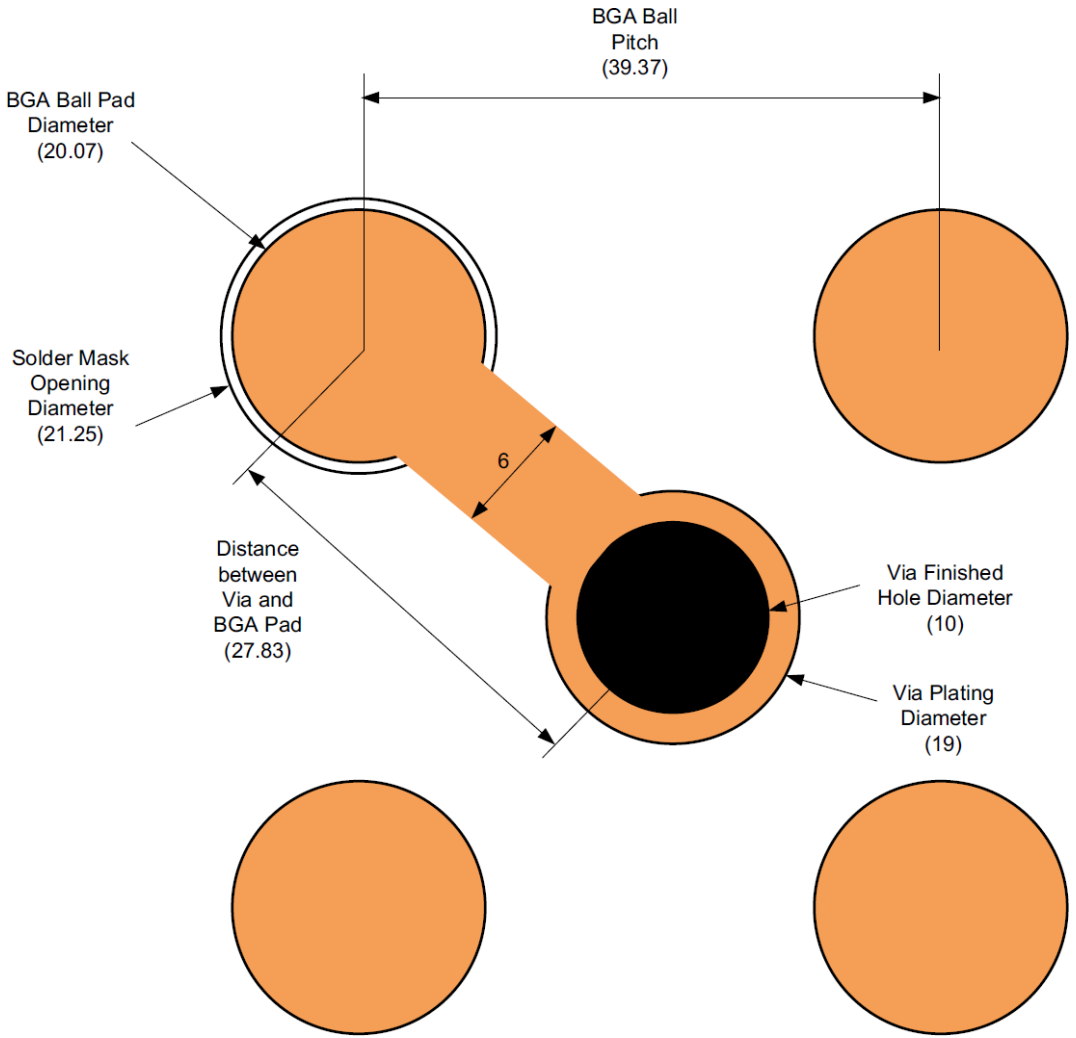
The maximum board thickness is a function of the minimum drill diameter and aspect ratio, both of which are provided by the PCB manufacturer. A typical aspect ratio of 10:1 indicates that the board can be no thicker than ten times the drill diameter. A drill diameter of 13 mils, for example, would lead to a maximum board thickness of 130 mils. With the exception of the CP package, Xilinx recommends finished drill diameters to be 10 mils, which translates to an actual drill diameter of about 13 mils (plating typically reduces the diameter by about 3 mils). A 13 mil drill would lead to a maximum board thickness of 130 mils, assuming a 10:1 aspect ratio. For the CP package, the finished drill diameter of 6 mils approximates a drill diameter of 9 mils, or a maximum board thickness of 90 mils. If a higher board thickness than the drill diameter and aspect ratio can support is required, the use of buried or blind vias can be used, but at a higher manufacturing cost.

## BGA Ball Pad and Via Dimensions

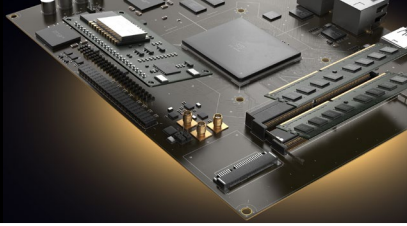
The amount of space available for routing under the FPGA is dependent on the area between the balls in the BGA area (for top and bottom layers), as well as the area between vias (for inner layers). The typical dimensions of FPGA ball pads and vias for 1.0 mm pitch devices are described in following figure.

# BGA and DDR Routing Best Practices

**Recommended Layout Dimensions within BGA Area for 1.0 mm Pitch Devices**




**Ball and Via Dimensions for 1.0mm Pitch FF, FG, FH, FL, RB, and RF Devices (mils)**



## Trace Widths Dimensions inside the BGA Area

The ball pitch and BGA pad/via diameters determine how much space is available to route traces between pads or vias. Standard PCB processes can allow for as low as 3.5 mil trace widths with 3.5 mil spacing. Advanced processes can allow for as low as 2 mil trace widths with 2 mil spacing.

## Trace Routing Between BGA Balls

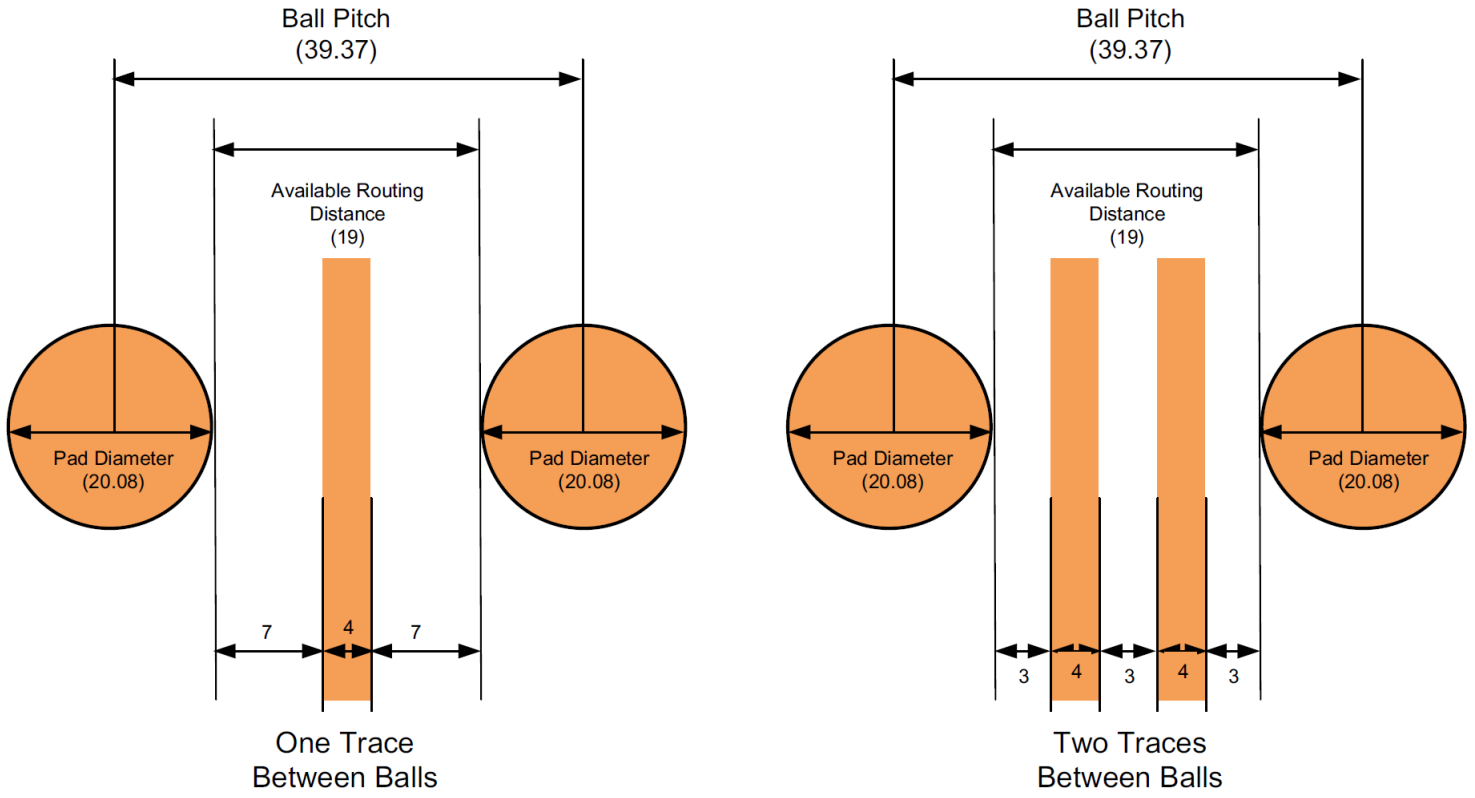
One or two traces can be routed between BGA balls with varying spacing between traces, as shown in the figure in the following slides.

## Trace Routing Between Vias

One or two traces can be routed between vias with varying spacing between traces, as shown in the figure in the following slides.

# BGA and DDR Routing Best Practices

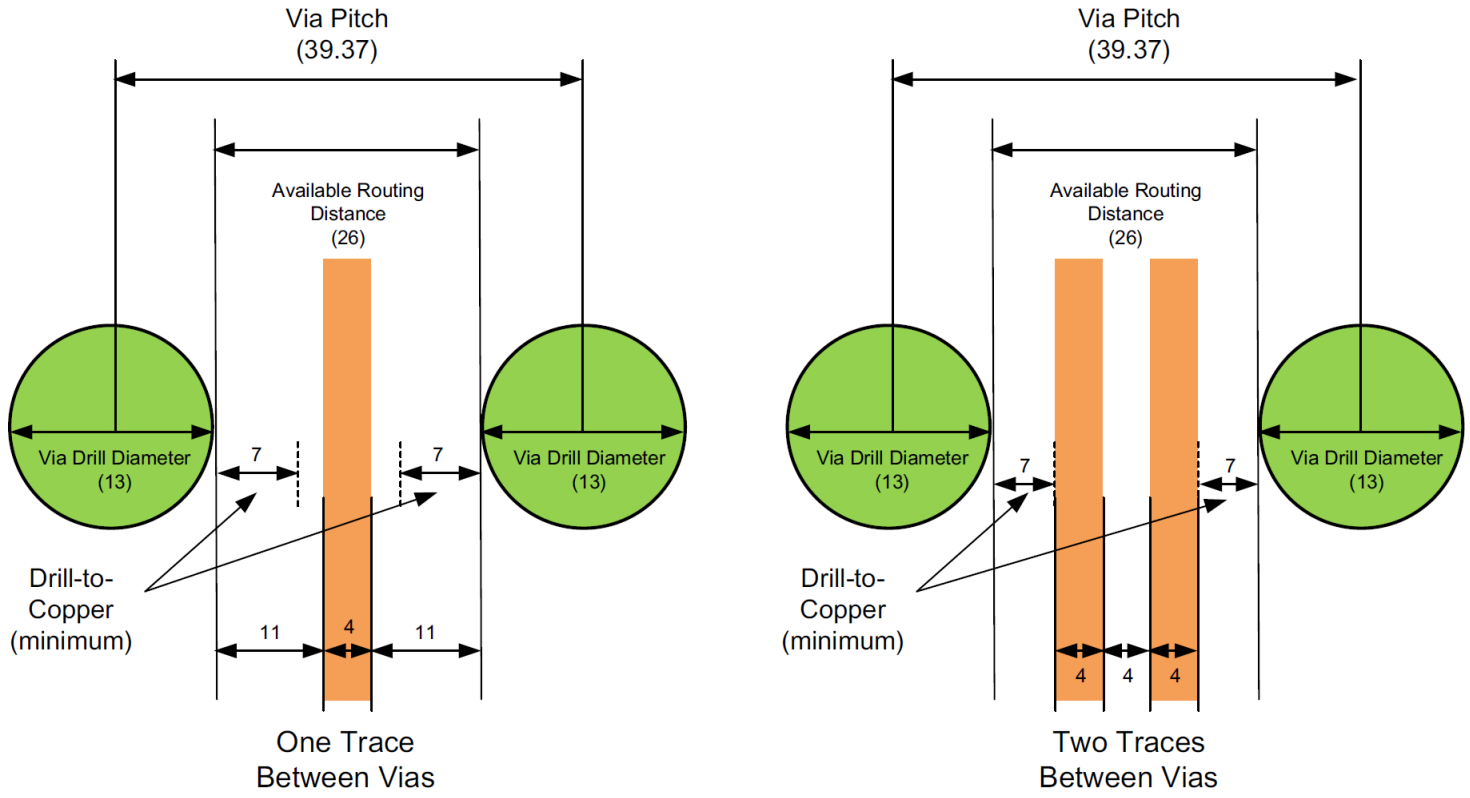
**Recommended Layout Dimensions within BGA Area for 1.0 mm Pitch Devices**



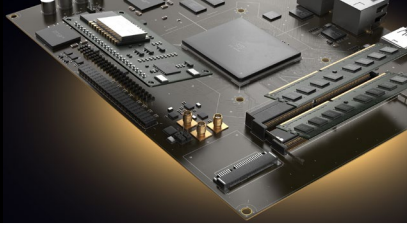

**Trace Routing Between BGA Balls for 1.0mm Pitch FF, FG, FH, FL, RB, and RF Devices (mils)**

# BGA and DDR Routing Best Practices

**Recommended Layout Dimensions within BGA Area for 1.0 mm Pitch Devices**




**Trace Routing Between Vias for 1.0mm Pitch Devices (mils)**



# Altium Tools and Fanout Automation

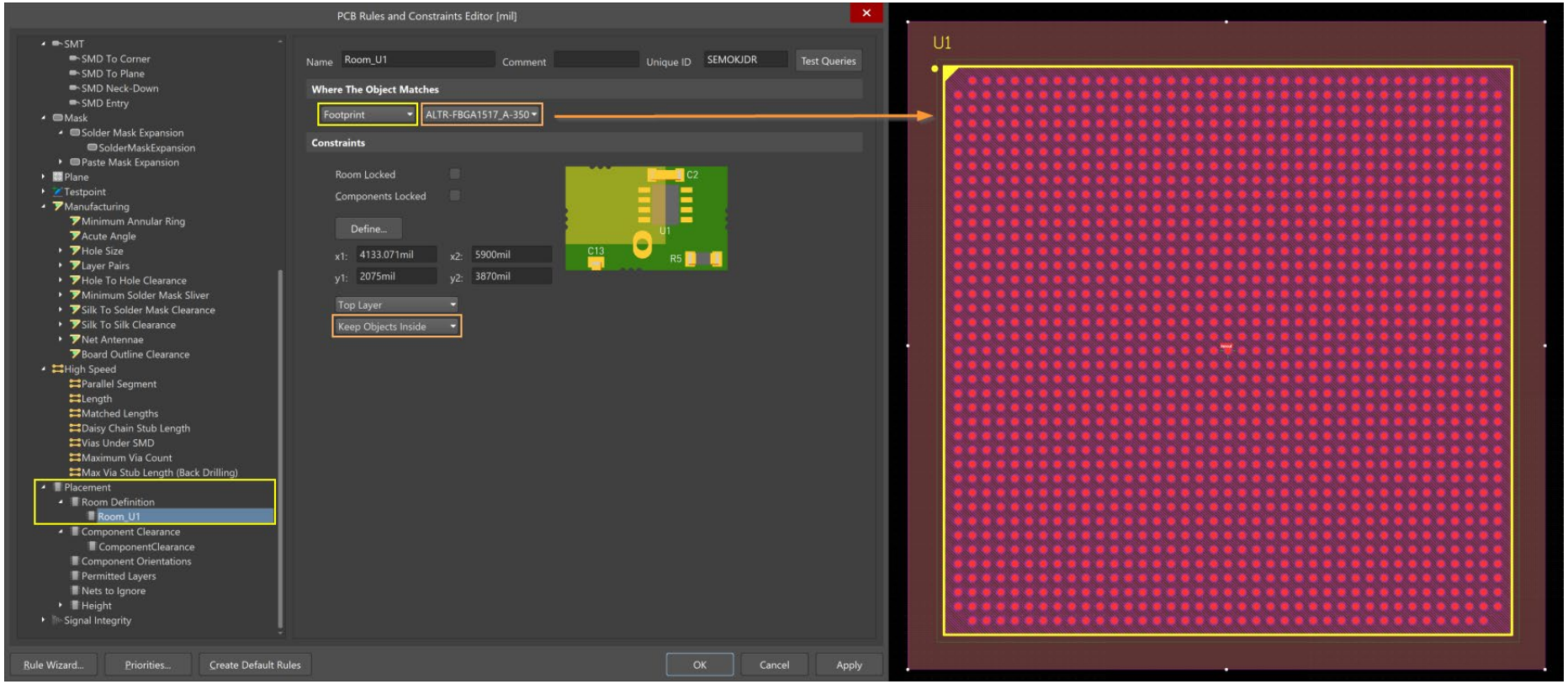
**Design Rules (Rooms, Clearance, Width, Via size, Fanout)**

**Rooms –** A room is an object used to graphically define a region on the PCB, to constrain the physical location of a specific component or group of components. Components can be constrained to either be kept inside or outside of a room. When a room is moved, all components assigned to the room can move with it.

A room in the PCB is defined by a design rule (**Design>>Rules>>Placement>>Room**). The Room's Design Rule Query will target the components associated with the room definition. The default generated rooms that transfer to the PCB from the schematic create design rules that target the automatically generated component class for the corresponding schematic sheet. The room definition can also be accessed by double-clicking on the room in the PCB.

Rooms can also be used to define a physical region on the board where only specific DRC rules are active. This can be useful when fine pitch component packages such as a BGA require a smaller routing Clearance, Width and Via Size constraints relative to the rest of the board area.

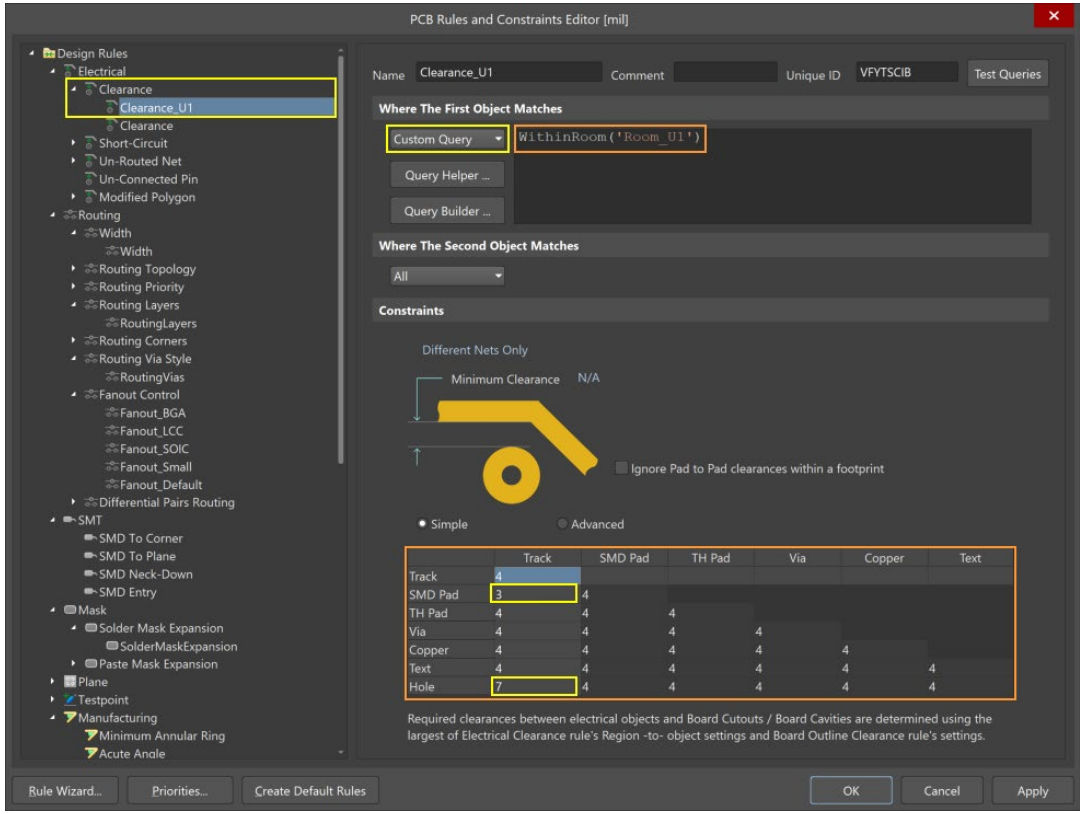
# BGA and DDR Routing Best Practices




Room Definition Design Rule bound to the BGA Footprint Name

# BGA and DDR Routing Best Practices

**Clearance -** This rule defines the minimum clearance allowed between any two primitive objects on a copper layer. Either a single value for clearance can be specified, or different clearances for different object pairings, through use of a dedicated *Minimum Clearance Matrix*. The latter, in combination with rule-scoping, provides the flexibility to build a concise and targeted set of clearance rules to meet even the most stringent of clearance needs.

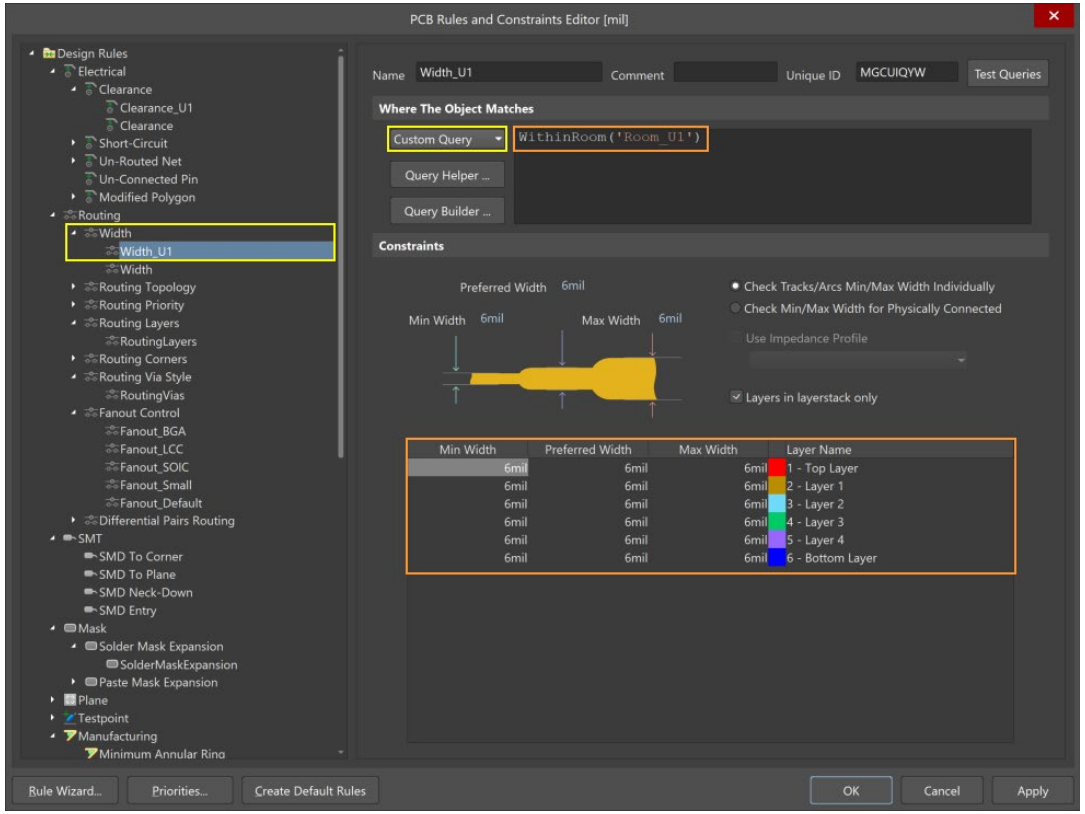



Clearance Design Rule scoped to WithinRoom

# BGA and DDR Routing Best Practices

**Width -** This rule defines the width of tracks placed on the copper (signal) layers.

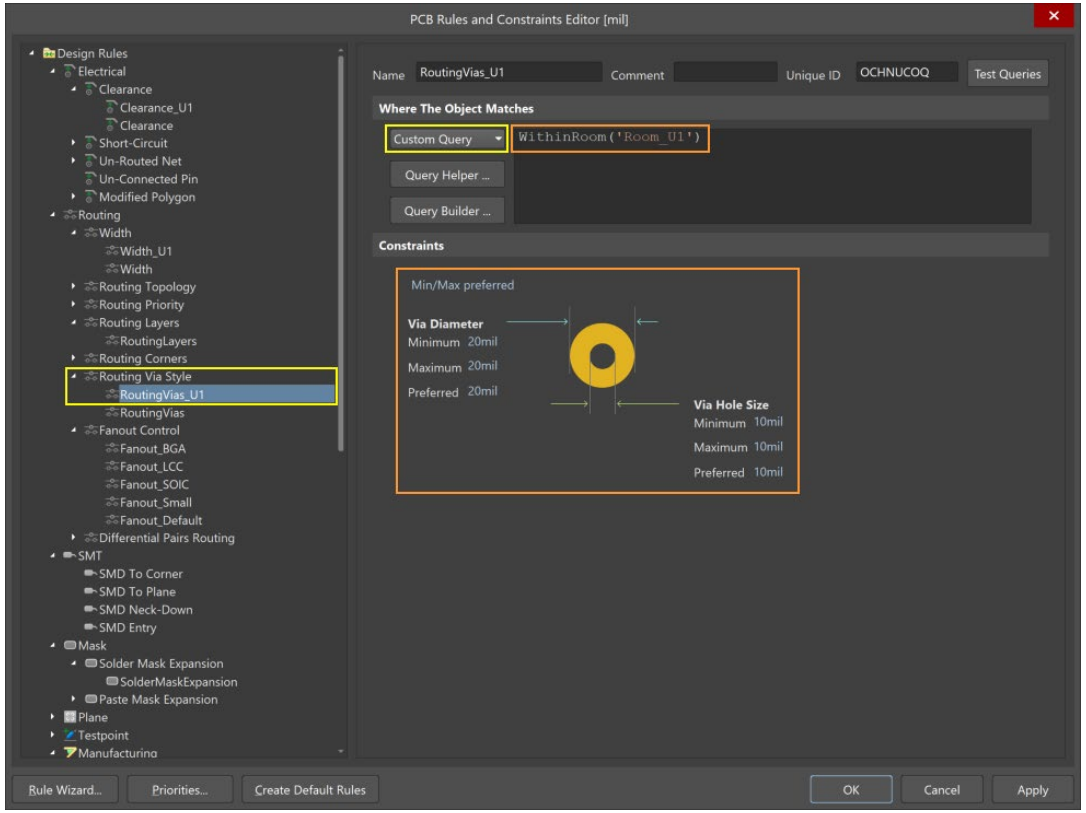
- **Min Width** - specifies the minimum permissible width to be used for tracks when routing the board.
- **Preferred Width** - specifies the preferred width to be used for tracks when routing the board.
- **Max Width** - specifies the maximum permissible width to be used for tracks when routing the board.




Width Design Rule scoped to WithinRoom

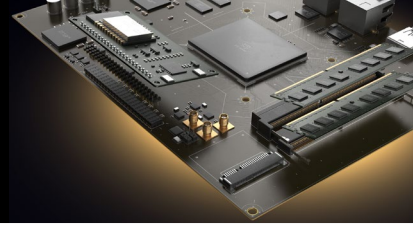
# BGA and DDR Routing Best Practices

**Routing Via Style -** This rule specifies the style of vias that can be used when routing. You have the option to define specific Min/Max/Preferred values for the via's diameter and hole size - defined as part of the rule's constraints.




Routing Via Style Design Rule scoped to WithinRoom

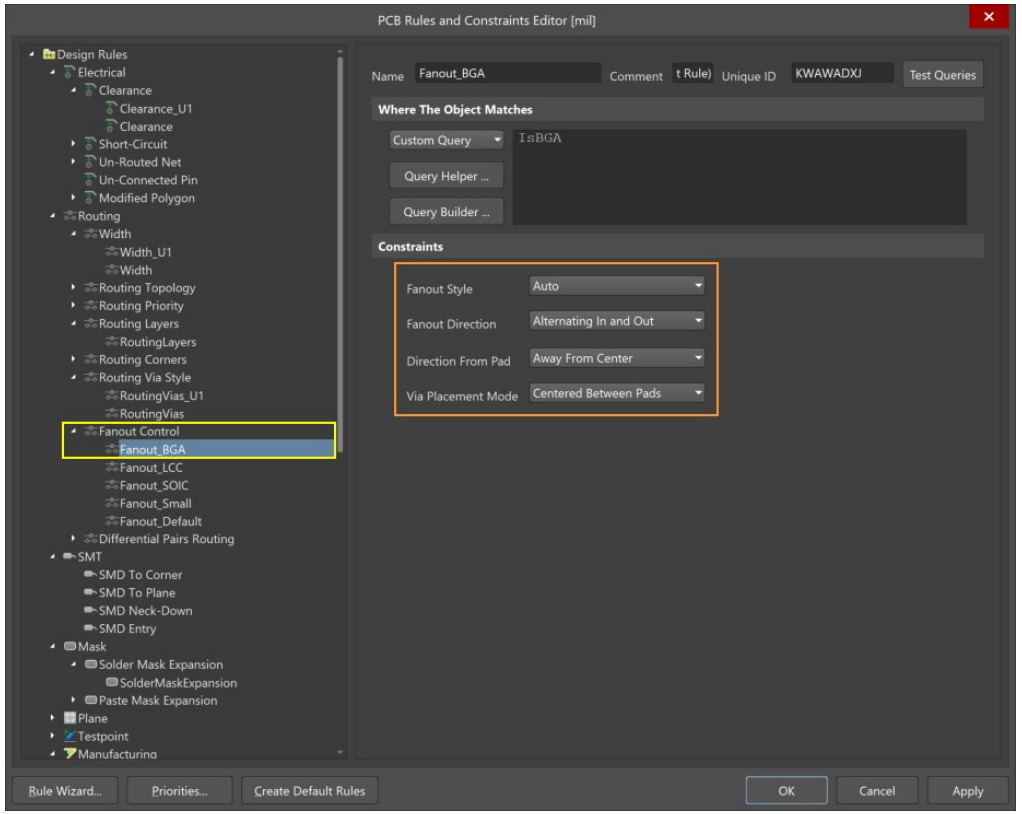
# BGA and DDR Routing Best Practices



**Fanout Control -** Theses rules specify fanout options to be used when fanning out the pads of surface mount components in the design that connect to signal and/or power plane nets. Fanout essentially turns an SMT pad into a thru hole pad, from a routing point of view, by adding a via and connecting track. This greatly increases the probability of successfully routing the board, as a signal is made available to all routing layers instead of just the top or bottom layer. This is particularly needed in high-density designs where routing space is very tight.

- **Fanout Style** - specifies how the fanout vias are placed in relation to the SMT component.
- **Fanout Direction** - specifies the direction to use for the fanout.
- **Direction From Pad** - specifies the direction to use for the fanout. When a BGA component is fanned out, its pads are sectioned into quadrants, with fanout applied to the pads in each quadrant simultaneously.
- **Via Placement Mode** - specifies how the fanout vias are placed in relation to the pads of the BGA component.

# BGA and DDR Routing Best Practices




## Fanout Style - The following options are available:

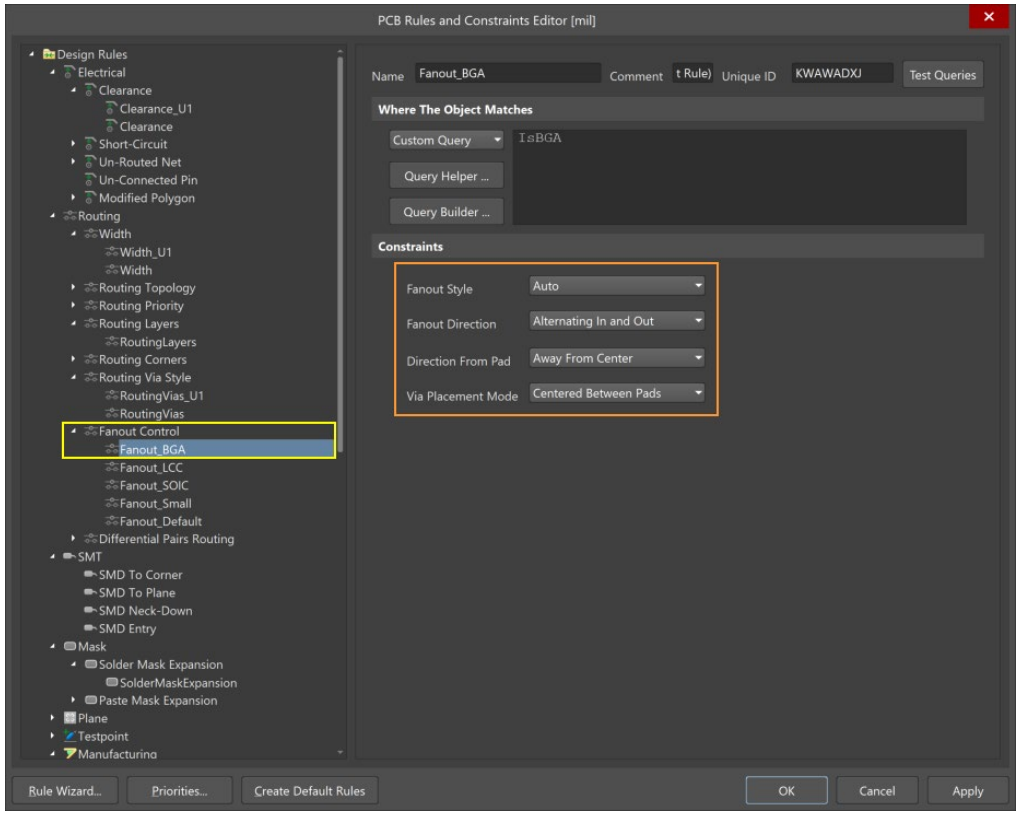
- **Auto** - chooses the style most appropriate for the component technology and in order to give optimal routing space results.
- **Inline Rows** - fanout vias are placed within two aligned rows.
- **Staggered Rows** - fanout vias are placed within two staggered rows.
- **BGA** - fanout occurs in accordance with the specified BGA Options.
- **Under Pads** - fanout vias are placed directly under SMT component pads.

## Fanout Direction - The following options are available:

- **Disable** - do not allow fanout with respect to the SMT components targeted by the rule.
- **Inline In Only** - fanout in an inward direction only. All fanout vias and connecting track will be placed within the component's bounding rectangle.
- **Out Only** - fanout in an outward direction only. All fanout vias and connecting track will be placed outside of the component's bounding rectangle.
- **In Then Out** - fanout all component pads in an inward direction to begin with. All pads that cannot be fanned out in this direction should be fanned out in an outward direction (if possible).
- **Out Then In -** fanout all component pads in an outward direction to begin with. All pads that cannot be fanned out in this direction should be fanned out in an inward direction (if possible).
- **Alternation In and Out -** fanout all component pads (where possible) in an alternating fashion, first inward then outward.

Fanout Control Design Rules

# BGA and DDR Routing Best Practices




## Direction From Pad - The following options are available:

- **Away From Center** - fanout for pads in each quadrant is applied following a 45° angle away from the component's center.
- **North-East** - all pads, in each quadrant, are fanned out in a North-Easterly direction (45° anti-clockwise from the horizontal).
- **South-East** - all pads, in each quadrant, are fanned out in a South-Easterly direction (45° clockwise from the horizontal).
- **South-West** - all pads, in each quadrant, are fanned out in a South-Westerly direction (135° clockwise from the horizontal).
- **North-West** - all pads, in each quadrant, are fanned out in a North-Westerly direction (135° anti-clockwise from the horizontal).
- **Towards Center -** fanout for pads in each quadrant is applied following a 45° angle toward the component's center. In most cases, uniformity of direction will not be possible due to required fanout space already taken by another pads' fanout via. In these cases, fanout will occur in the next available direction (North-East, South-East, South-West, North-West).

## Via Placement Mode - The following options are available:

- **Close To Pad (Follow Rules)** - fanout vias will be placed as close to their corresponding SMT component pads as possible, without violating defined clearance rules.
- **Centered Between Pads** - fanout vias will be centered between the SMT component pads.

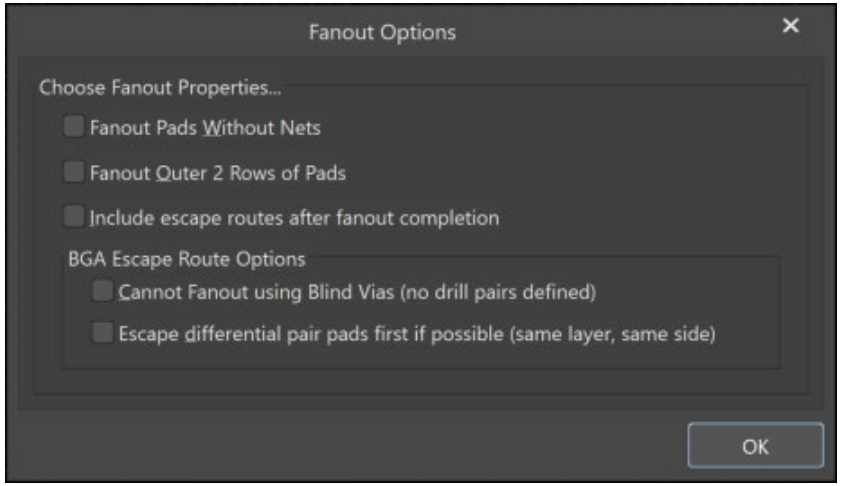
Fanout Control Design Rules

## Fanout Options

This dialog allows you to specify fanout and escape routing options. Typical fanout behavior is for used inner pads to first be fanned out using the traditional dog-bone (a short route with a via on the end) to access another layer, and then from the via, they are escape-routed out just beyond the edge of the device, working through the available routing layers until all pads have been escape-routed. Ultimately, this makes routing connections to them much easier.

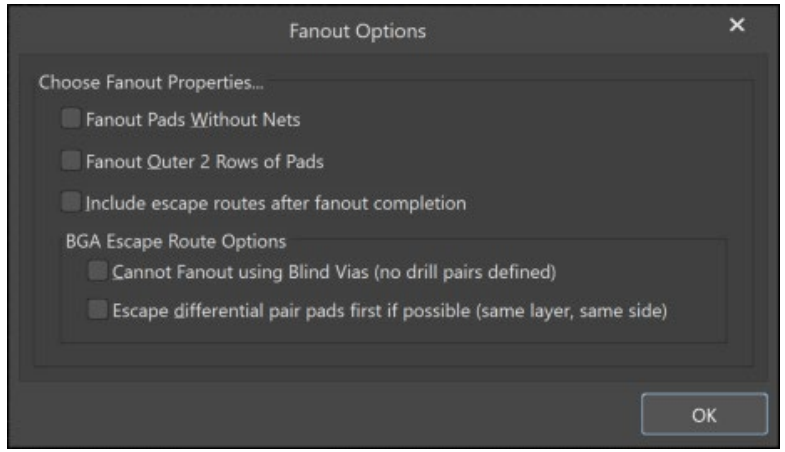
**The dialog is accessed from the PCB Editor in one of the following ways:**

- Use any of the commands on the **Route » Fanout** sub-menu.
- Right-click over a placed component in the design workspace then choose the **Component Actions » Fanout Component** command from the context menu.




Fanout Options

# BGA and DDR Routing Best Practices




## Options/Controls -

- **Fanout Pads Without Nets** - enable this option to fanout pads from the component even if they have no nets assigned to them. When this option is disabled, only pads with nets assigned will be fanned out.
- **Fanout Outer 2 Rows of Pads** - enable this option to fanout pads from the component including the outer two rows (which are usually easily routed).
- **Include escape routes after fanout completion** - enable this option to add escape routing to each fanout. Escape routing places tracks onto the fanout vias and component pads, bringing them out to the edges of the component, to make routing connections to them easier.

## BGA Escape Route Options - The options in this region of the dialog only become available when the **Include escape routes after fanout completion** option is enabled.

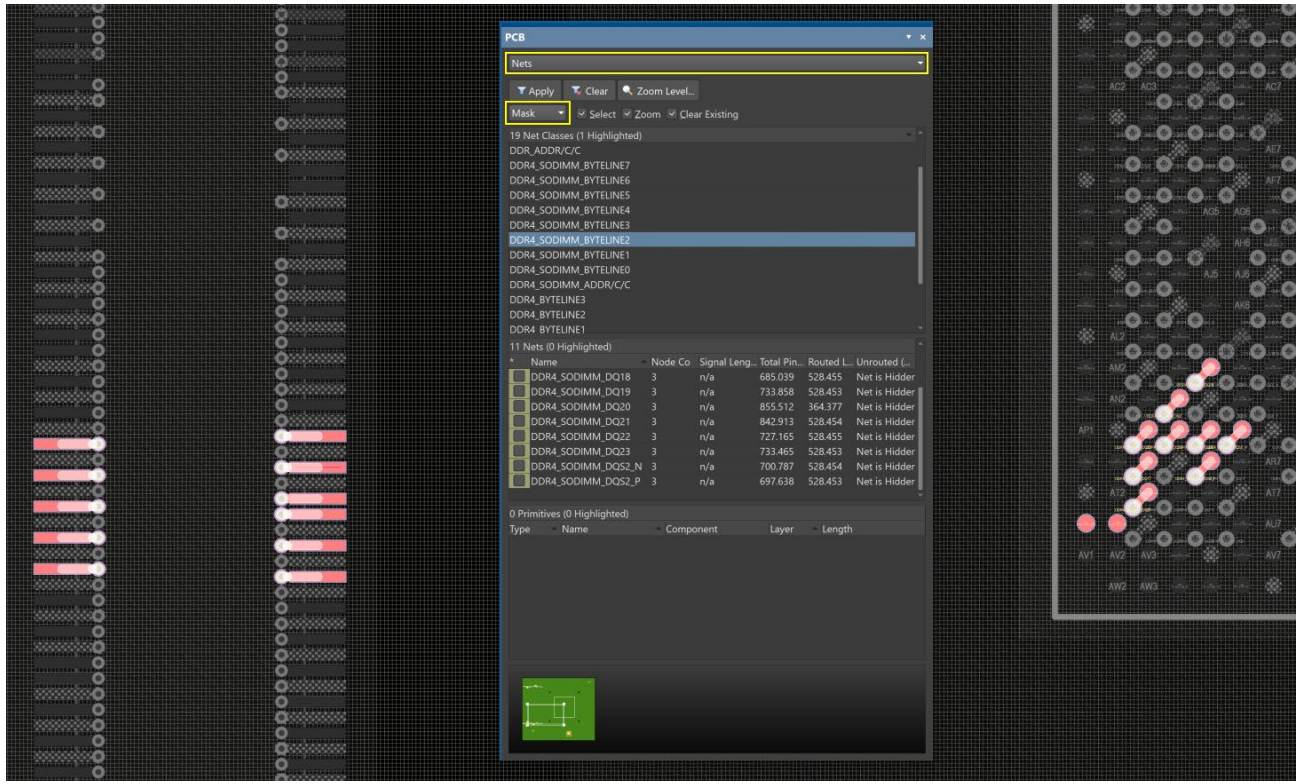
- **Update fanout using Blind Vias (BGA escape routing only)** - enable this option to drop blind vias between configured drill-pair layers in the layer stack. When this option is disabled, only through-hole vias will be dropped regardless of drill-pair layer settings.
- **Escape differential pair pads first if possible (same layer, same side)** - enable this option to fanout and escape route any assigned differential pair nets together, and before performing other fan out operations, effectively keeping their routes together. The fanout will place escape routing tracks on to the same layer and as adjacent as possible.

Fanout Options

# BGA and DDR Routing Best Practices

## Signal Identification using the PCB Panel

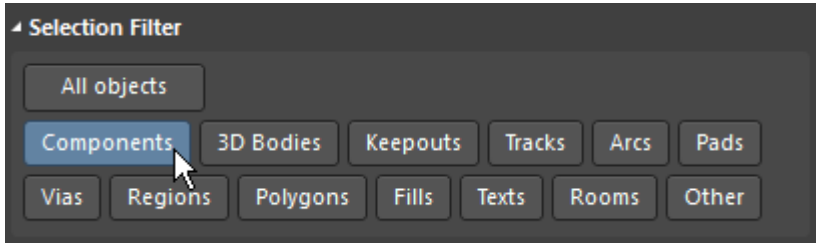
Enable the Mask feature in the PCB Panel to easily identify signals for Routing Layer and Blind/Buried via assignment.

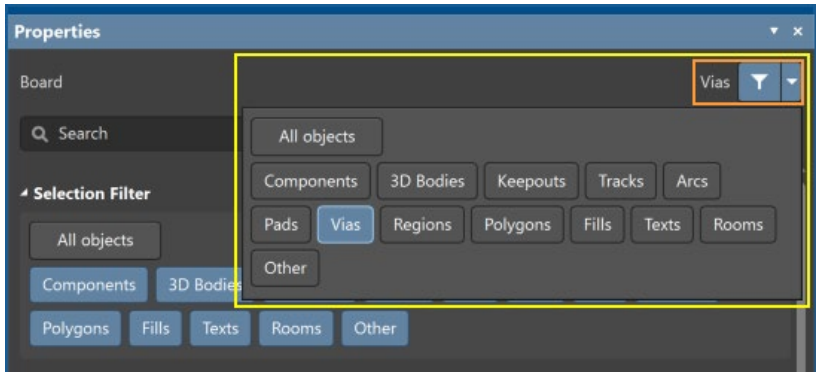



Identifying Signals with the PCB Panel

## Selection Methods for editing Fanout

Any fine tuning needed is done easily with the use of Selection Methods such as the Pre and Post Selection filter of the Properties Panel along with the mouse drag options of Select Within or Select Touching.




**Select Within** - click and drag a blue rectangle from Left to Right to select all unlocked objects allowed through your selection filter, that are *completely within* the selection rectangle.

**Select Touching** - click and drag a green rectangle from Right to Left to select all unlocked objects allowed through your selection filter, that *touch* the selection rectangle.

Selection Methods

ALTIUM DESIGNER

# BGA and DDR Routing Best Practices