Altium

ALTIUMLIVE 2018:
PCB DESIGN BEST PRACTICES:
ADVANCED STACK-UP IN ALTIUM DESIGNER

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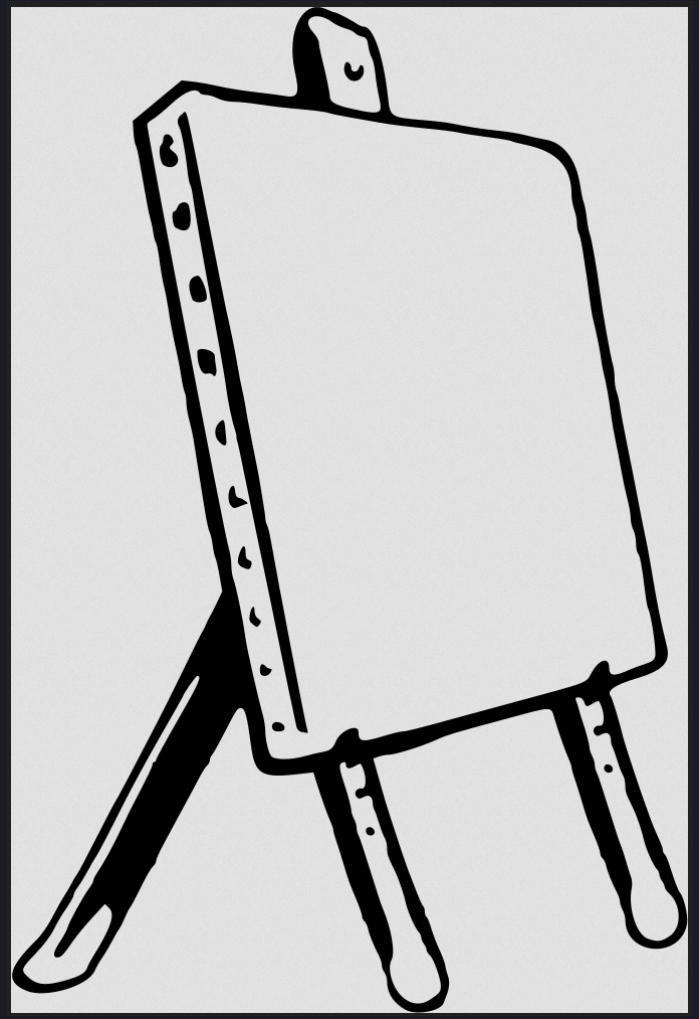
San Diego
October 3rd-5th,2018

PCB Layer Stack-Up Agenda

1. Introduction – Why learn about PCB Stack-Ups?
2. PCB Layer Stack-Up Physics
3. Communicating About Stack-Ups and What Do You Ask?
4. Tools and Processes
5. Altium Designer 19 Implementation Examples



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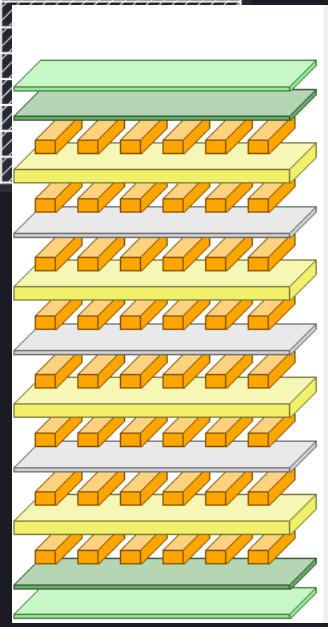
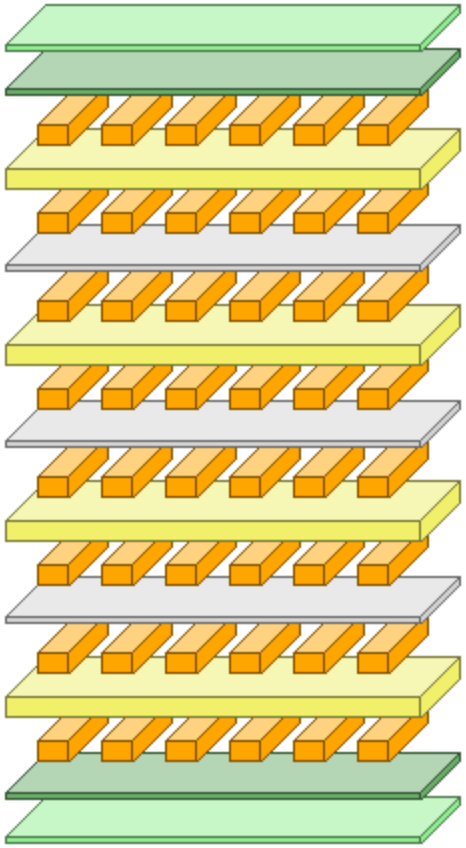
Layer	Name	Material	Thickness	Constant	Board Layer Stack
1	Top Overlay				
2	Top Solder	Solder Resist	0.010mm	3.5	
3	L01_Top_Layer	Copper	0.025mm		
4	Dielectric_1	EM-827B 1080(68)	0.067mm	3.7	
5	L02_Signal_Layer_1	Copper	0.025mm		
6	Dielectric_2	EM-827B 1080(68)	0.072mm	3.7	
7	L03_Signal_Layer_2	Copper	0.025mm		
8	Dielectric 3	EM-827B 1080(68)	0.082mm	3.7	
9	L04_Signal_Layer_3	Copper	0.025mm		
10	Dielectric 4	EM-827B 2116X1(68)	0.128mm	3.8	
11	L05_Signal_Layer_4	Copper	0.012mm		
12	Dielectric 5	EM827 1080X1	0.076mm	3.8	
13	L06_Internal_Plane_2	Copper	0.012mm		
14	Dielectric 6	EM-827B 2116X1(68)	0.129mm	4.2	
15	L07_Internal_Plane_3	Copper	0.025mm		
16	Dielectric 7	EM827 2116X1	0.127mm	4.1	
17	L08_Internal_Plane_4	Copper	0.025mm		
18	Dielectric 8	EM-827B 2116X1(68)	0.129mm	4.2	
19	L09_Internal_Plane_5	Copper	0.012mm		
20	Dielectric 9	EM827 1080X1	0.076mm	3.8	
21	L10_Signal_Layer_5	Copper	0.012mm		
22	Dielectric 10	EM-827B 2116X1(68)	0.128mm	3.8	
23	L11_Signal_Layer_6	Copper	0.025mm		
24	Dielectric 14	EM-827B 1080(68)	0.081mm	3.7	
25	L12_Signal_Layer_7	Copper	0.025mm		
26	Dielectric 12	EM-827B 1080(68)	0.072mm	3.7	
27	L13_Signal_Layer_8	Copper	0.025mm		
28	Dielectric 13	EM-827B 1080(68)	0.067mm	3.7	
29	L14_Bottom_Layer	Copper	0.025mm		
30	Bottom Solder	Solder Resist	0.010mm	3.5	
31	Bottom Overlay				



Layer Name	Type	Material	Thickness (mm)	Dielectric Material	Dielectric Constant	Pullback (mm)	Orientation	Coverlay Expansion
Top Overlay	Overlay							
Top Solder	Solder Mask/Co...	Surface Material	0.02032	Solder Resist	3.5			0
Top Layer(1)	Signal	Copper	0.04826				Top	
Dielectric 1	Dielectric	Core	0.254	2x 2313 - 57%	4.2			
MidLayer(2)	Signal	Copper	0.03048				Not Allowed	
Dielectric 2	Dielectric	Prepreg	0.127	FR-4	4.2			
MidLayer(3)	Signal	Copper	0.03048				Not Allowed	
Dielectric 3	Dielectric	Core	0.254	2x 2313 - 57%	4.2			
MidLayer(4)	Signal	Copper	0.03048				Not Allowed	
Dielectric 4	Dielectric	Prepreg	0.127	FR-4	4.2			
MidLayer(5)	Signal	Copper	0.03048				Not Allowed	
Dielectric 5	Dielectric	Core	0.254	2x 2313 - 57%	4.2			
MidLayer(6)	Signal	Copper	0.03048				Not Allowed	
Dielectric 6	Dielectric	Prepreg	0.127	FR-4	4.2			
MidLayer(7)	Signal	Copper	0.03048				Not Allowed	
Dielectric 7	Dielectric	Core	0.254	2x 2313 - 57%	4.2			
Bottom Layer(8)	Signal	Copper	0.04826				Bottom	
Bottom Solder	Solder Mask/Co...	Surface Material	0.02032	Solder Resist	3.5			0
Bottom Overlay	Overlay							



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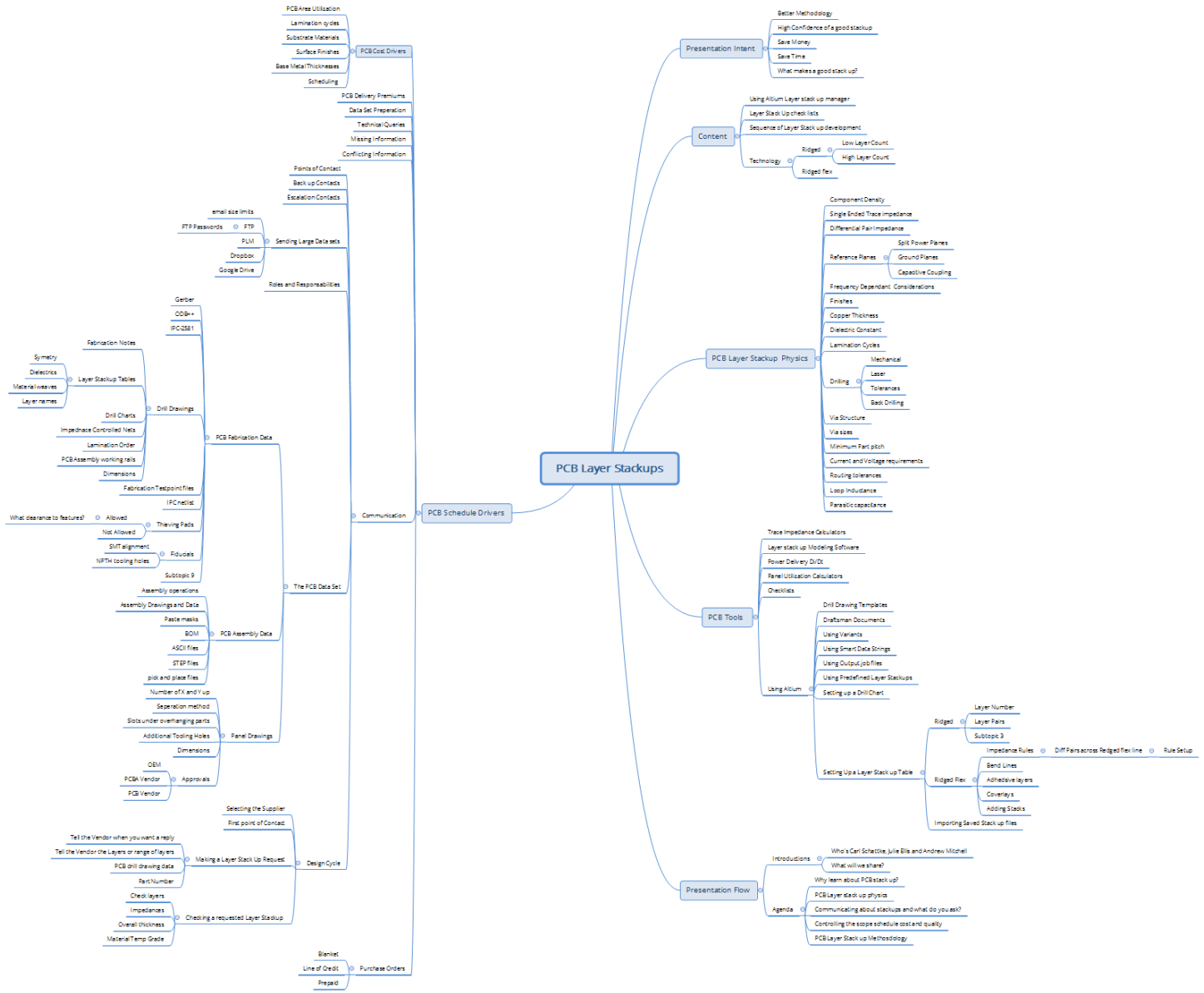
MidLayer(7)	Signal	Copper	0.03048				Not Allowed	
Dielectric 7	Dielectric	Core	0.254	2x 2313 - 57%	4.2			
Bottom Layer(8)	Signal	Copper	0.04826				Bottom	
Bottom Solder	Solder Mask/Co...	Surface Material	0.02032	Solder Resist	3.5			0
Bottom Overlay	Overlay							

PCB Layer Stack Up Mind Map



PCB Layer Stack Up
Agenda:

1. **Introduction -Why learn about PCB Stack Ups?**
2. PCB Layer Stackup Physics
3. Communicating about stack ups and what do you ask?
4. Tools and processes
5. Implementation Examples

Why do we want to get PCB Layer Stackup right?

- Can save time
- Can save us BIG money
- Can save aggravation
- Can save us from massive rework
- Can save us or accelerate design cycles
- Can help us save face in our organization
- Can save us from a faulty process

We are going to explore this at the board physics level, the people level and the tools and process level.

What's important to learn about Printed Circuit Board Layer Stack-ups?

- Stack up impacts design options
- Stack up impacts design time
- Stack up controls costs
- Stack up can mitigate Signal Integrity issues
- Stack up impacts production lead time

Stack up impacts design options

- More layers allow for more signals
- More layers allows for higher current capacity
- More Dielectric layers can improve voltage isolation
- More layers allows for denser fine pitch and BGA parts
- Proper layer stackup provides an excellent return path.
- Stack up control, controls Signal Integrity
- Stack up impacts production lead time

Some PCB Layer Stackup horror stories

- The Impossible stack
- The Rework
- The Money Burner
- The Potato Chip

The Impossible Stack-up

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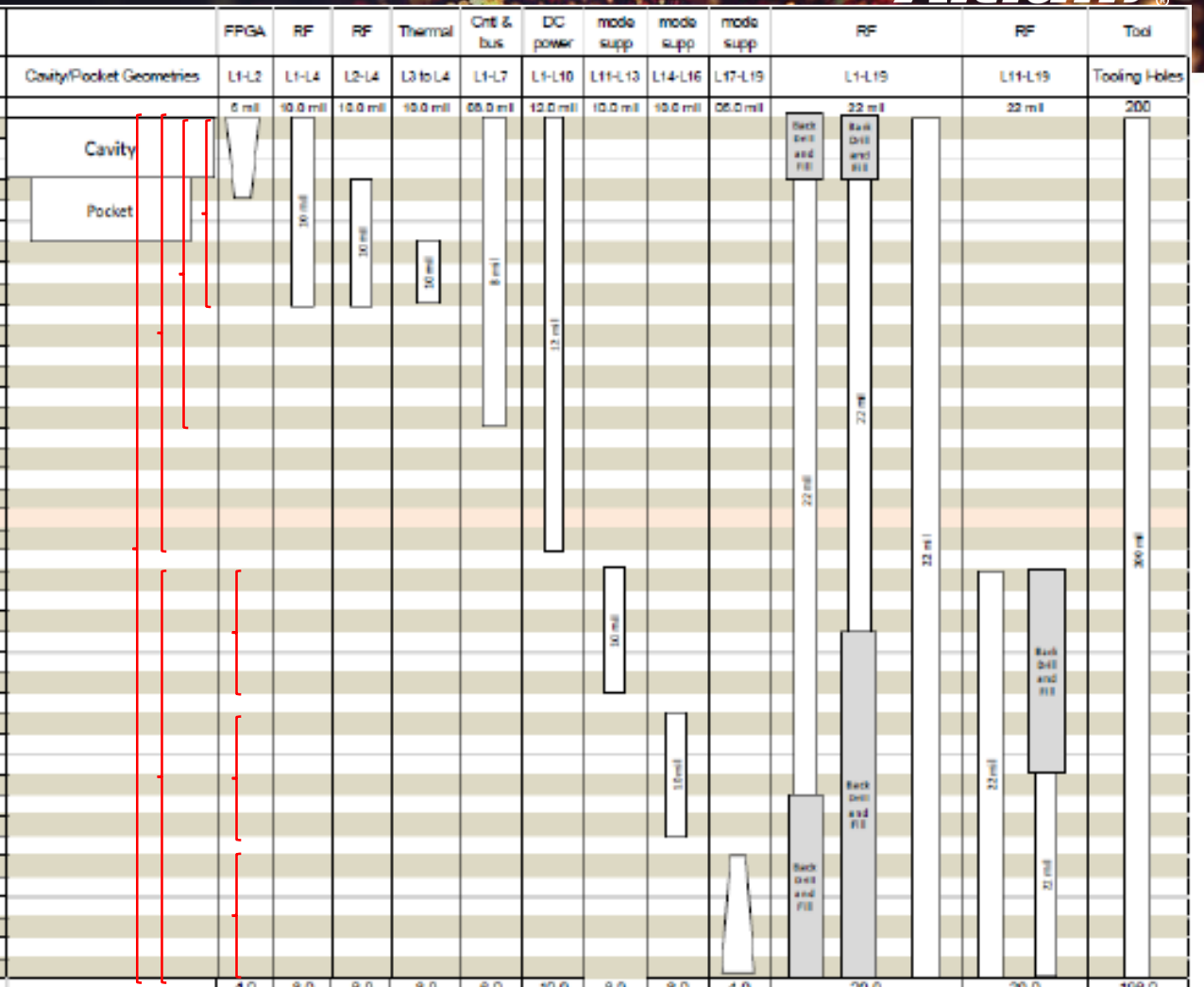
	Layer No.	Layer Name	Layer Type	Material / Part Number	Weight (oz.)	Material Thickness (mil) nom.	min.	max.	Finished Thickness (mil) nom.	min.	max.
RF Coax 1 RF 0.022" GND to GND	1	RF1 Ground/FPGA Mount	Metal	C110 Copper, Rolled	1.5	2.07	2.07	2.07	3.87	3.87	3.87
			Substrate	CLTE-XT Core	-	10.00	9.00	11.00	10.00	9.00	11.00
			Bond Ply	2929 Bond Ply 2 mil (X1)	-	2.00	1.90	2.10	2.00	1.90	2.10
	2	RF1 Signal/MMIC Control	Metal	C110 Copper, Rolled	0.5	0.69	0.69	0.69	0.69	0.69	0.69
			Substrate	CLTE Core	-	3.00	2.90	3.10	3.00	2.90	3.10
			Bond Ply	2929 Bond Ply 2 mil (X1)	-	2.00	1.90	2.10	2.00	1.90	2.10
	3	Gnd/Therm1	Metal	C110 Copper, Rolled	1.0	1.38	1.38	1.38	1.38	1.38	1.38
			Substrate	CLTE-XT Core(s)	-	5.00	4.90	5.10	5.00	4.90	5.10
	4	RF1 Ground	Metal	C110 Copper, Rolled	1.5	2.07	2.07	2.07	2.87	2.87	2.87
			Bond Ply	2929 Bond Ply 3 mil (X2)	-	6.00	5.70	6.30	6.00	5.70	6.30
DC / Digital / Control	5	DC GND	Metal	C110 Copper, Rolled	0.5	0.69	0.69	0.69	1.29	1.29	1.29
			Substrate	CLTE-AT Core	-	5.00	4.90	5.10	5.00	4.90	5.10
	6	DC/CNTL	Metal	C110 Copper, Rolled	0.5	0.69	0.69	0.69	0.69	0.69	0.69
			Bond Ply	2929 Bond Ply 2 mil (X1); 3 mil (X1)	-	5.00	4.90	5.10	5.00	4.90	5.10
	7	DC/CNTL	Metal	C110 Copper, Rolled	1.0	1.38	1.38	1.38	1.38	1.38	1.38
			Substrate	CLTE-AT Core	-	5.00	4.90	5.10	5.00	4.90	5.10
	8	DC Power Plane	Metal	C110 Copper, Rolled	1.0	1.38	1.38	1.38	1.38	1.38	1.38
			Bond Ply	2929 Bond Ply 2 mil (X1); 3 mil (X1)	-	5.00	4.90	5.10	5.00	4.90	5.10
	9	DC Power Plane	Metal	C110 Copper, Rolled	1.0	1.38	1.38	1.38	1.38	1.38	1.38
			Substrate	CLTE-AT Core	-	5.00	4.90	5.10	5.00	4.90	5.10
	10	DC/ GND	Metal	C110 Copper, Rolled	1.0	1.38	1.38	1.38	1.98	1.98	1.98
			Bond Ply	2929 Bond Ply 3 mil (X2)	-	6.00	5.70	6.30	6.00	5.70	6.30
RF Coax 2 RF 0.022" GND to GND	11	RF2 Ground	Metal	C110 Copper, Rolled	1.5	2.07	2.07	2.07	2.67	2.67	2.67
			Substrate	CLTE-XT Core	-	10.00	9.00	11.00	10.00	9.00	11.00
	12	RF2 Signal - resistors	Metal	C110 Copper, Rolled; Resistors	0.5	0.69	0.69	0.69	0.69	0.69	0.69
			Bond Ply	2929 Bond Ply 2 mil (X1)	-	2.00	1.90	2.10	2.00	1.90	2.10
			Substrate	CLTE-XT Core	-	10.00	9.00	11.00	10.00	9.00	11.00
	13	RF2 Ground	Metal	C110 Copper, Rolled	1.0	1.38	1.38	1.38	2.58	2.58	2.58
			Bond Ply	2929 Bond Ply 3 mil (X2)	-	6.00	5.70	6.30	6.00	5.70	6.30
RF Coax 3 RF 0.022" GND to GND	14	RF3 Ground	Metal	C110 Copper, Rolled	1.0	1.38	1.38	1.38	2.58	2.58	2.58
			Substrate	CLTE-XT Core	-	10.00	9.00	11.00	10.00	9.00	11.00
			Bond Ply	2929 Bond Ply 2 mil (X1)	-	2.00	1.90	2.10	2.00	1.90	2.10
	15	RF3 Signal - resistors	Metal	C110 Copper, Rolled; Resistors	0.5	0.69	0.69	0.69	0.69	0.69	0.69
			Substrate	CLTE-XT Core	-	10.00	9.00	11.00	10.00	9.00	11.00
	16	RF3 Ground	Metal	C110 Copper, Rolled	1.0	1.38	1.38	1.38	1.98	1.98	1.98
			Bond Ply	2929 Bond Ply 3 mil (X2)	-	6.00	5.70	6.30	6.00	5.70	6.30
RF Coax 4 RF 0.022" GND to GND	17	RF4 Ground	Metal	C110 Copper, Rolled	0.5	0.69	0.69	0.69	1.29	1.29	1.29
			Substrate	CLTE-XT Core(s)	-	5.00	4.90	5.10	5.00	4.90	5.10
			Bond Ply	2929 Bond Ply 2 mil (X1)	-	2.00	1.90	2.10	2.00	1.90	2.10
	18	RF4 Signal	Metal	C110 Copper, Rolled	0.5	0.69	0.69	0.69	0.69	0.69	0.69
			Substrate	CLTE-XT Core	-	10.00	9.00	11.00	10.00	9.00	11.00
	19	RF4 Ground	Metal	C110 Copper, Rolled	1.5	2.07	2.07	2.07	3.87	3.87	3.87

			Total Thickness (mil) nom.	min.	max.	Total Final Thickness (mil) nom.	min.	max.
Layer Count	16	RF2, RF3 as separate	148.6	142.8	150.8	150.9	152.4	159.4
Press Count	7	RF2 and RF3 and RF4 as sub lam						
		RF1 and DC/Dig/CNTL as separate						
RF Gnd Cu Weight	0.5 oz	Layer 3 to Gnd						
DC Cu Weight	0.5 oz	RF1 to						
RF Signal Cu Weight	0.5 oz							

Notes:



Layer Stack & Via Details

16 metal layers

Rogers (Arlon)

Mechanical Properties

CTE match needs review

Total Mass: 157g Nom. (0.346#)

The Rework Stack-Ups (3 Similar Asia Transfers with NA DFM Rules)

North America Design Rules: 8mil/16mil/28mil drill/back-drill/antipad

Layer	Cu Thick. (mils)	Cu Foil wt (oz)	DK	Lam. Thick. (mils)	Description
1	2.10	.5 oz			Foil, .5 oz Reduce to .333 oz
			3.47	3.10	Prepreg R5620 1078
2	0.60	.5 oz			
			3.76	5.00	Core R5725 5mils .5 oz / .5 oz 1078x2 RTF
3	0.60	.5 oz			
			3.38	8.05	Prepreg R5620 1067/1078/1067
4	0.60	.5 oz			
			3.76	5.00	Core R5725 5mils .5 oz / .5 oz 1078x2 RTF
5	0.60	.5 oz			
			3.38	8.05	Prepreg R5620 1067/1078/1067
6	0.60	.5 oz			
			3.76	5.00	Core R5725 5mils .5 oz / .5 oz 1078x2 RTF
7	0.60	.5 oz			
			3.38	7.95	Prepreg R5620 1078/1067/1078
8	2.50	2 oz			
			4.00	2.00	Core R5725 2mils 2 oz / 2 oz 1067x1
9	2.50	2 oz			
			3.33	3.85	Prepreg R5620 1067/1067
10	2.50	2 oz			
			4.00	2.00	Core R5725 2mils 2 oz / 2 oz 1067x1
11	2.50	2 oz			
			3.38	7.95	Prepreg R5620 1078/1067/1078
12	0.60	.5 oz			
			3.76	5.00	Core R5725 5mils .5 oz / .5 oz 1078x2 RTF
13	0.60	.5 oz			
			3.38	8.05	Prepreg R5620 1067/1078/1067
14	0.60	.5 oz			
			3.76	5.00	Core R5725 5mils .5 oz / .5 oz 1078x2 RTF
15	0.60	.5 oz			
			3.38	8.05	Prepreg R5620 1067/1078/1067
16	0.60	.5 oz			
			3.76	5.00	Core R5725 5mils .5 oz / .5 oz 1078x2 RTF
17	0.60	.5 oz			
			3.47	3.10	Prepreg R5620 1078
18	2.10	.5 oz			Foil, .5 oz Reduce to .333 o z

Layers	Drill Type			
1 - 18	PTH	Via filling	109.35	Thickness over Laminate
			113.55	Thickness over Copper
			114.95	Thickness over Soldermask

Impedance Table

Layer	Structure Type	Coated Microstrip	Target Impedance (ohms)	Impedance Tolerance (ohms)	Target Linewidth (mils)	Proposed Linespacing (mils)	Reference Layers	Modelled Linewidth (mils)	Modelled Impedance (ohms)
1	Single Ended	Yes	33.00	+/-5	11.00		(2)		32.90
1	Single Ended	Yes	40.00	+/-5	7.90		(2)		39.90
1	Single Ended	Yes	50.00	+/-5	5.00		(2)		50.08
1	Edge Coupled Differential	Yes	75.00	+/-7.5	6.70	5.30	(2)	6.70	75.06
1	Edge Coupled Differential	Yes	88.00	+/-8.8	5.50	8.50	(2)	5.50	88.41
1	Edge Coupled Differential	Yes	100.00	+/-10	4.70	14.30	(2)	4.70	99.47
3	Single Ended	---	33.00	+/-5	12.20		(2, 4)		33.20
3	Single Ended	---	38.00	+/-5	9.80		(2, 4)		38.21
3	Single Ended	---	50.00	+/-5	6.00		(2, 4)		50.32
3	Edge Coupled Differential	---	75.00	+/-7.5	8.30	4.70	(2, 4)	8.30	74.88
3	Edge Coupled Differential	---	88.00	+/-8.8	6.80	7.20	(2, 4)	6.80	88.14
3	Edge Coupled Differential	---	100.00	+/-10	6.00	14.50	(2, 4)	6.00	99.46
5	Single Ended	---	33.00	+/-5	12.20		(4, 6)		33.20
5	Single Ended	---	38.00	+/-5	9.80		(4, 6)		38.21
5	Single Ended	---	50.00	+/-5	6.00		(4, 6)		50.32
5	Edge Coupled Differential	---	75.00	+/-7.5	8.30	4.70	(4, 6)	8.30	74.88
5	Edge Coupled Differential	---	88.00	+/-8.8	6.80	7.20	(4, 6)	6.80	88.14
5	Edge Coupled Differential	---	100.00	+/-10	6.00	14.50	(4, 6)	6.00	99.46
7	Single Ended	---	33.00	+/-5	12.20		(6, 8)		33.07
7	Single Ended	---	38.00	+/-5	9.80		(6, 8)		38.07
7	Single Ended	---	50.00	+/-5	6.00		(6, 8)		50.17

The Rework Stack-Ups (3 Similar Asia Transfers with NA DFM Rules)

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North America Design Rules: 8mil/16mil/28mil drill/back-drill/antipad
China Design Rules: 10mil/18mil/33mil drill/back-drill/antipad

Designer Re-routed all layers to transfer 3 similar PCBs to China during Christmas break 2014!!

Impedance Table

Layer	Structure Type	Coated Microstrip	Target Impedance (ohms)	Impedance Tolerance (ohms)	Target Linewidth (mils)	Proposed Linespacing (mils)	Reference Layers	Modelled Linewidth (mils)	Modelled Impedance (ohms)
1	Single Ended	Yes	33.00	+/-5	11.00		(2)		32.90
1	Single Ended	Yes	40.00	+/-5	7.90		(2)		39.90
1	Single Ended	Yes	50.00	+/-5	5.00		(2)		50.08
1	Edge Coupled Differential	Yes	75.00	+/-7.5	6.70	5.30	(2)	6.70	75.06
1	Edge Coupled Differential	Yes	88.00	+/-8.8	5.50	8.50	(2)	5.50	88.41
1	Edge Coupled Differential	Yes	100.00	+/-10	4.70	14.30	(2)	4.70	99.47
3	Single Ended	---	33.00	+/-5	12.20		(2, 4)		33.20
3	Single Ended	---	38.00	+/-5	9.80		(2, 4)		38.21
3	Single Ended	---	50.00	+/-5	6.00		(2, 4)		50.32
3	Edge Coupled Differential	---	75.00	+/-7.5	8.30	4.70	(2, 4)	8.30	74.88
3	Edge Coupled Differential	---	88.00	+/-8.8	6.80	7.20	(2, 4)	6.80	88.14
3	Edge Coupled Differential	---	100.00	+/-10	6.00	14.50	(2, 4)	6.00	99.46
5	Single Ended	---	33.00	+/-5	12.20		(4, 6)		33.20
5	Single Ended	---	38.00	+/-5	9.80		(4, 6)		38.21
5	Single Ended	---	50.00	+/-5	6.00		(4, 6)		50.32
5	Edge Coupled Differential	---	75.00	+/-7.5	8.30	4.70	(4, 6)	8.30	74.88
5	Edge Coupled Differential	---	88.00	+/-8.8	6.80	7.20	(4, 6)	6.80	88.14
5	Edge Coupled Differential	---	100.00	+/-10	6.00	14.50	(4, 6)	6.00	99.46
7	Single Ended	---	33.00	+/-5	12.20		(6, 8)		33.07
7	Single Ended	---	38.00	+/-5	9.80		(6, 8)		38.07
7	Single Ended	---	50.00	+/-5	6.00		(6, 8)		50.17
7	Edge Coupled Differential	---	75.00	+/-7.5	8.30	4.70	(6, 8)	8.30	74.72
7	Edge Coupled Differential	---	88.00	+/-8.8	6.80	7.20	(6, 8)	6.80	87.95
7	Edge Coupled Differential	---	100.00	+/-10	6.00	14.50	(6, 8)	6.00	99.19
12	Single Ended	---	33.00	+/-5	12.20		(11, 13)		33.07
12	Single Ended	---	38.00	+/-5	9.80		(11, 13)		38.07
12	Single Ended	---	50.00	+/-5	6.00		(11, 13)		50.17
12	Edge Coupled Differential	---	75.00	+/-7.5	8.30	4.70	(11, 13)	8.30	74.72
12	Edge Coupled Differential	---	88.00	+/-8.8	6.80	7.20	(11, 13)	6.80	87.95
12	Edge Coupled Differential	---	100.00	+/-10	6.00	14.50	(11, 13)	6.00	99.19
14	Single Ended	---	33.00	+/-5	12.20		(13, 15)		33.20
14	Single Ended	---	38.00	+/-5	9.80		(13, 15)		38.21
14	Single Ended	---	50.00	+/-5	6.00		(13, 15)		50.32
14	Edge Coupled Differential	---	75.00	+/-7.5	8.30	4.70	(13, 15)	8.30	74.88
14	Edge Coupled Differential	---	88.00	+/-8.8	6.80	7.20	(13, 15)	6.80	88.14
14	Edge Coupled Differential	---	100.00	+/-10	6.00	14.50	(13, 15)	6.00	99.46
16	Single Ended	---	33.00	+/-5	12.20		(15, 17)		33.13
16	Single Ended	---	38.00	+/-5	9.80		(15, 17)		38.16
16	Single Ended	---	50.00	+/-5	6.00		(15, 17)		50.35
16	Edge Coupled Differential	---	75.00	+/-7.5	8.30	4.70	(15, 17)	8.30	75.13
16	Edge Coupled Differential	---	88.00	+/-8.8	6.80	7.20	(15, 17)	6.80	88.42
16	Edge Coupled Differential	---	100.00	+/-10	6.00	14.50	(15, 17)	6.00	99.62
18	Single Ended	Yes	33.00	+/-5	11.00		(17)		32.90
18	Single Ended	Yes	40.00	+/-5	7.90		(17)		39.90
18	Single Ended	Yes	50.00	+/-5	5.00		(17)		50.08
18	Edge Coupled Differential	Yes	75.00	+/-7.5	6.70	5.30	(17)	6.70	75.06

The Money-Burner Stack-up

…is any product which is accidentally designed with DFM guidelines provided by a capable, high-tech, quick-turn prototype supplier, without knowledge of mass production limitations and requirements of increased dimensions and/or tolerances.

The following story is true, and no names are used to protect the innocent. We received permission to use these files.

Medical Mass Production Stack-up – 10L,1 Lam Through-hole

Altium

Layer	Type	CU Weight	CU %	Material Description	Via Structure	Segment	Glass Style	Material Family	Dielectric constant	Copper Plating Thickness [mil]	Thickness after lamination [mil]
Soldermask											0.80
L1	Signal	H	20			Foil				1.40	2.00 *
				Press thk = 3.82 mil		Prepreg	106(75)	IT180A	4.10		3.82
							106(75)	IT180A	4.10		
L2	Plane	H	70								0.60
				4.0 mil H/H		Core		IT180A	4.10		4.00
L3	Signal	H	20								0.60
				Press thk = 12.24 mil		Prepreg	1080(65)	IT180A	4.10		12.24
							2113(58)	IT180A	4.10		
							2113(58)	IT180A	4.10		
							2113(58)	IT180A	4.10		
L4	Signal	H	20								0.60
				4.0 mil H/1		Core		IT180A	4.10		4.00
L5	Plane	1.0	70								1.20
				Press thk = 3.28 mil		Prepreg	106(75)	IT180A	4.10		3.28
							106(75)	IT180A	4.10		
L6	Plane	1.0	70								1.20
				4.0 mil 1/H		Core		IT180A	4.10		4.00
L7	Signal	H	20								0.60
				Press thk = 12.24 mil		Prepreg	2113(58)	IT180A	4.10		12.24
							2113(58)	IT180A	4.10		
							2113(58)	IT180A	4.10		
							1080(65)	IT180A	4.10		
L8	Signal	H	20								0.60
				4.0 mil H/H		Core		IT180A	4.10		4.00
L9	Plane	H	70								0.60
				Press thk = 3.82 mil		Prepreg	106(75)	IT180A	4.10		3.82
							106(75)	IT180A	4.10		
L10	Signal	H	20			Foil				1.40	2.00 *
Soldermask											0.80

* **Estimated Cu Plating for reference use only.**

Specification (Over mask on plated copper:):	mil
Overall Board Thickness:	63.00
Tolerance:	+6.3/-6.3
Min-Max Board Thickness:	56.7-69.3

Anticipated Board Thickness:	mil
After lamination:	58.60
Over mask on plated copper::	63.00

Medical Mass Production Stack-up – 1 Lam Through-hole

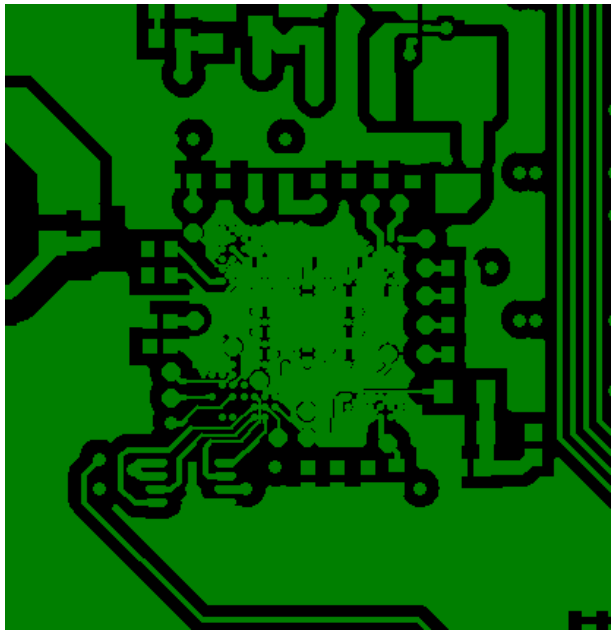
Impedance Table

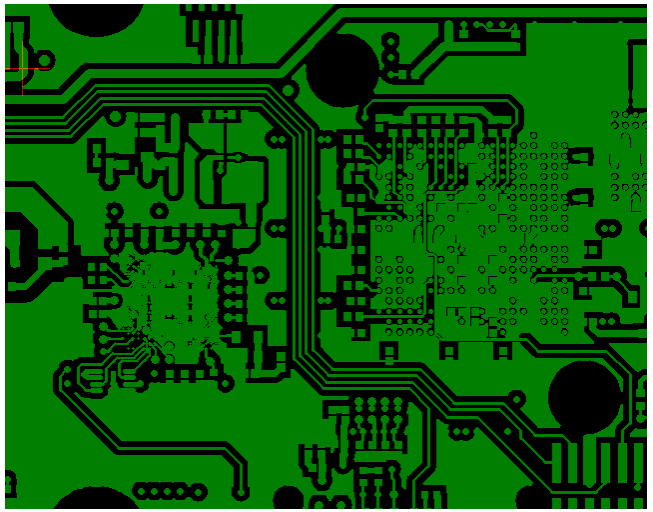
Layer	Impedance Requiremnt [ohms]	Tolerance [ohms]		Type	Upper Ref	Lower Ref	Designed Line Width [mil]	Plotted Line Width [mil]	Designed Spacing [mil]	Coplanar Spacing [mil]	Finished Line Width [mil]	Finished Spacing [mil]	Impedance Simulation [ohms]
		+	-										
L1	40	4.0	4.0	Coated microstrip SE	--	L2	9.50	10.00	--	--	9.50	--	40.3
L1	50	5.0	5.0	Coated microstrip SE	--	L2	6.00	6.50	--	--	6.00	--	50.4
L1	90	9.0	9.0	Coated microstrip Diff	--	L2	5.00	5.50	6.00	--	5.00	6.00	90.5
L1	100	10.0	10.0	Coated microstrip Diff	--	L2	4.50	5.00	8.00	--	4.50	8.00	99.9
L3	40	4.0	4.0	Single-Ended	L5	L2	8.00	9.25	--	--	8.75	--	41.0
L3	50	5.0	5.0	Single-Ended	L5	L2	6.00	6.50	--	--	6.00	--	50.1
L3	80	8.0	8.0	Differential	L5	L2	7.00	7.50	5.00	--	7.00	5.00	79.8
L3	90	9.0	9.0	Differential	L5	L2	5.50	6.00	5.50	--	5.50	5.50	90.6
L3	100	10.0	10.0	Differential	L5	L2	5.00	5.50	8.00	--	5.00	8.00	100.1
L4	40	4.0	4.0	Single-Ended	L2	L5	8.00	9.25	--	--	8.75	--	41.0
L4	50	5.0	5.0	Single-Ended	L2	L5	6.00	6.50	--	--	6.00	--	50.1
L4	90	9.0	9.0	Differential	L2	L5	5.50	6.00	5.50	--	5.50	5.50	90.6
L4	100	10.0	10.0	Differential	L2	L5	5.00	5.50	8.00	--	5.00	8.00	100.1
L7	40	4.0	4.0	Single-Ended	L9	L6	8.00	9.25	--	--	8.75	--	41.0
L7	50	5.0	5.0	Single-Ended	L9	L6	6.00	6.50	--	--	6.00	--	50.1
L7	90	9.0	9.0	Differential	L9	L6	5.50	6.00	5.50	--	5.50	5.50	90.6
L7	100	10.0	10.0	Differential	L9	L6	5.00	5.50	8.00	--	5.00	8.00	100.1
L8	40	4.0	4.0	Single-Ended	L6	L9	8.00	9.25	--	--	8.75	--	41.0
L8	50	5.0	5.0	Single-Ended	L6	L9	6.00	6.50	--	--	6.00	--	50.1
L8	90	9.0	9.0	Differential	L6	L9	5.50	6.00	5.50	--	5.50	5.50	90.6
L8	100	10.0	10.0	Differential	L6	L9	5.00	5.50	8.00	--	5.00	8.00	100.1
L10	40	4.0	4.0	Coated microstrip SE	--	L9	9.50	10.00	--	--	9.50	--	40.3
L10	50	5.0	5.0	Coated microstrip SE	--	L9	6.00	6.50	--	--	6.00	--	50.4
L10	90	9.0	9.0	Coated microstrip Diff	--	L9	5.00	5.50	6.00	--	5.00	6.00	90.5
L10	100	10.0	10.0	Coated microstrip Diff	--	L9	4.50	5.00	8.00	--	4.50	8.00	99.9

Medical Mass Production Stack-up – MAJOR COST/DFM VIOLATIONS

Went to transfer to Asia and couldn't find any takers

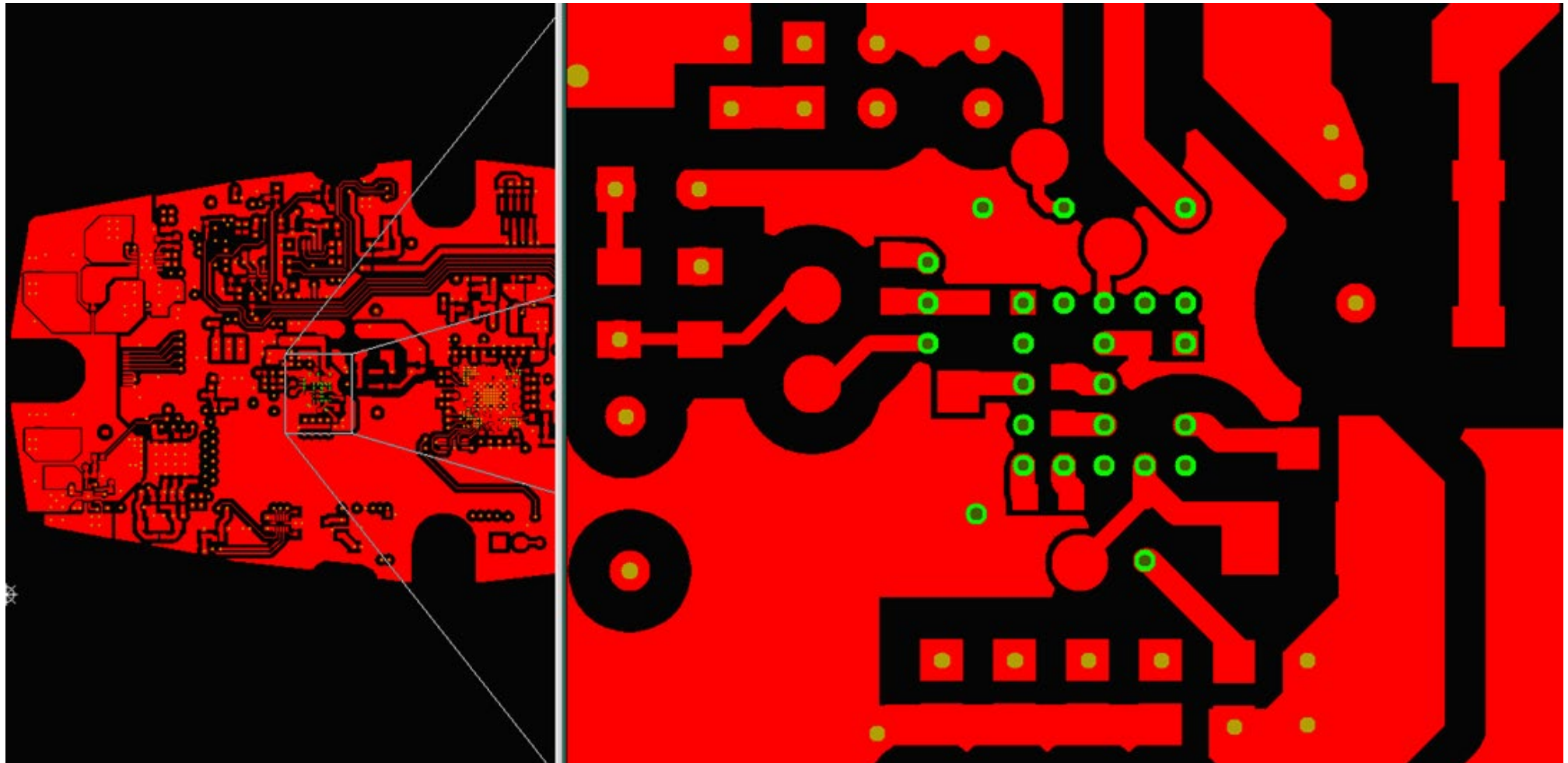
1) .063in thick, **5mil mechanically drilled through-holes** (8:1 aspect ratio <8mil drills, who drills 5mil mech drill in production???)
2) 5mil and 6mil **mechanical vias on 8, 10.24mil pads** (insufficient annular ring)
3) **2.54mil distance drill-to-Cu** (8mil min STD, 7mil ADV)
4) **2.5mil lines/spaces on Outer Layers with VIPPO**





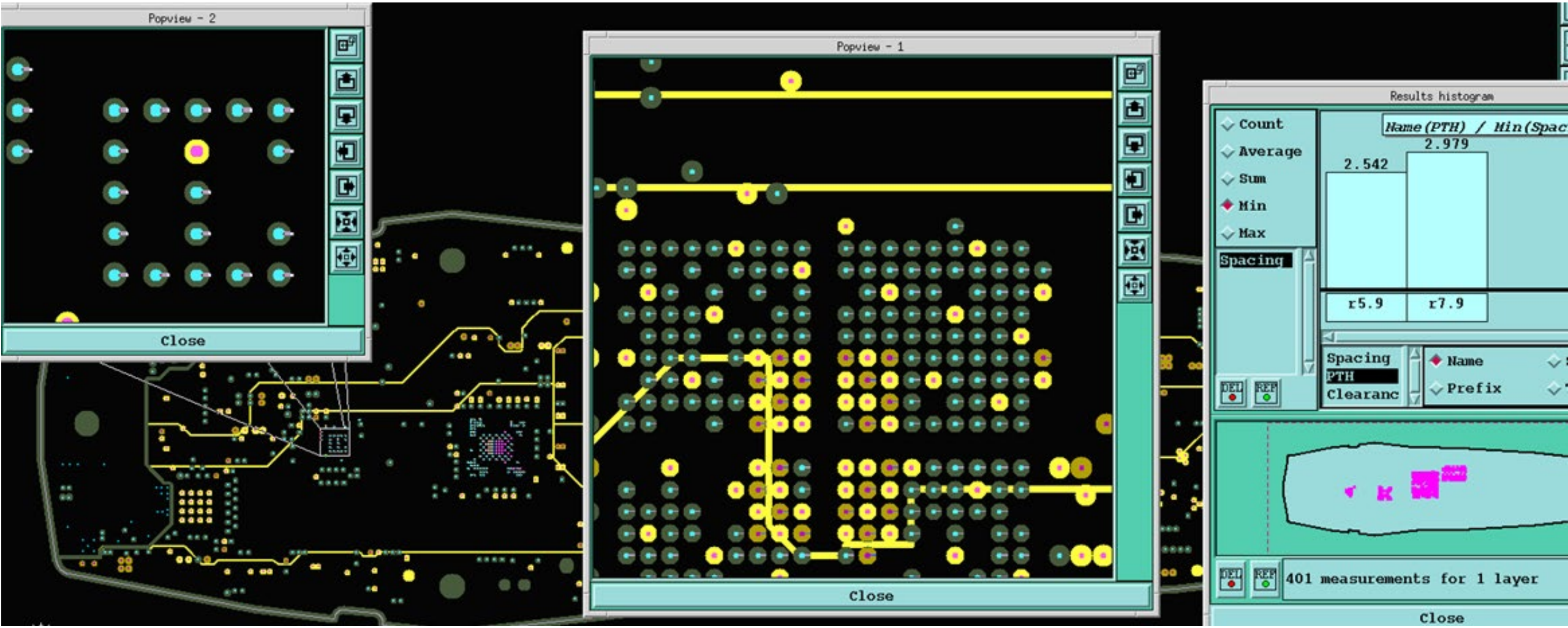
Medical Mass Production Stack-up – DFM Violation – A/R

#5 Via holes 127mil (5mil) and 150mil (5.9mil) drill with 5.9mil drill on copper pads of 5mil, 8mil, 10.236mil, 10.5mil and 10.63mil **does not give Class 2 Annular Ring** and will give break-out on all holes on all positive layer inner layers and outer layers.
There is no room to increase copper pads since design has spacing from 2.06mil to less than 3mil. (We required minimum design copper pads on all positive layers for these via are 14mil to get class 2 annular ring and avoid break-out on all layers) (As per note# 6 (c) break-outs not allowed).
Please see an Attached image and advise.



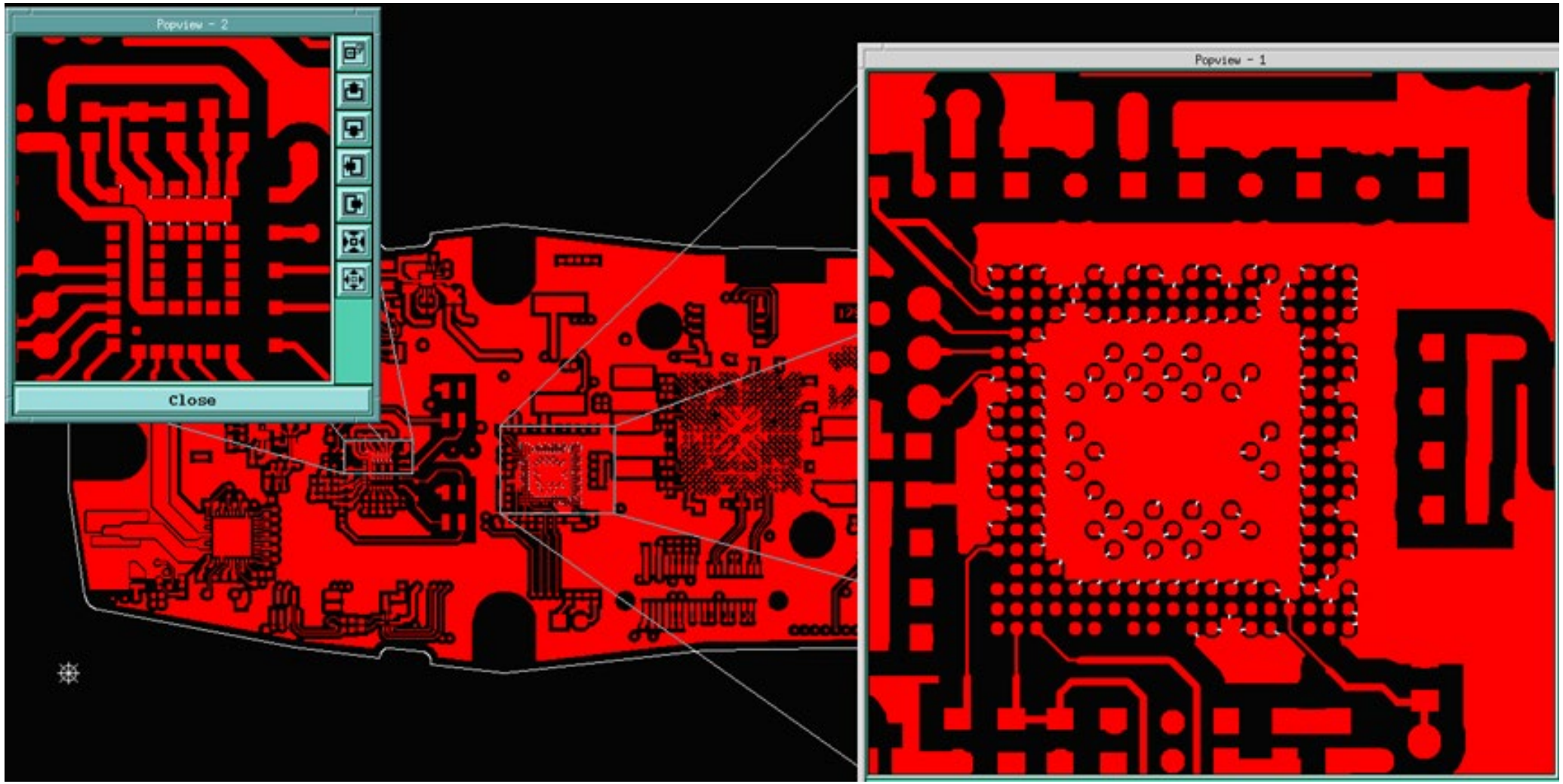
Medical Mass Production Stack-up – DFM Violation Drill-to-Cu

#8 On inner layer 2, layer 5 , layer 6 , layer 7 and layer 9 plated holes to copper (black) range from 2.542 mil to 2.9 mil for via 127mil and 150mil. (5mil and 5.9mil) We require minimum clearance Drill-to-Cu of 8mil each side (drill+16 pads).



Medical Mass Production Stack-up – O/L Space Violation

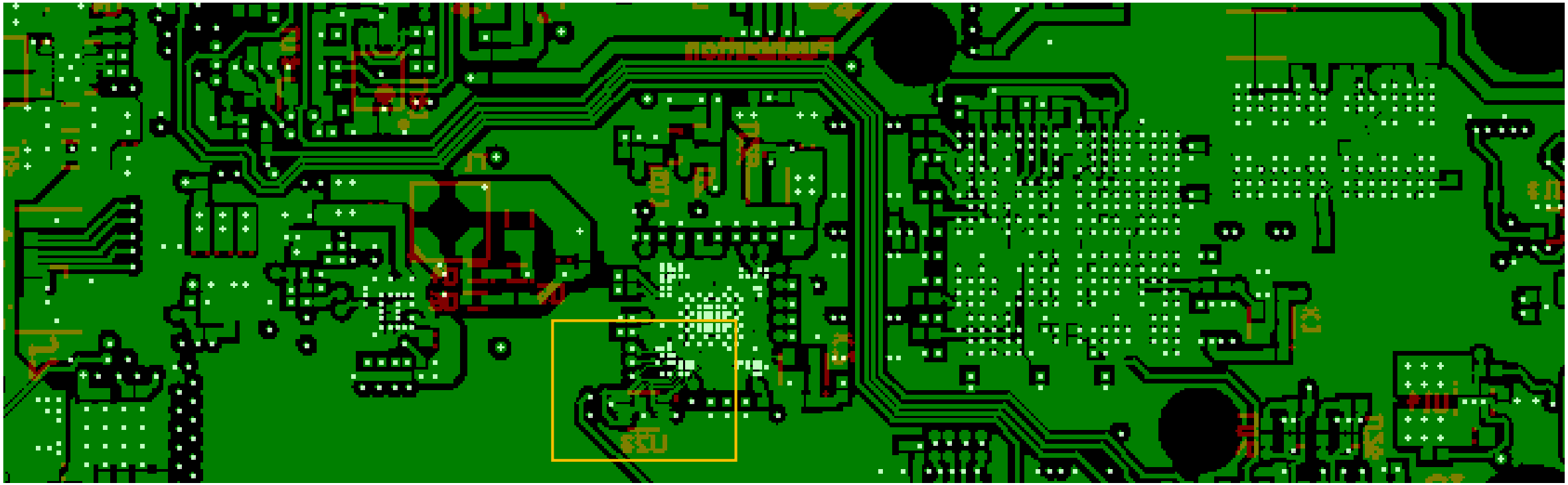
#9 On outer layer design spacing range from 2.5mil to 3mil. Since via will be epoxy fill and plated over, we have to apply minimum of 1mil etch comp. For 1mil etch comp, we require minimum 4mil design spacing between any two copper features.



Medical Mass Production Stack-up – KEY DESIGN PROBLEM

#9 On outer layer design spacing range from 2.5mil to 3mil. Since via will be epoxy fill and plated over, we have to apply minimum of 1mil etch comp. For 1mil etch comp, we require minimum 4mil design spacing between any two copper features.

Designer's Real Problem: U23 fan-out established the min trace/widths that carried through the rest of the design, but it wasn't identified in the DFM. Could he re-design to meet cost-effective guidelines?

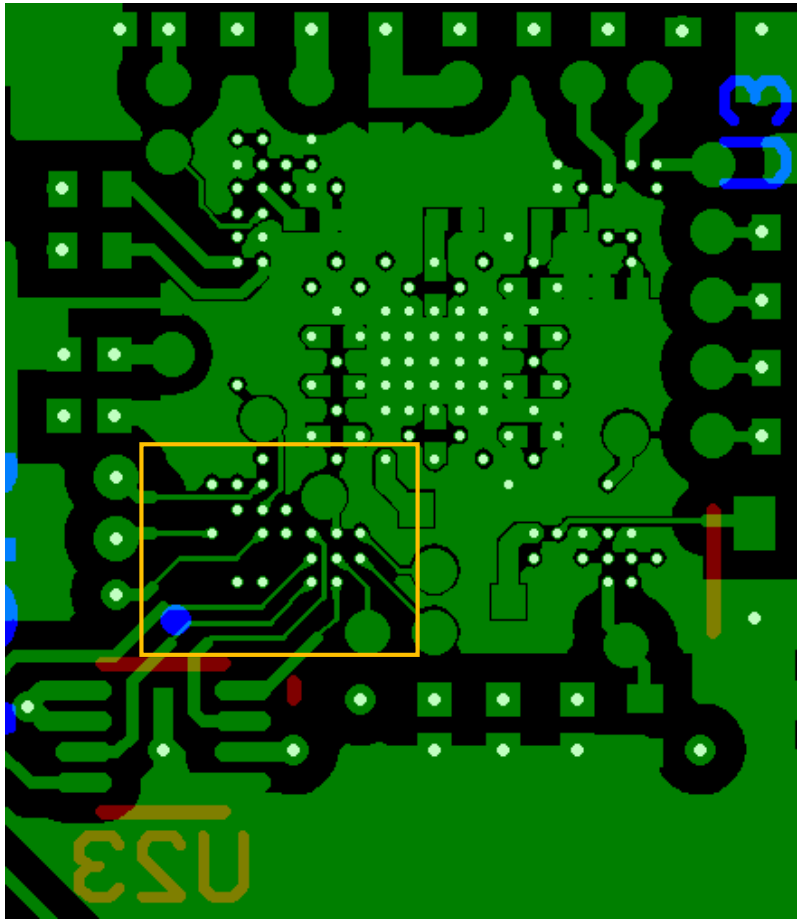


Medical Mass Production Stack-up – KEY DESIGN PROBLEM FIXED

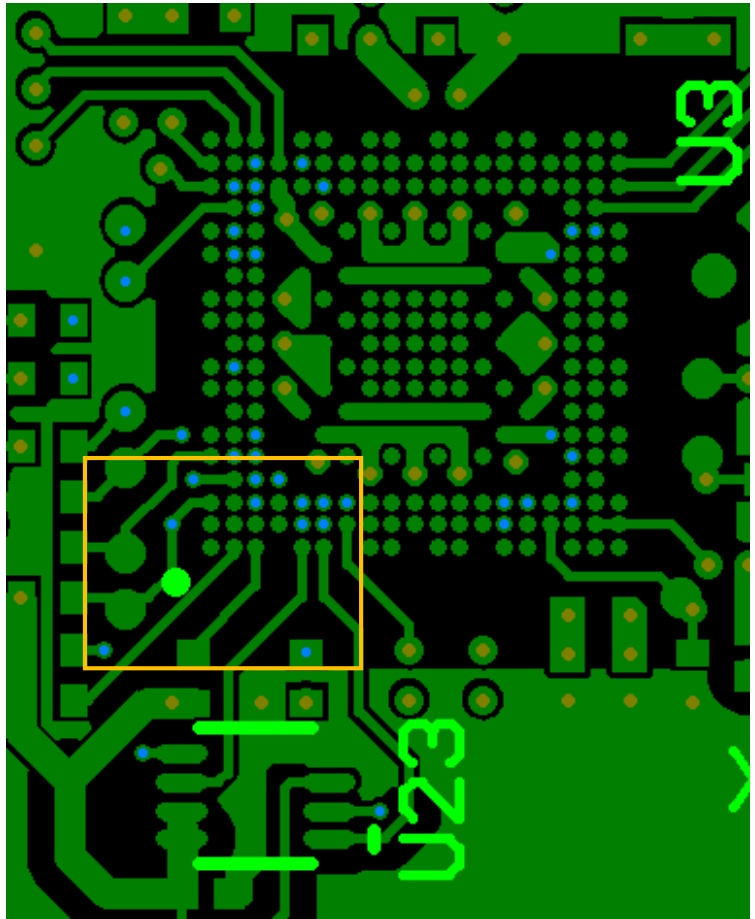
#9 On outer layer design spacing range from 2.5mil to 3mil. Since via will be epoxy fill and plated over, we have to apply minimum of 1mil etch comp. For 1mil etch comp, we require minimum 4mil design spacing between any two copper features.

Designer's FIX: U3 fan-out modified to increase lines/spaces by removing traces running between BGA pads.

Original Design had 2.5mil/2.5mil lines/spaces



Re-Design has 6mil/9.5mil lines/spaces

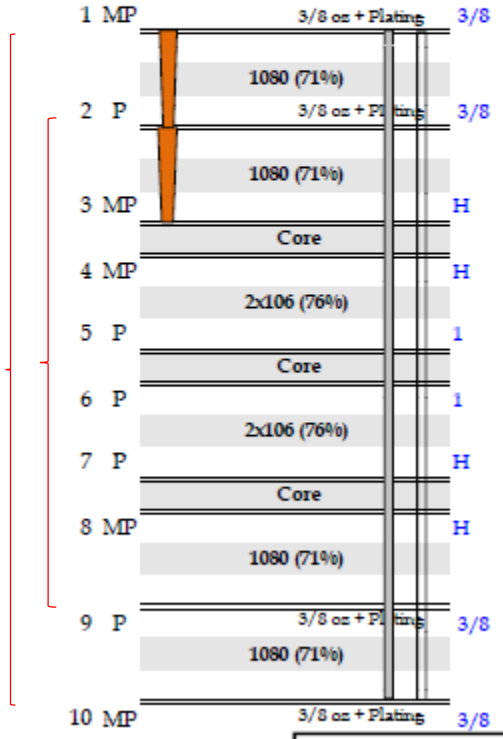


Medical Mass Production Stack-up – NEW 2 LAM STACK-UP

Replaced impossible-in-Asia 5mil/8-10mil drills/pads with 4mil uvias

Altium®

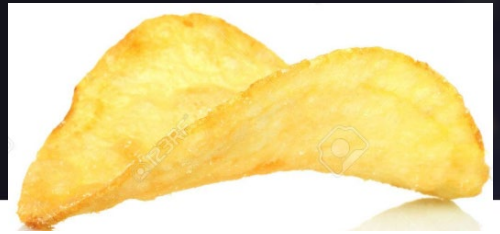
Waivers - Customer approval of stackup includes approval of:	Notes / Comments:
1: Dielectrics thickness and trace widths have been adjusted to meet target impedances.	1- Please include approved stackup with final data set. Microvias 1-2 and 2-3 to be copper filled. Through vias filled with non-conductive epoxy.



Starting Dielectric	Nominal Thick.	Tolerance	Lyr #	Single Ended Model: Org. L/W		Fin. L/W	Ref. Plane	Calc. Imp.	Lyr #	Differential Model: Org. L/W	Org. space			Fin. L/W	Fin. space	Ref. Plane	Calc. Imp.
	2.55		1	6		5.25	2	50	1	4.5	8			4	8.5	2	100
									1	5	6			4.6	6.4	2	90
=>	3.55																
	0.60																
=>	3.45																
H	0.65		3	6		5	2,5	50	3	7	5			6.3	5.7	2,5	80
=>	12.00																
H	0.65		4	6		6.2	2,5	50									
=>	4.40																
1	1.30																
=>	5.00																
1	1.30																
=>	4.45																
H	0.65																
=>	12.00																
H	0.65		8	6		4.8	7,9	50	8	5	8			4.4	8.6	7,9	100
=>	3.45																
	0.60																
=>	3.55																
									10	5	6			4.6	6.4	9	90
	2.55		10	6		5.25	9	50									

Thickness After plating	63.35	not including solder mask		Units	Mils		
Target Thickness	63+/-10%	over	All	Impedance Tolerance	(SE)	+/- 10%	(DIFF) +/- 10%

The Potato Chip Stack-up?



Board thickness:128mil+/-10%(over mask on plated copper)

Layer	Cu Thick. (mils)	Cu Foil wt (oz)	DK(2G Hz)	Lam. Thick. (mils)	Description
1	1.80	.333 oz			Foil .333 oz
			3.34	3.17	Prepreg R5670G 1078(68)
2	0.55	0.5 oz			
			3.42	3.00	Core R5775G 3.00mils 1x1078 0.5 oz / 0.5 oz HVLP
3	0.55	0.5 oz			
			3.25	4.14	Prepreg R5670G 1035(70)/1035(70)
4	0.55	0.5 oz			
			3.42	3.00	Core R5775G 3.00mils 1x1078 0.5 oz / 0.5 oz HVLP
5	0.55	0.5 oz			
			3.25	4.14	Prepreg R5670G 1035(70)/1035(70)
6	0.55	0.5 oz			
			3.42	3.00	Core R5775G 3.00mils 1x1078 0.5 oz / 0.5 oz HVLP
7	0.55	0.5 oz			
			3.25	4.14	Prepreg R5670G 1035(70)/1035(70)
8	0.55	0.5 oz			
			3.42	3.00	Core R5775G 3.00mils 1x1078 0.5 oz / 0.5 oz HVLP
9	0.55	0.5 oz			
			3.25	4.14	Prepreg R5670G 1035(70)/1035(70)
10	0.55	0.5 oz			
			3.42	3.00	Core R5775G 3.00mils 1x1078 0.5 oz / 0.5 oz HVLP
11	0.55	0.5 oz			
			3.25	4.25	Prepreg R5670G 1035(70)/1035(70)
12	0.55	0.5 oz			
			3.58	2.60	Core R5775G 2.60mils 1x1080 0.5 oz / 0.5 oz HVLP
13	0.55	0.5 oz			
			3.34	3.06	Prepreg R5670G 1078(68)
14	0.55	0.5 oz			
			3.58	2.60	Core R5775G 2.60mils 1x1080 0.5 oz / 0.5 oz HVLP
15	0.55	0.5 oz			
			3.34	3.28	Prepreg R5670G 1078(68)
16	1.00	.333 oz			Foil .333 oz
			3.40	5.20	Prepreg R5670G 1080(64)/1080(64)
17	1.00	.333 oz			Foil .333 oz
			3.34	3.28	Prepreg R5670G 1078(68)
18	0.55	0.5 oz			
			3.58	2.60	Core R5775G 2.60mils 1x1080 0.5 oz / 0.5 oz HVLP
19	0.55	0.5 oz			
			3.34	3.06	Prepreg R5670G 1078(68)
20	0.55	0.5 oz			
			3.58	2.60	Core R5775G 2.60mils 1x1080 0.5 oz / 0.5 oz HVLP
21	0.55	0.5 oz			
			3.25	4.25	Prepreg R5670G 1035(70)/1035(70)
22	0.55	0.5 oz			
			3.42	3.00	Core R5775G 3.00mils 1x1078 0.5 oz / 0.5 oz HVLP
23	0.55	0.5 oz			
			3.25	4.14	Prepreg R5670G 1035(70)/1035(70)
24	0.55	0.5 oz			
			3.42	3.00	Core R5775G 3.00mils 1x1078 0.5 oz / 0.5 oz HVLP
25	0.55	0.5 oz			
			3.25	4.14	Prepreg R5670G 1035(70)/1035(70)
26	0.55	0.5 oz			
			3.42	3.00	Core R5775G 3.00mils 1x1078 0.5 oz / 0.5 oz HVLP
27	0.55	0.5 oz			
			3.25	4.14	Prepreg R5670G 1035(70)/1035(70)
28	0.55	0.5 oz			
			3.42	3.00	Core R5775G 3.00mils 1x1078 0.5 oz / 0.5 oz HVLP
29	0.55	0.5 oz			
			3.25	4.14	Prepreg R5670G 1035(70)/1035(70)
30	0.55	0.5 oz			
			3.42	3.00	Core R5775G 3.00mils 1x1078 0.5 oz / 0.5 oz HVLP
31	0.55	0.5 oz			
			3.34	3.17	Prepreg R5670G 1078(68)
32	1.80	.333 oz			Foil .333 oz

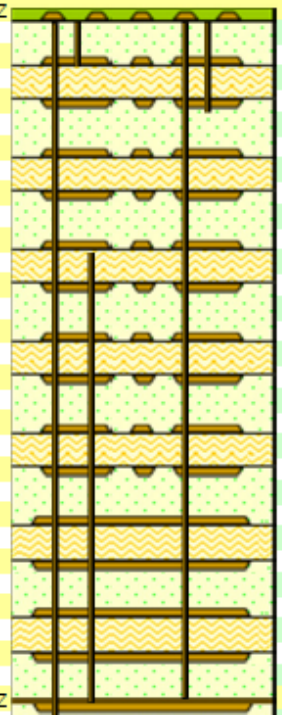
Designer wants to use one half of the left stack-up for a complete 16L board and maintain much of the design. This will set the precedence for multiple, long life-cycle products. Is the stack-up below feasible?

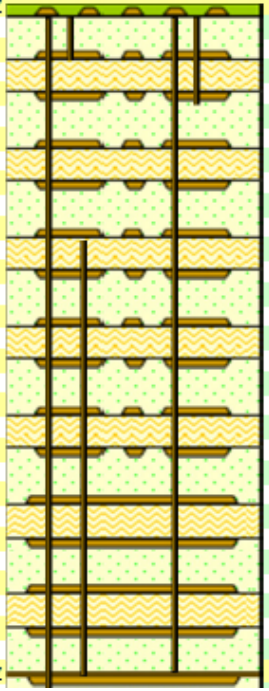
Layer	Cu Thick. (mils)	Cu Foil wt (oz)	DK(2G Hz)	Lam. Thick. (mils)	Description
1	1.80	.333 oz			Foil .333 oz
			3.34	3.17	Prepreg R5670G 1078(68)
2	0.55	0.5 oz			
			3.42	3.00	Core R5775G 3.00mils 1x1078 0.5 oz / 0.5 oz HVLP
3	0.55	0.5 oz			
			3.25	4.14	Prepreg R5670G 1035(70)/1035(70)
4	0.55	0.5 oz			
			3.42	3.00	Core R5775G 3.00mils 1x1078 0.5 oz / 0.5 oz HVLP
5	0.55	0.5 oz			
			3.25	4.14	Prepreg R5670G 1035(70)/1035(70)
6	0.55	0.5 oz			
			3.42	3.00	Core R5775G 3.00mils 1x1078 0.5 oz / 0.5 oz HVLP
7	0.55	0.5 oz			
			3.25	4.14	Prepreg R5670G 1035(70)/1035(70)
8	0.55	0.5 oz			
			3.42	3.00	Core R5775G 3.00mils 1x1078 0.5 oz / 0.5 oz HVLP
9	0.55	0.5 oz			
			3.25	4.14	Prepreg R5670G 1035(70)/1035(70)
10	0.55	0.5 oz			
			3.42	3.00	Core R5775G 3.00mils 1x1078 0.5 oz / 0.5 oz HVLP
11	0.55	0.5 oz			
			3.25	4.25	Prepreg R5670G 1035(70)/1035(70)
12	0.55	0.5 oz			
			3.58	2.60	Core R5775G 2.60mils 1x1080 0.5 oz / 0.5 oz HVLP
13	0.55	0.5 oz			
			3.34	3.06	Prepreg R5670G 1078(68)
14	0.55	0.5 oz			
			3.58	2.60	Core R5775G 2.60mils 1x1080 0.5 oz / 0.5 oz HVLP
15	0.55	0.5 oz			
			3.34	3.28	Prepreg R5670G 1078(68)
16	1.00	.333 oz			Foil .333 oz

The Potato Chip Stack-up?

Designer thinks they can use one half of the left stack-up for a complete 16L board and maintain much of the design. This Will set the precedence for multiple, long life-cycle products. Is the stack-up below feasible?

Layer	Cu Thick. (mils)	Cu Foil wt (oz)	DK(2G Hz)	Lam. Thick. (mils)	Description
1	1.80	.333 oz			Foil .333 oz
			3.34	3.17	Prepreg R5670G 1078(68)
2	0.55	0.5 oz			
			3.42	3.00	Core R5775G 3.00mils 1x1078 0.5 oz / 0.5 oz HVLP
3	0.55	0.5 oz			
			3.25	4.14	Prepreg R5670G 1035(70)/1035(70)
4	0.55	0.5 oz			
			3.42	3.00	Core R5775G 3.00mils 1x1078 0.5 oz / 0.5 oz HVLP
5	0.55	0.5 oz			
			3.25	4.14	Prepreg R5670G 1035(70)/1035(70)
6	0.55	0.5 oz			
			3.42	3.00	Core R5775G 3.00mils 1x1078 0.5 oz / 0.5 oz HVLP
7	0.55	0.5 oz			
			3.25	4.14	Prepreg R5670G 1035(70)/1035(70)
8	0.55	0.5 oz			
			3.42	3.00	Core R5775G 3.00mils 1x1078 0.5 oz / 0.5 oz HVLP
9	0.55	0.5 oz			
			3.25	4.25	Prepreg R5670G 1035(70)/1035(70)
10	0.55	0.5 oz			
			3.58	2.60	Core R5775G 2.60mils 1x1080 0.5 oz / 0.5 oz HVLP
11	0.55	0.5 oz			
			3.34	3.06	Prepreg R5670G 1078(68)
12	0.55	0.5 oz			
			3.58	2.60	Core R5775G 2.60mils 1x1080 0.5 oz / 0.5 oz HVLP
13	0.55	0.5 oz			
			3.34	3.28	Prepreg R5670G 1078(68)
14	0.55	0.5 oz			
15	0.55	0.5 oz			
16	1.00	.333 oz			Foil .333 oz





Layer	Cu Thick. (mils)	Cu Foil wt (oz)	DK(2G Hz)	Lam. Thick. (mils)	Description
1	1.80	.333 oz			Foil .333 oz
			3.34	3.17	Prepreg R5670G 1078(68)
2	0.55	0.5 oz			
			3.42	3.00	Core R5775G 3.00mils 1x1078 0.5 oz / 0.5 oz HVLP
3	0.55	0.5 oz			
			3.25	4.14	Prepreg R5670G 1035(70)/1035(70)
4	0.55	0.5 oz			
			3.42	3.00	Core R5775G 3.00mils 1x1078 0.5 oz / 0.5 oz HVLP
5	0.55	0.5 oz			
			3.25	4.14	Prepreg R5670G 1035(70)/1035(70)
6	0.55	0.5 oz			
			3.42	3.00	Core R5775G 3.00mils 1x1078 0.5 oz / 0.5 oz HVLP
7	0.55	0.5 oz			
			3.25	4.14	Prepreg R5670G 1035(70)/1035(70)
8	0.55	0.5 oz			
			3.42	3.00	Core R5775G 3.00mils 1x1078 0.5 oz / 0.5 oz HVLP
9	0.55	0.5 oz			
			3.25	4.14	Prepreg R5670G 1035(70)/1035(70)
10	0.55	0.5 oz			
			3.42	3.00	Core R5775G 3.00mils 1x1078 0.5 oz / 0.5 oz HVLP
11	0.55	0.5 oz			
			3.25	4.14	Prepreg R5670G 1035(70)/1035(70)
12	0.55	0.5 oz			
			3.58	3.00	Core R5775G 3.00mils 1x1078 0.5 oz / 0.5 oz HVLP
13	0.55	0.5 oz			
			3.34	4.14	Prepreg R5670G 1035(70)/1035(70)
14	0.55	0.5 oz			
			3.58	3.00	Core R5775G 3.00mils 1x1078 0.5 oz / 0.5 oz HVLP
15	0.55	0.5 oz			
			3.34	3.28	Prepreg R5670G 1078(68)
16	1.00	.333 oz			Foil .333 oz

ANSWER: Yes, if the stack-up can be made symmetric by Matching Layers 11 – 15 to Layers 2 – 6.

4.14	Prepreg R5670G 1035(70)/1035(70)
3.00	Core R5775G 3.00mils 1x1078 0.5 oz / 0.5 oz HVLP
4.14	Prepreg R5670G 1035(70)/1035(70)
3.00	Core R5775G 3.00mils 1x1078 0.5 oz / 0.5 oz HVLP

PCB Layer Stack-Up Agenda

1. Introduction – Why learn about PCB Stack-Ups?
2. **PCB Layer Stack-Up Physics**
3. Communicating About Stack-Ups and What Do You Ask?
4. Tools and Processes
5. Altium Designer 19 Implementation Examples

How do we mitigate these problems?

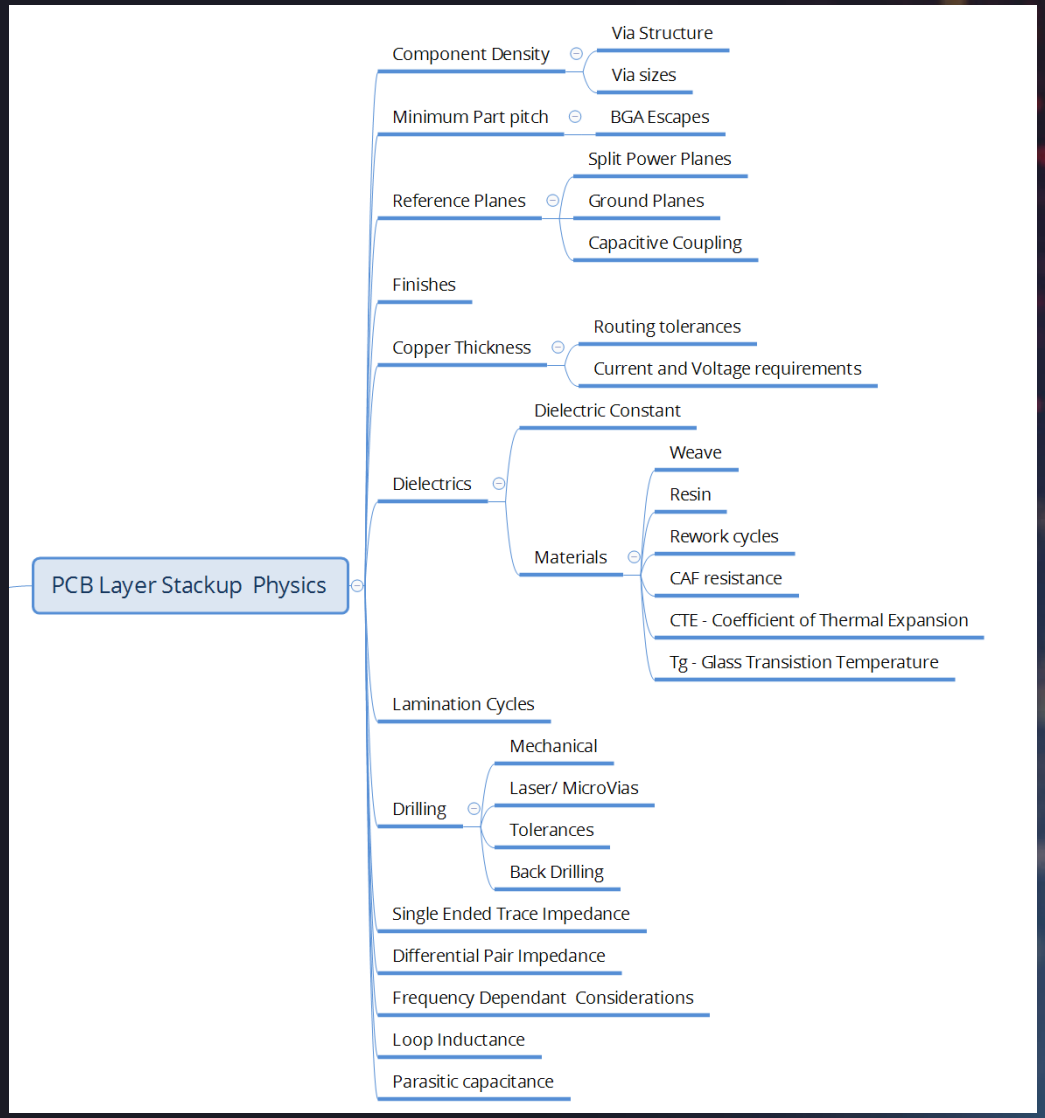
With understanding of PCB Board Level Physics!

PCB Board Physics
– Making our Electro-Mechanical Choices

-Conductors

-Dielectrics

-Process



Begin with the end in mind

3 stage process:

1)Put the physical requirements in the design

2)Communicate clear intent

3) Create the documentation

PCB Layer Stack-Up Agenda

1. Introduction – Why learn about PCB Stack-Ups?
2. PCB Layer Stack-Up Physics
3. **Design Considerations and Communication**
4. Tools and Processes
5. Altium Designer 19 Implementation Examples

“Can you please send your design guidelines?”

22 fab sites = 22 similar, not exactly the same, DFM guidelines

A&D

Aerospace & Defense

1. Denver - DEN
2. North Jackson - NJ
3. Stafford - ST
4. Stafford Springs - SS
5. Sterling - STE

Specialty

6. Anaheim - ANA
7. Forest Grove - FG
8. Santa Ana - SA
9. Santa Clara - SC
10. San Diego - SD

AMI&I

Automotive

11. Zhongshan - ZS
12. Guangzhou - GZ

Medical, Ind, Inst

13. Huiyang - HY
14. Logan - LG
15. San Jose - SJ
16. Toronto - TOR

C&C

Mobility

17. Guangzhou - GME
    Guangzhou - FPC
18. Shanghai - SME
19. Shanghai - SP

Communications

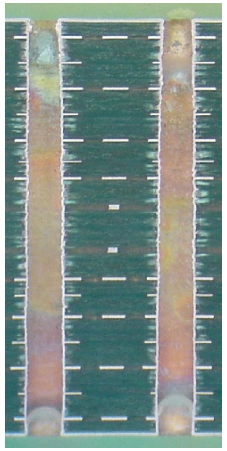
20. Hong Kong - OPCM
21. Chippewa Falls - CF
22. Dongguan - DMC

E-MS

E-M Solutions

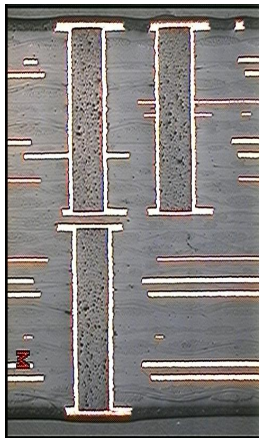
23. Shanghai - SH
24. Shanghai - SH E-MS
25. Shenzhen - SZ

What is your Technology Requirement?



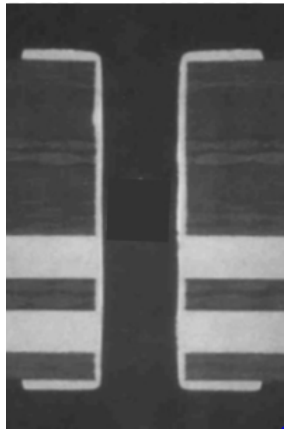
Single Lamination Mech Drills

- Conventional Through Hole
- >0.65mm BGA
- Min .008” drill
- 4mil line/space
- 10:1 aspect ratio



Multiple Lam Mech Drills

- Blind vias
- Buried vias
- Through Hole
- Min .008” drill
- 10:1 Aspect Ratio
- Lamination cycles= press+drill+plate
- Significant cost

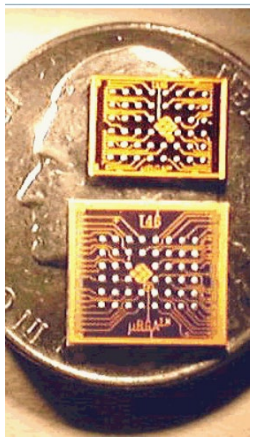


Heavy Copper

- > 2oz. Cu foil
- Up to 12 oz. Inner Layers
- High Voltage/Amps
- Single or multiple lam
- Increased lines/spaces for etch capability
- Special-order material
- Increases cost & lead time

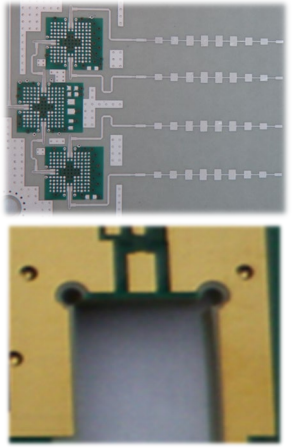
Standard HDI > 0.4mm BGA

- 4mil laser uvias
- 10mil pads
- Offset uvias
- 3mil min lines
- 1 or more lams
- Offset uvias
- Stacked uvias



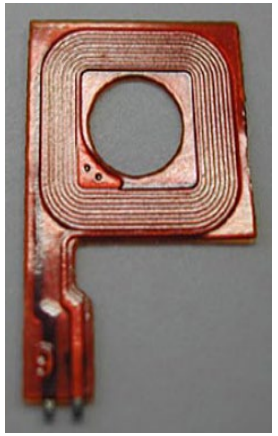
Micro HDI ≤ 0.4mm BGA

- 3-4mil laser uvias
- 8.8mil pads
- 2.36mil lines/spaces
- Stacked uvias
- Multiple lam cycles
- CONTACT TTM



RF & Microwave

- Advanced materials
- Cavities
- Horizontal Launch
- Filters , antennas
- Controlled etch
- Hybrid stack-ups
- Multiple lam cycles
- CONTACT TTM



Flex

Rigid-Flex

What is your Design-for-Final-Volume Plan?

Do we need Seamless Global Transfer?

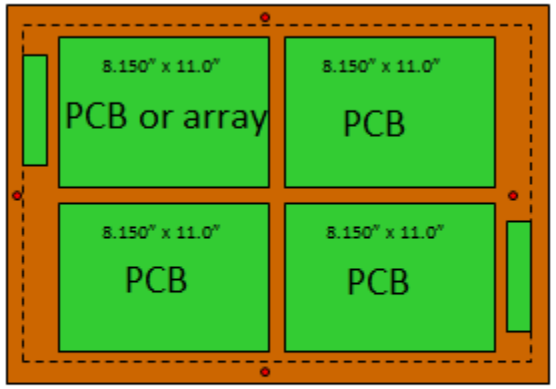
Design For Volume (DFV)

- Plan ahead for “Seamless Global Transfer, if necessary”
- What are proto quantities, lead time?
- Where will prototypes be built?
- Where is final production site?
  - Technology required
  - Volumes
- Which site builds long-term reliability testing units?
- Are minor changes occur between prototypes and final production units allowed?
  - Materials, glass styles, resin %
  - Plated layers final Cu thickness
  - Linewidths adjusted to meet controlled impedance requirements
- **Design for Volume, DFV: Use Design Guidelines and Stack-up from Final Production Site and duplicate them at your prototype site to achieve “Seamless Global Transfer”**

PCB Technology Requirements and Cost Factors

1) **Manufacturing Panel Utilization** (how many PCBs fit on the master panel)
2) **Performance Class** (IPC-6012D Class 2, 3, A, S, or MIL-PRF-55110/31032, IPC-6013 (Flex, rigid-flex), IPC-6018 (RF))
3) **Layer Count** (total number of required cores) #cores = (#Layers-2)/2
4) **Type of dielectric Material** (Standard, mid-loss, low-loss, Teflon, polyimide/flex, lead time, processing complications)
5) **Number of Lamination Cycles** – each cycle requires lam/drill/plate/etch *est.+25% per lam cycle*
6) **Via Protection –** consider if solder will flow down via holes in a soldered thermal pad, or adjacent to a soldered pad
7) **HDI** (via-in-pad, multiple lam cycles, **requires enabling equipment**)
8) **Design Complexity** - **STANDARD (green), ADVANCED (yellow),** or **Engineering (red)** capability
   - ***Line Widths and Feature Spacing***
     - *4/4mil STD, 3/3mil +23-30%, 2.5/2/5mil +50%* ***require LDI***
   - ***Controlled Impedance (CI) requirement & tolerance***
     - *10%CI STD, 7%CI +20%, 5%CI +30% (if process-capable)*
   - ***Drilled Hole Size*** *(**Aspect Ratio** = PCB Thickness: Drill Diameter)*
     - *25K drills/panel STD, extra 10K +1-2%, +15-20%*
     - ***Laser drilled microvias***
       - ***Requires special plating process***
   - ***Overall PCB Thickness*** *(Equipment Limitations)/ Aspect Ratios*
     - *<10:1 STD, 10-11.99:1 +10-15%, 12-12.99:1 +20-25%*
   - ***Annular Ring Requirements vs Design*** *(Registration Capabilities)*
   - ***Copper Weights*** *(Cost, Availability, and impact on Etching)*

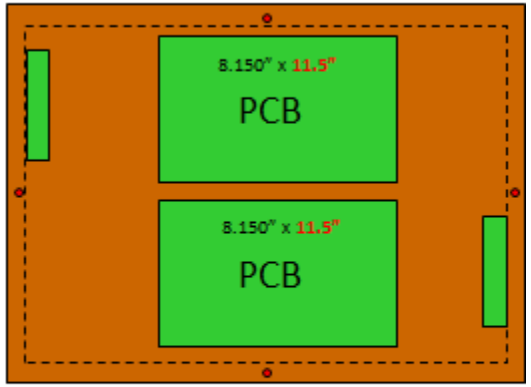
Excellent Panel Utilization



Total usable area 371 in² total
Circuit area (including assembly rails) 300 in²
81% panel utilization

Add 0.5" rails to the long sides, and we reduce the panel to 2-up

Poor Panel Utilization



Total usable area 371 in² total
Circuit area (including assembly rails) 187 in²
50% panel utilization

PCB COST = 2X

9) **Special requirements** (routed cavities, castellations, edge plating, controlled depth drill, back-drill, solder mask plugged vias, or VIPPO)
10) **Process Yield** (often a **Hidden Cost** based on DFM violations!)

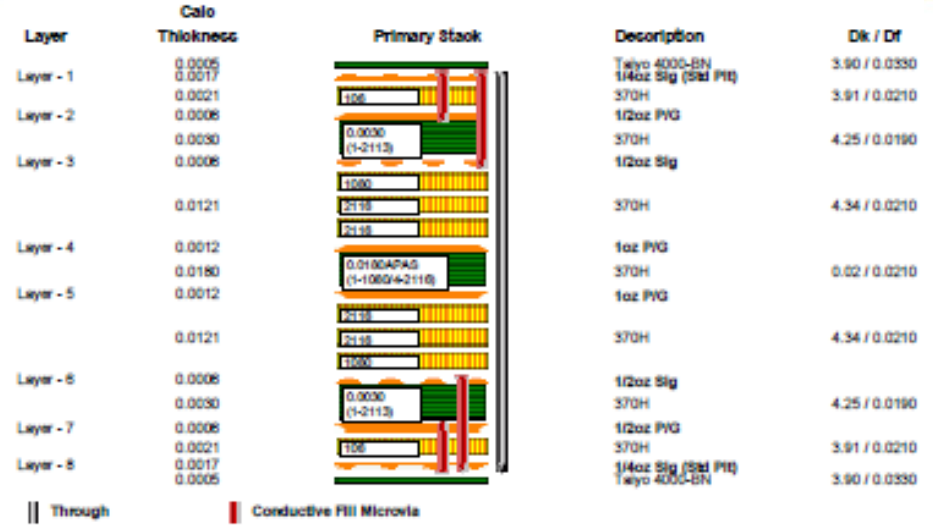
What should you provide to your fabricator for a Stack-up?

- ❑ **Top Level Specification/s** (ITAR, MIL-PRF-55110/31032, IPC-6012 Class 2/3, A/S, 6013 (Flex), 6018 (RF))
- ❑ **Location of final production site** (ITAR stays in North America, otherwise Design for Volume, DFV)
- ❑ **Material**
- ❑ **Overall thickness (tol +/-10%)**
- ❑ **# of Layers**
  - ❑ Cu thickness per layer
  - ❑ Signal, Plane (PWR/GND), or Mixed assignment for each layer
  - ❑ Controlled impedance requirements per layer
  - ❑ **Min lines/spaces** when <3.7mil
  - ❑ Estimated dielectric thicknesses, when required (High V, similar thicknesses between all layers, etc.)
- ❑ **Minimum pitch of BGA**
  - ❑ Calculate min line/spaces to route between pads
  - ❑ Calculate min drill/pad diameters for fan-out that can be fabricated at Final Fab Site
- ❑ **Drill structures**
  - ❑ Through-hole (standard aspect ratio </= 10: 1 for >8mil drills in Asia)
  - ❑ Via-in-pad-plated-over (VIPPO, non-conductive filled via with Cu cap plating)
  - ❑ Laser uvias (aspect ratio <0.8: 1)
    - ❑ off-set or stacked (buried stacked uvias should be solid Cu-filled)
    - ❑ Skip blind vias
  - ❑ Back-drills (specify Starting and Do-Not-Cut layers)
- ❑ **Special requirements** (Cavities, < +/-5mil tol Routing, Solder mask-defined pads, Castellations, Edge-plating, etc.)

Red highlights indicate capabilities that are affected by plating surfaces.

Checklist of Information Fabricator Should Verify to You

- ❑ **Stack-up with controlled impedance table, when necessary**
- ❑ **Material**
- ❑ **Overall thickness (tol +/-10%)**
- ❑ **Number of lamination cycles (adds cost)**
- ❑ **Layers**
  - ❑ #
  - ❑ Cu thickness per layer
  - ❑ Signal, Plane (PWR/GND), or Mixed assignment for each layer
  - ❑ Controlled impedance requirements per layer
- ❑ **Minimum lines/spaces allowed**
  - ❑ Internal layers, etch only
  - ❑ Plated layers, whether internal or external
- ❑ **Drill structures**
  - ❑ Min drill/pads/antipads for all layers
  - ❑ Verification of VIPPO
  - ❑ Confirm Laser uvias
    - ❑ off-set or stacked (buried stacked uvias should be solid Cu-filled)
    - ❑ Skip blind vias
  - ❑ Back-drills (confirming Starting and Do-Not-Cut layers, drill/antipad diameter)
- ❑ **Any Special dimensional requirements affecting routing, drilling, and lamination**



Requirement	Req. Thickness	Tol +	Tol -	Calc Thick
Incl. Plating & Mask	0.0620	0.0062	0.0062	0.0618
Incl. Mask over Laminate	0.0588	0.0059	0.0059	0.0582
Incl. Plating	0.0610	0.0061	0.0061	0.0608
After Lamination	0.0582	0.0029	0.0029	0.0578
Over Laminate	0.0578	0.0058	0.0058	0.0572

	Impedance Type	Layer	Design	Actual	Pitch	Plane	Target	Tol (ohms)	Predict
1	Stripline	L3	-	0.00575	-	L2	40	4.0	40.06
		-	-	-	-	L4			
2	Stripline	L3	-	0.00375	-	L2	50	5.0	50.06
		-	-	-	-	L4			
3	EC Stripline	L3	0.0040	0.0045	0.0085	L2	80	8.0	79.80
		-	0.0040	0.0045	-	L4			
4	EC Stripline	L3	-	0.0035	0.0140	L2	100	10.0	100.51
		-	-	0.0035	-	L4			

What Documentation should you provide for fabrication?

Altium

Required:

1. Gerber Files (RS-274-X or RS-274-D format)
   - All copper layers (including inner and outer layers)
   - Solder mask layers
   - Silkscreen/Legend layers
   - Via plugging layers (if applicable)
   - Solder paste layers (for board assembly)
   - Aperture list if apertures are not embedded in the Gerber data (i.e. not using RS-274-X)
2. Drill file with tool codes and X-Y coordinates for all holes (ASCII or EIA format).
3. IPC-D-356 netlist (used for continuity testing).
4. Readme File containing Engineering contact information and any special instructions.
5. Fab drawing
   - Board outline, dimensions, including cutouts, chamfers, radii, bevels, scores, etc.
   - Dimensions from a reference hole in the board to a corner or to two sides of the board outline.
   - A drill chart with the hole symbols on the drawing and the finished hole sizes
   - Material requirements
   - Finished board thickness and tolerance
   - Layer stack-up order
   - Controlled impedance requirements (if applicable)
   - Dimensioned array drawing if the design is to be shipped as a multiple-up array
   - Notes defining any other requirements or specifications pertinent to the design

Optional:

1. Valor ODB++ file - preferred by PCB vendors instead of Gerber format.
2. Check plots in Adobe PDF form. Incoming QC uses this to check PCB.
3. IPC 2581 file **WITH A PDF FAB DRAWING for non-2581 users to view***

*

Buyers
FAEs
Inspectors (PCB, R/I)
CAM Techs
PMs
Customer Service
Process Engineers
Fab
Assembly

PCB Layer Stack-Up Agenda

1. Introduction – Why learn about PCB Stack-Ups?
2. PCB Layer Stack-Up Physics
3. Design Considerations and Communication
4. **Tools and Processes**
5. Altium Designer 19 Implementation Examples

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Any Questions?