



Altium®

ALTUMLIVE 2018:
UNLEASH THE POWER AND POTENTIAL
OF ALTIUM'S DESIGN RULE
CAPABILITIES

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DRC syntax can be intimidating

Altium[®]

Dictionary definition

syn·tax

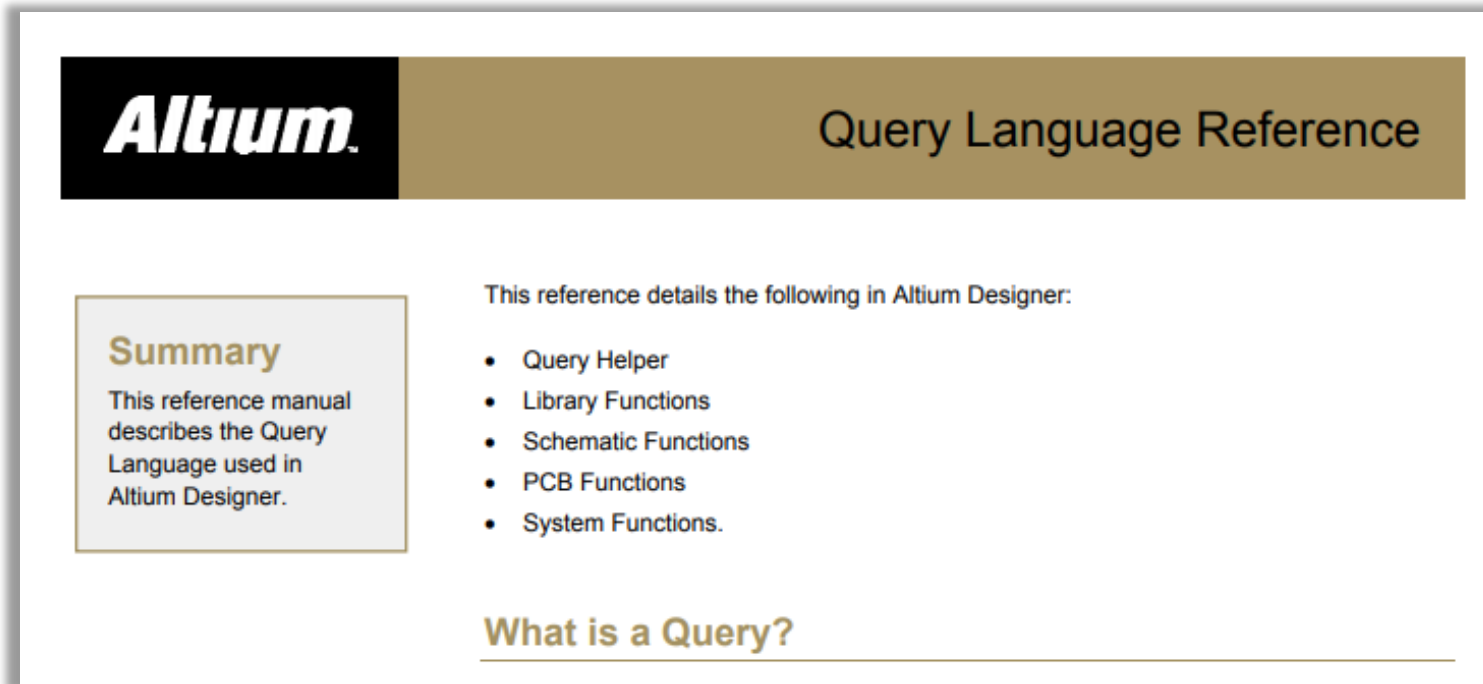
/sin ,taks/

noun

**a set of rules for or an analysis of
this.**

You can turn to Altium's Query Language Reference!

<http://valhalla.altium.com/Learning-Guides/TR0110%20Query%20Language%20Reference.pdf>



The screenshot shows the top portion of a document titled "Query Language Reference". On the left is the Altium logo. The main title "Query Language Reference" is centered at the top. Below the title, there is a "Summary" section in a light gray box, followed by a bulleted list of topics covered in the reference, and a section titled "What is a Query?".

Altium Query Language Reference

Summary
This reference manual describes the Query Language used in Altium Designer.

This reference details the following in Altium Designer:

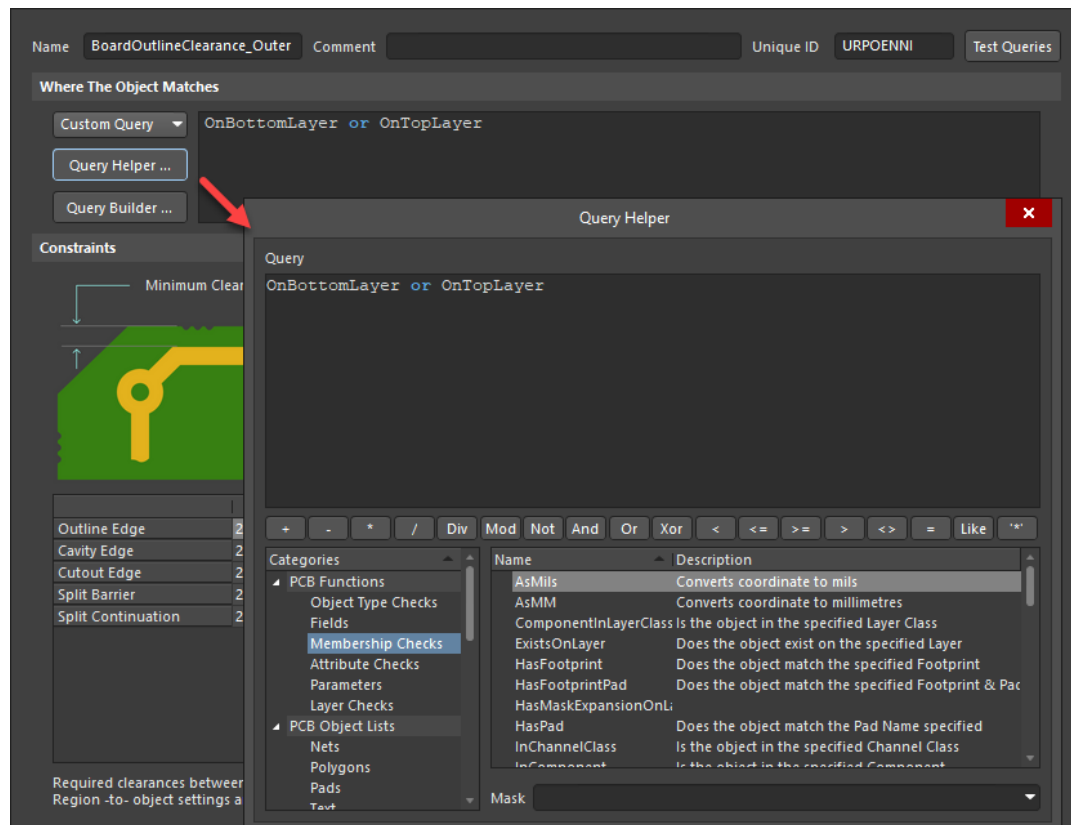
- Query Helper
- Library Functions
- Schematic Functions
- PCB Functions
- System Functions.

What is a Query?

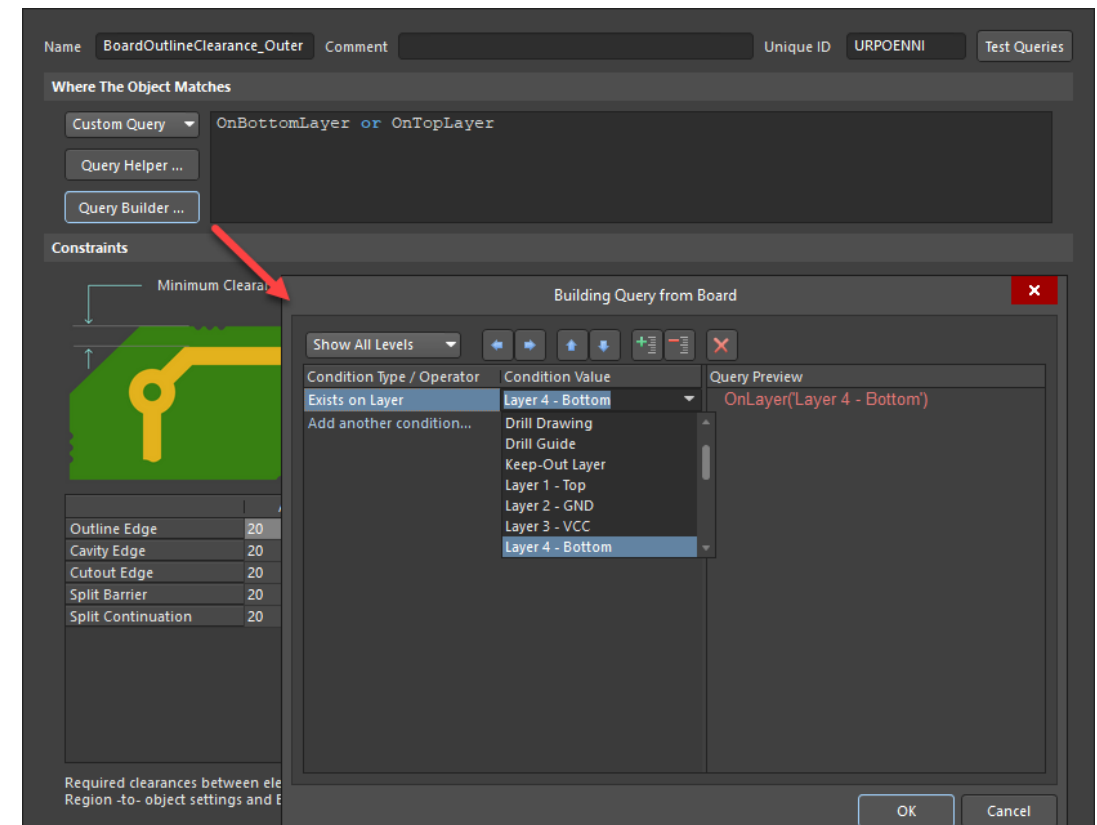
349 pages of detailed syntax information! Umm...maybe not.

Fortunately Altium has automated the syntax entry...

...with Query Helper



...and Query Builder



Let's start with something easy...

...how about a rule for board outline clearance?

This will also set the polygon back-off from the edge of the PCB.

The screenshot shows the 'PCB Rules and Constraints Editor [mil]' window. The left pane shows a tree view with 'Board Outline Clearance' expanded to 'BoardOutlineClearance_Outer'. The right pane shows the rule configuration for 'BoardOutlineClearance_Outer'.

Name: BoardOutlineClearance_Outer
Comment:
Unique ID: URPOENNI
Test Queries:
Where The Object Matches: Custom Query: OnBottomLayer or OnTopLayer
Constraints: Minimum Clearance: N/A

The diagram shows a yellow polygon on a green PCB background. A red box highlights the 'Poly' column in the table below, with a red arrow pointing to it and the text: "This sets the polygon pour back-off to the PCB edge..."

	Arc	Track	SMD P	TH Pad	Via	Fill	Poly	Region	Text
Outline Edge	20	10	5	5	20	20	20	0	20
Cavity Edge	20	10	5	5	20	20	20	0	20
Cutout Edge	20	10	5	5	20	20	20	0	20
Split Barrier	20	10	5	5	20	20	20	0	20
Split Continuati	20	10	5	5	20	20	20	0	20

Required clearances between electrical objects and Board Cutouts / Board Cavities are determined using the largest of Electrical Clearance rule's Region -to- object settings and Board Outline Clearance rule's settings.

Let's start with something easy...

Now let's create a separate outline rule for the inside layer.


We will increase the polygon back-off by 5 mils on the inner VCC layer to offset it from the outer GND planes.

PCB Rules and Constraints Editor [mil]

Name: BoardOutlineClearance_Inner Comment: Unique ID: WISJNVRA Test Queries:

Where The Object Matches
Layer: Layer 3 - VCC

Constraints
Minimum Clearance: 25mil



This increases the polygon pour back-off slightly on the inner layers.

	Arc	Track	SMD P	TH Pad	Via	Fill	Poly	Region	Text
Outline Edge	25	25	25	25	25	25	25	25	25
Cavity Edge	25	25	25	25	25	25	25	25	25
Cutout Edge	25	25	25	25	25	25	25	25	25
Split Barrier	25	25	25	25	25	25	25	25	25
Split Continuati	25	25	25	25	25	25	25	25	25

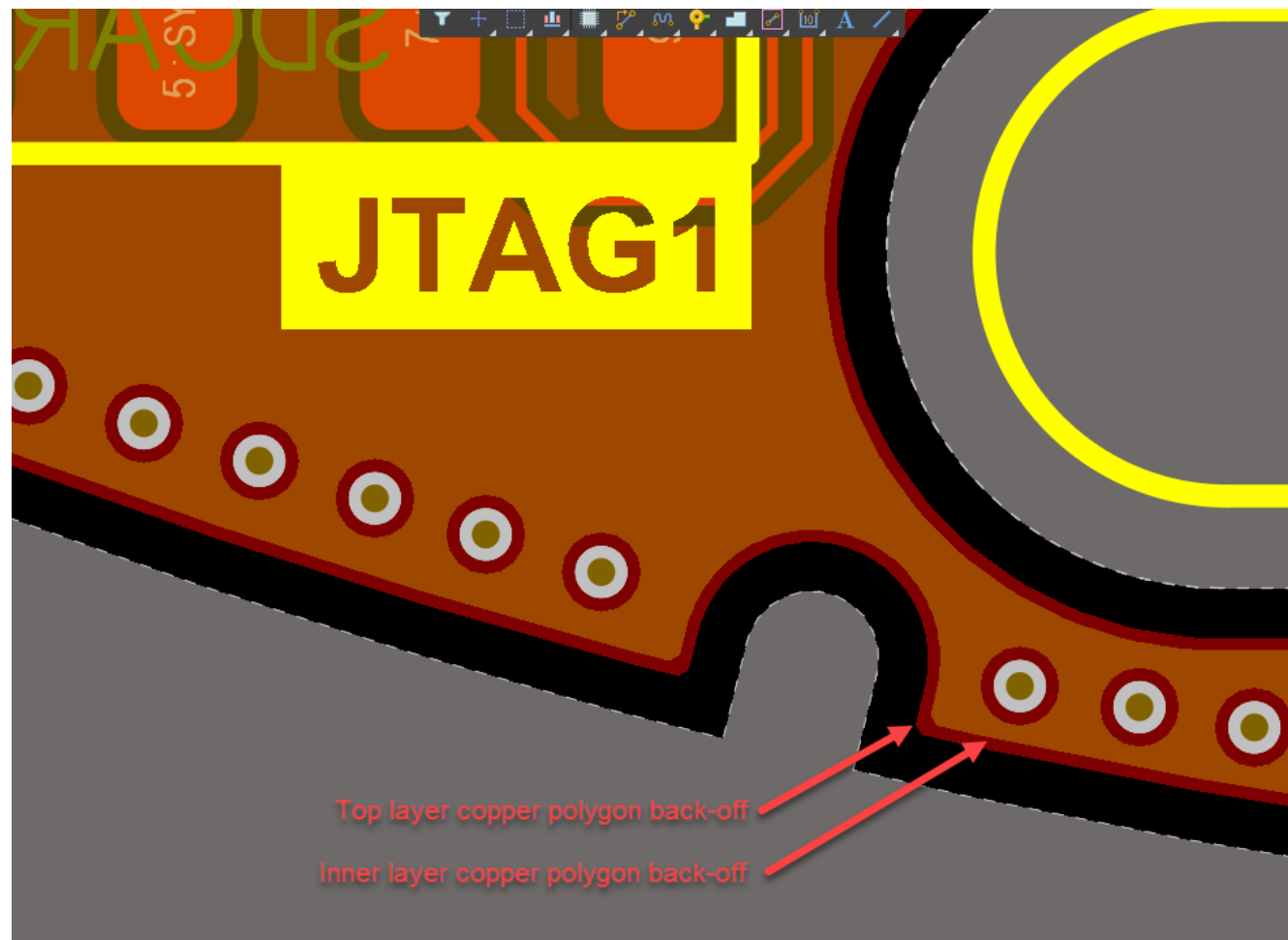
Required clearances between electrical objects and Board Cutouts / Board Cavities are determined using the largest of Electrical Clearance rule's Region -to- object settings and Board Outline Clearance rule's settings.

Rule Wizard... Priorities... Create Default Rules OK Cancel Apply

Let's start with something easy...

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This slightly greater polygon back-off on the inner VCC layer prevents a detrimental field effect called 'fringing'.



Fringing is an outward EMI radiation from the Power and GND planes at the edge of the PCB as shown here.

2. 20H RULE

20H rule: If there are high-speed currents on the board, there are electromagnetic fields associated with them. At the edge of the planes (presumably at the edge of the board) these fields will fringe outward from the board as shown in Figure 1. If the ground plane is larger than the power plane, the energy can not radiate out, as we can see from Figure 1(b). Thus, outward EMI radiation is reduced and there is less chance for an external EMI problem.

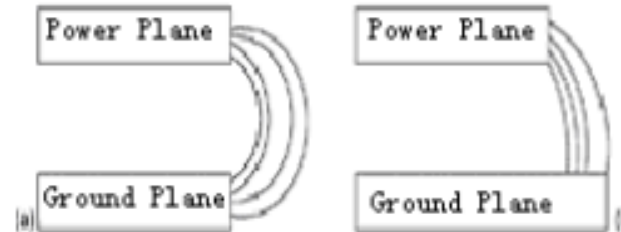


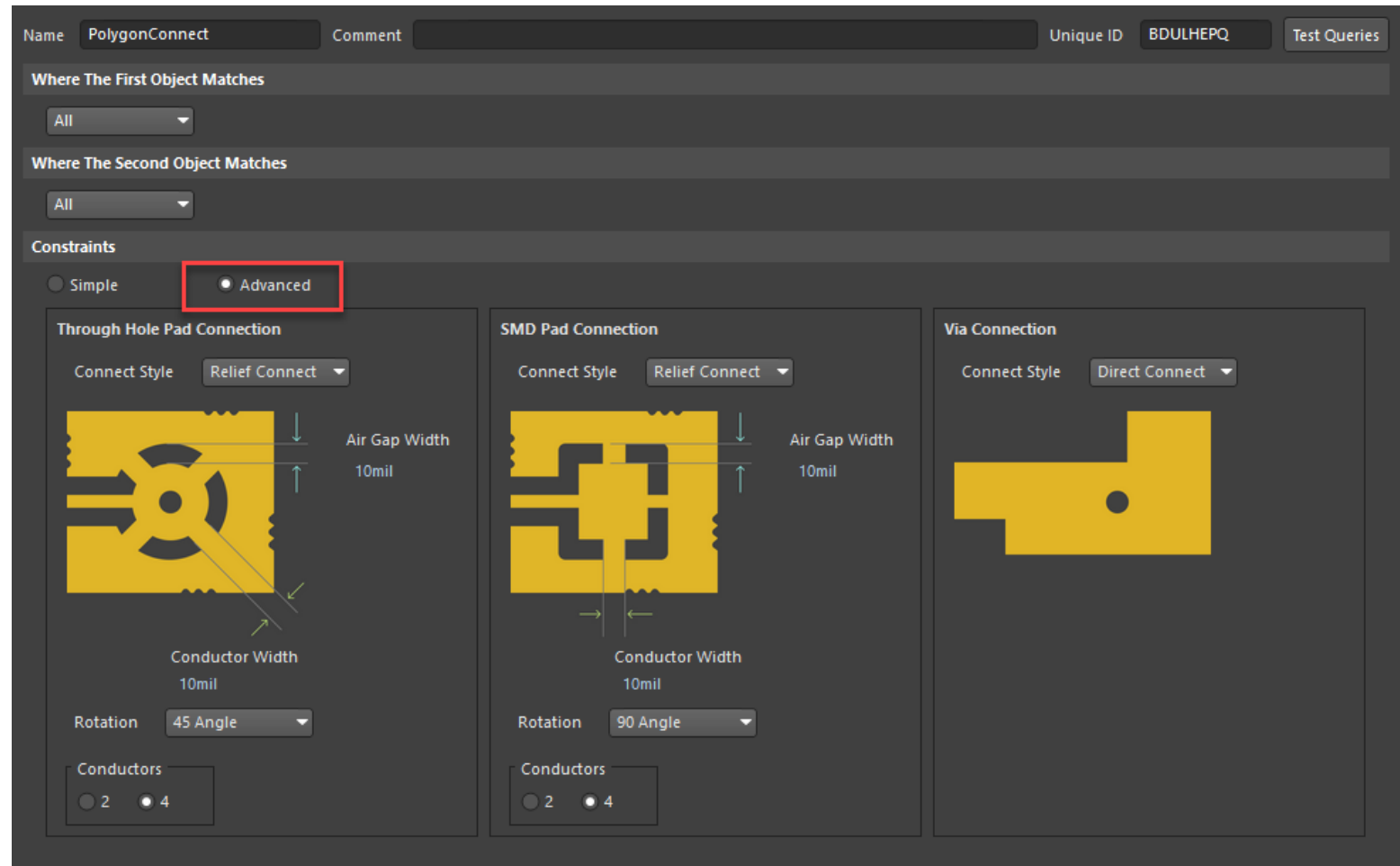
Figure 1: Recessing power plane may reduce outward fringing.

The reduction of edge radiation relates to the plane edge retraction. 20H rule (H is the height between the power plane and the ground plane) take it that if the power plane edge is retracted 20H of the ground plane edge, 70% of the energy radiation can be repressed.

20H rule is experiential method without theoretically confirmation and demonstration. Some designers believe that the 20H rule will cause more radiation than not applying it [2, 3]. There also exist a saying that whether the 20H rule is applicable depends on the dimension of the PCB and the frequency and the layers separation [4]. Others think that using discrete components instead of implementing the 20-H rule is another choice [5].

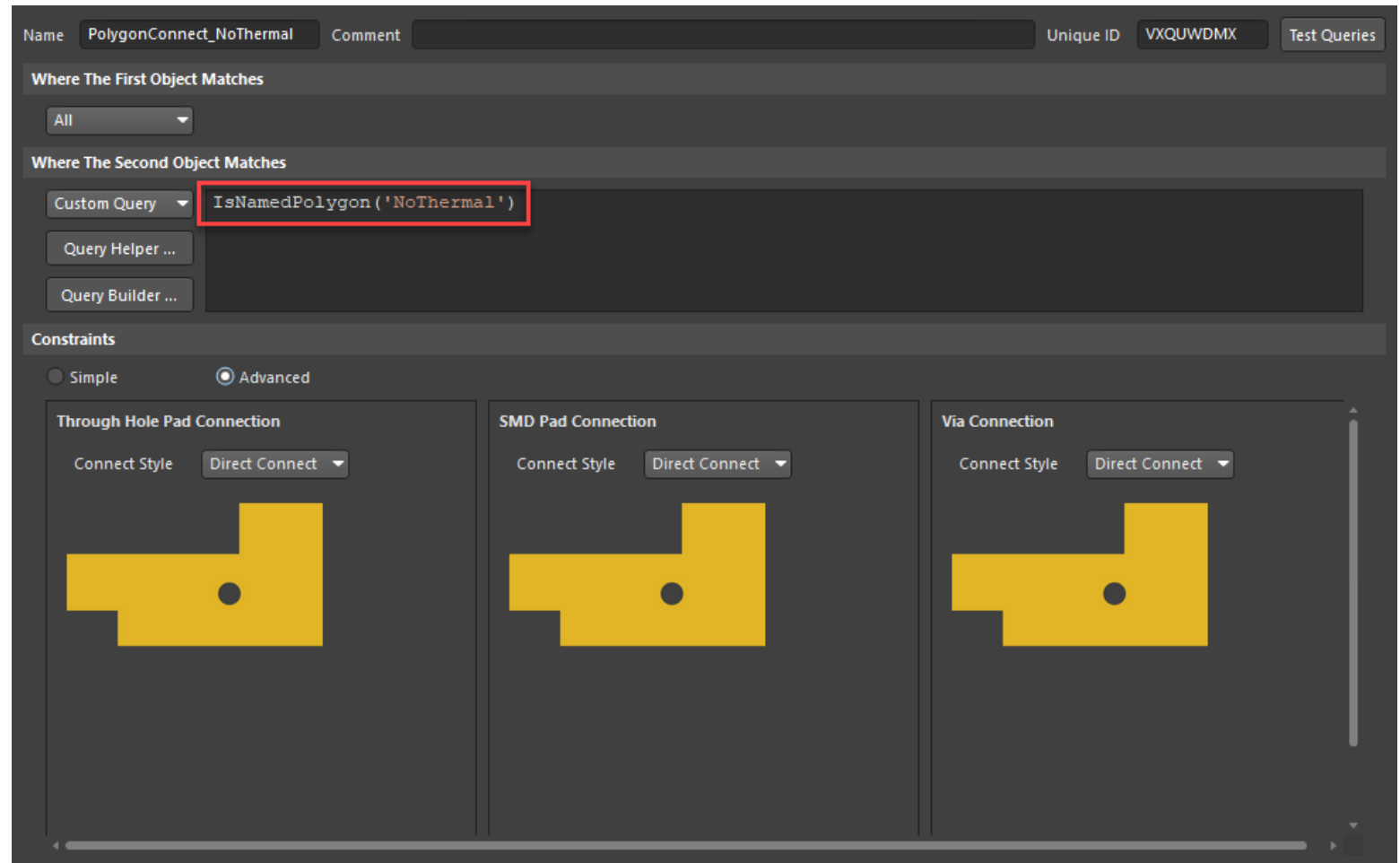
...polygon DRC options have been greatly enhanced in recent revision updates!

Click the 'Advanced' radio button to view these options.



...what if we want our polygons to flood the SMD and through-hole pads with no thermal relief?

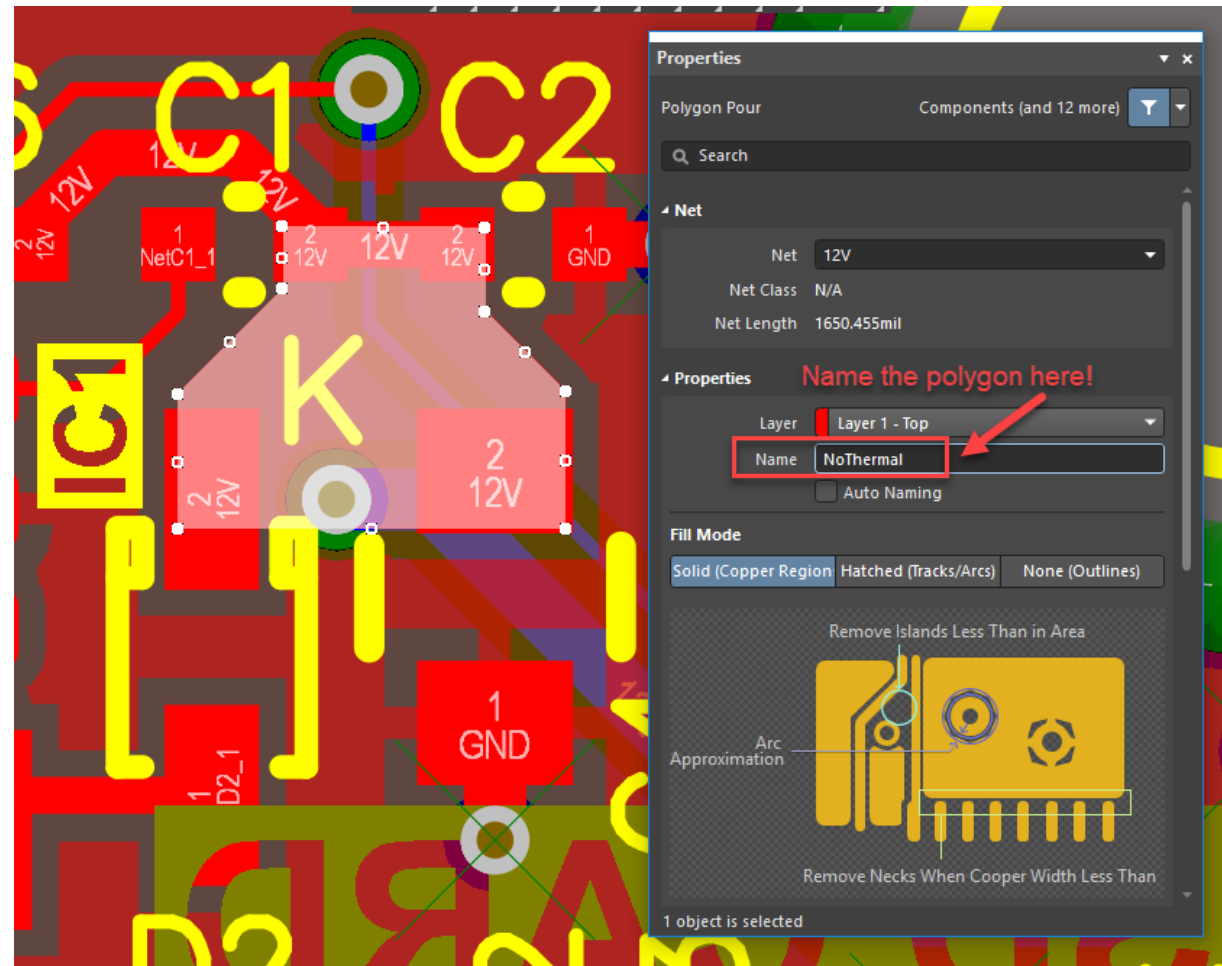
Let's create a NoThermal polygon rule!



Here is an easy way to create a polygon rule...

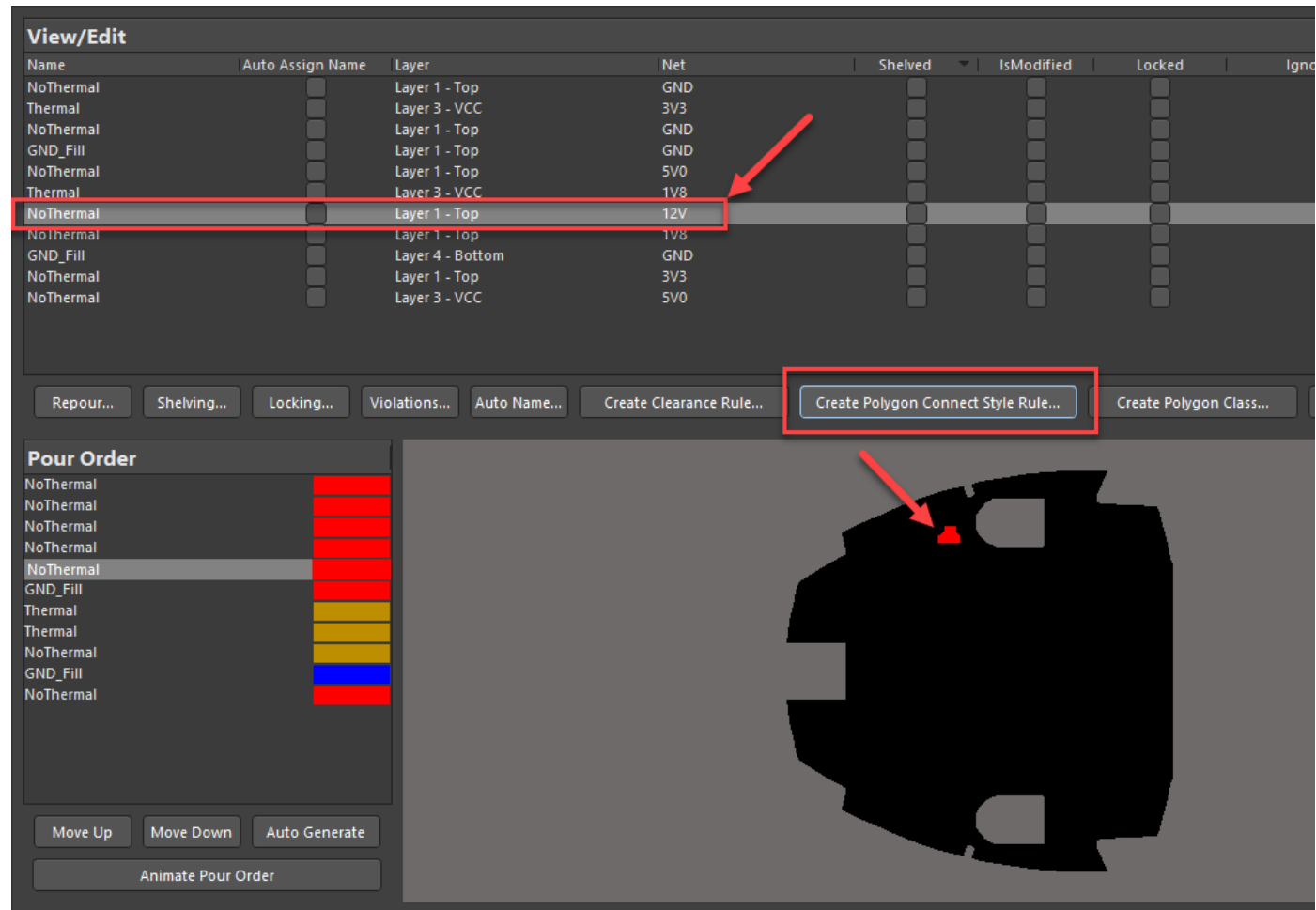
First, select the polygon that you wish to eliminate the thermal relief connections.

Then rename it appropriately in the Properties panel as shown here. I'll call it 'NoThermal'.



Here is an easy way to create a polygon rule...

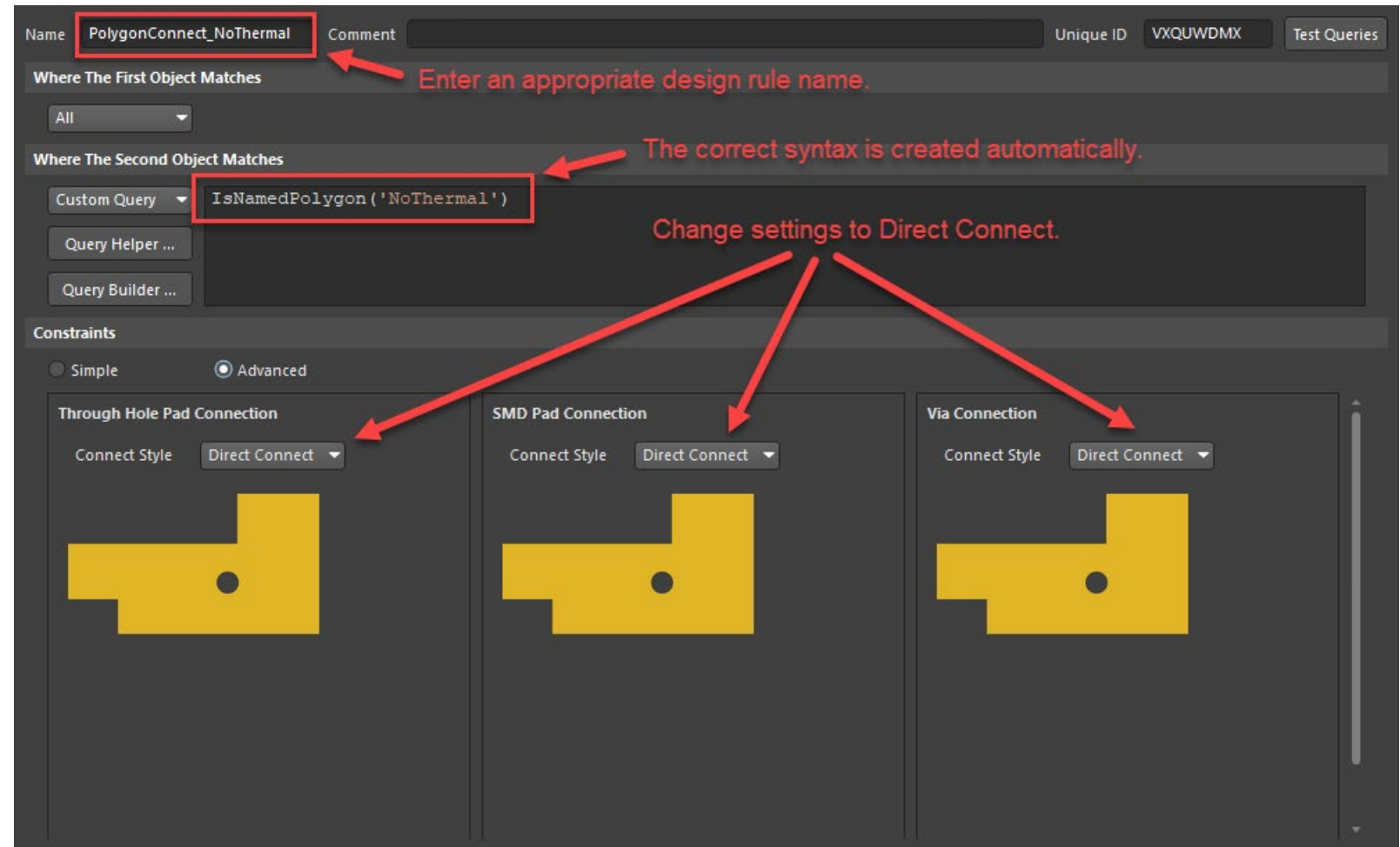
Next, in the Polygon Pour Manager dialog box (shown), select the 'Create Polygon Connect Style Rule...'



A polygon clearance rule can be created in a similar way...

Finally, in the design rule dialog box that appears, enter an appropriate name and change the connection style settings to Direct Connect.

This new rule now appears in the design rules!



Here is an easy way to create a polygon rule...

This same procedure can be used to create a polygon clearance rule for a GND fill copper polygon.

This allows us to set increased clearances on these planes.

The screenshot shows the 'PCB Rules and Constraints Editor [mil]' window. The 'Design Rules' tree on the left has 'Clearance_GND_Fill' selected under the 'Electrical' category. The main panel shows the rule configuration:

- Name: Clearance_GND_Fill
- Unique ID: IRGWAJVE
- Where The First Object Matches: Custom Query with the expression `InNamedPolygon('GND_Fill')`
- Where The Second Object Matches: All
- Constraints: Different Nets Only, Minimum Clearance: 8mil, Ignore Pad to Pad clearances within a footprint (checked)
- Mode: Simple
- Clearance Table:

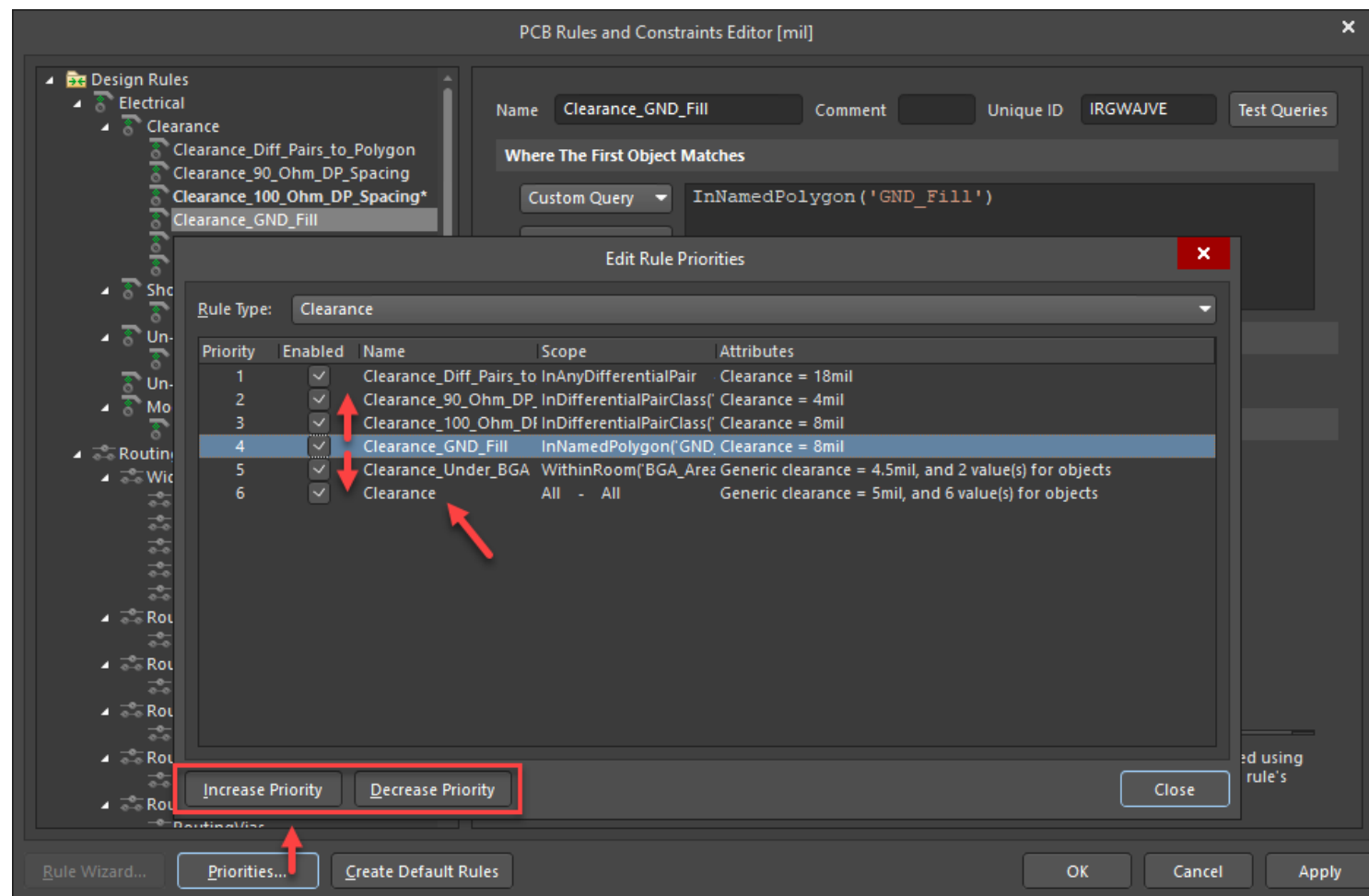
	Track	SMD Pad	TH Pad	Via	Copper	Text
Track	8					
SMD Pad	8	8				
TH Pad	8	8	8			
Via	8	8	8	8		
Copper	8	8	8	8	8	
Text	8	8	8	8	8	8
Hole	8	8	8	8	8	8

Required clearances between electrical objects and Board Cutouts / Board Cavities are determined using the largest of Electrical Clearance rule's Region -to- object settings and Board Outline Clearance rule's settings.

Order of priority and processing is critical...

If a new design rule doesn't seem to be working correctly, try increasing the priority as shown.

The baseline default rule should always be the catch-all at the bottom of the list.



Now let's create some differential pair rules...

Now we need to create a design rule for our 90 ohm differential USB signals as shown.

The screenshot shows the 'PCB Rules and Constraints Editor [mil]' window. The left-hand tree view shows the hierarchy of rules, with 'Differential Pairs Routing' expanded and '90_Ohm_DP' selected. The main panel shows the configuration for the '90_Ohm_DP' rule. The 'Where The Object Matches' section has 'Diff Pair Class' set to '90_Ohms_DP'. The 'Constraints' section shows a diagram of a differential pair with various parameters: Min Width (N/A), Min Gap (N/A), Preferred Width (N/A), Preferred Gap (N/A), Max Width (N/A), and Max Gap (N/A). Below the diagram, 'Max Uncoupled Length' is set to 500mil and 'Layers in layerstack only' is checked. The 'Attributes on Layer' table is shown below, with a red box highlighting the first three rows.

Attributes on Layer						Layer Stack Reference
Min Width	Min Gap	Preferred Wi	Preferred G	Max Width	Max Gap	Name
3mil	4mil	5.5mil	4mil	5.5mil	4mil	Layer 1 - Top
0mil	0mil	0mil	0mil	0mil	0mil	Layer 3 - VCC
3mil	4mil	5.5mil	4mil	5.5mil	4mil	Layer 4 - Bottom

Now let's create some differential pair rules...

This track width and spacing information is gained from our favorite online calculator.

Differential Pairs

Conductor Width (W) **mils**

Conductor Spacing (S) **mils**

Conductor Height (H) **mils**

W/H = 1.100
S/H = 0.800

Target Zdiff **Ohms**

Formula Restrictions:
0.1 < W/H < 3.0
0.1 < S/H < 3.0

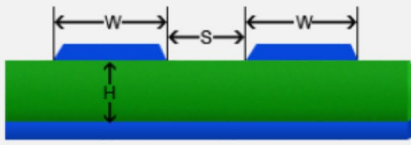
Zdiff **Ohms**

Zo **Ohms**

+/- Tolerance = 10%

Ohms

Ohms



Options

Base Copper Weight
 0.25oz
 0.5oz
 1oz
 1.5oz
 2oz
 2.5oz
 3oz
 4oz
 5oz

Plating Thickness
 Bare PCB
 0.5oz
 1oz
 1.5oz
 2oz
 2.5oz
 3oz

Differential Layer
 Edge Cpld Ext
 Edge Cpld Int Sym
 Edge Cpld Int Asym
 Edge Cpld Embed
 Broad Cpld Shld
 Broad Cpld NShld

Units
 Imperial
 Metric

Substrate Options
Material Selection

Er Tg (°C)

Temp Rise (°C)

Temp in (°F) = 36.0

Ambient Temp (°C)

Temp in (°F) = 71.6

Information

Total Copper Thickness
1.40 mils






Via Thermal Resistance
N/A

Via Count:

Conductor Temperature
Temp in (°C) = N/A
Temp in (°F) = N/A

Via Voltage Drop
N/A

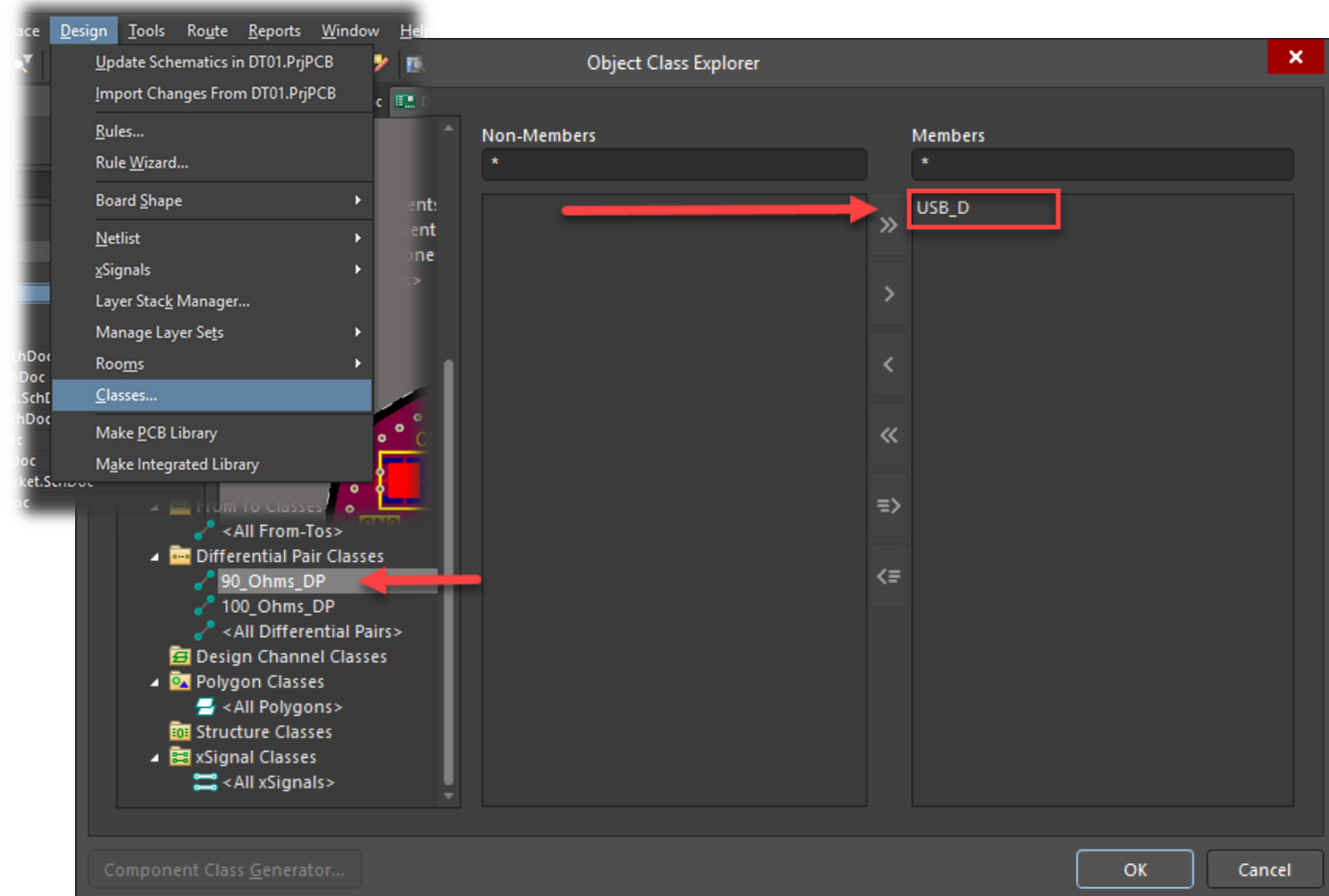
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Turnkey Electronic Engineering Solutions

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Now let's create some differential pair rules...

The best practice is to define a Differential Pair Class for these USB signals.

Think of these classes as a bucket to contain the nets we want to constrain.



Now let's create some differential pair rules...

Next we need to create a Width rule for these signals as shown.

Yes, this seems redundant but is necessary to automate the routing.

The screenshot shows the PCB Rules and Constraints Editor with the following configuration:

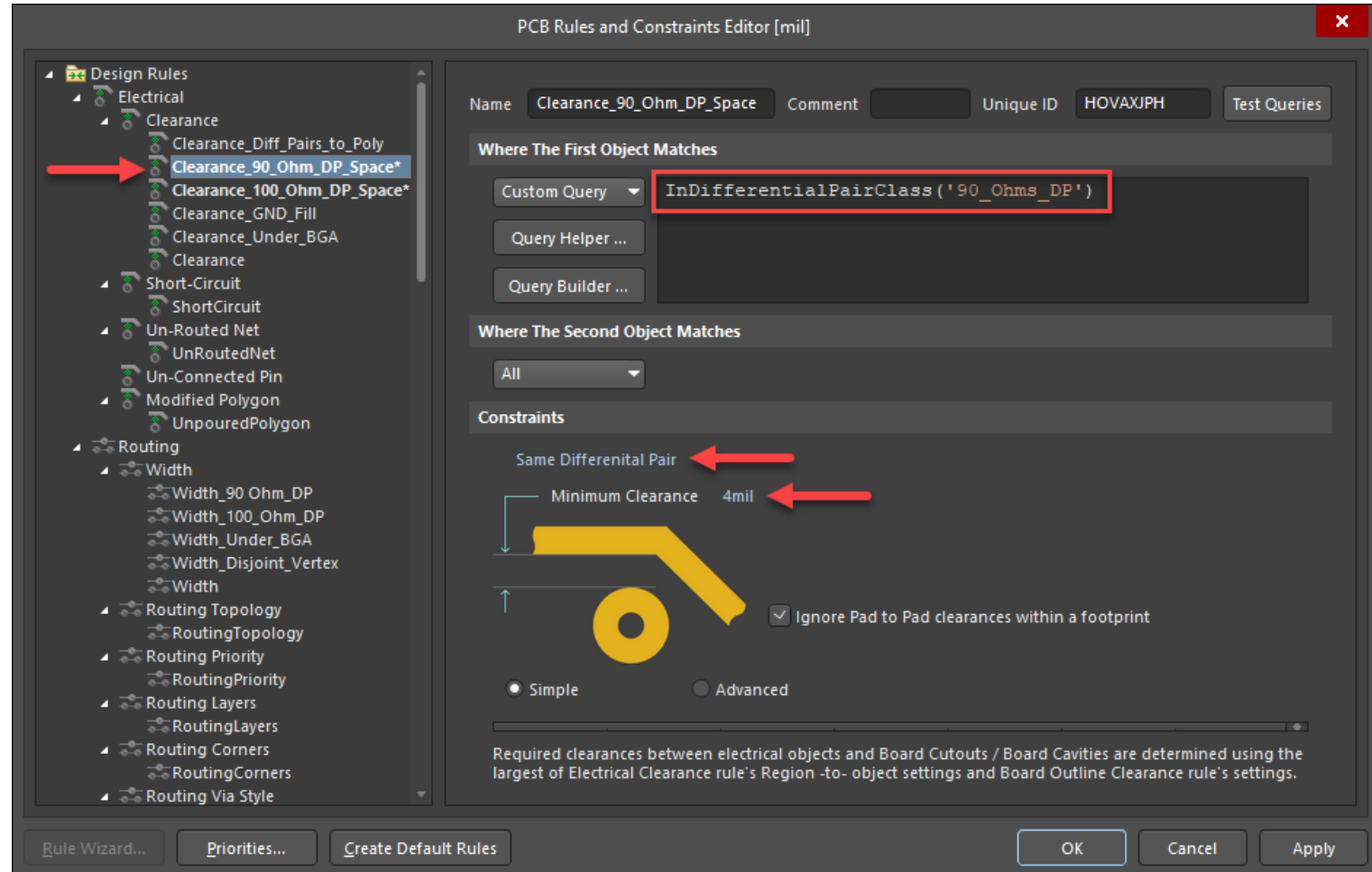
- Name:** Width_90 Ohm_DP
- Comment:** (empty)
- Unique ID:** LPNSVENP
- Test Queries:** (empty)
- Where The Object Matches:** Custom Query: `InDifferentialPairClass ('90_Ohms_DP')`
- Constraints:**
 - Preferred Width: N/A
 - Min Width: N/A
 - Max Width: N/A
 - Check Tracks/Arcs Min/Max Width Individually (selected)
 - Check Min/Max Width for Physically Connected Copper (tracks, arcs, fills, pads & vias) (unselected)
 - Characteristic Impedance Driven Width (unselected)
 - Layers in layerstack only (checked)
- Attributes on Layer Table:**

Attributes on Layer			Layer Stack Reference		Absolute Layer	
Min Width	Preferred Size	Max Width	Name	In	Name	In
5.5mil	5.5mil	5.5mil	Layer 1 - Top	32	TopLayer	1
0mil	0mil	0mil	Layer 3 - VCC	33	MidLayer1	2
5.5mil	5.5mil	5.5mil	Layer 4 - Bottom	34	BottomLayer	32

Now let's create some differential pair rules...

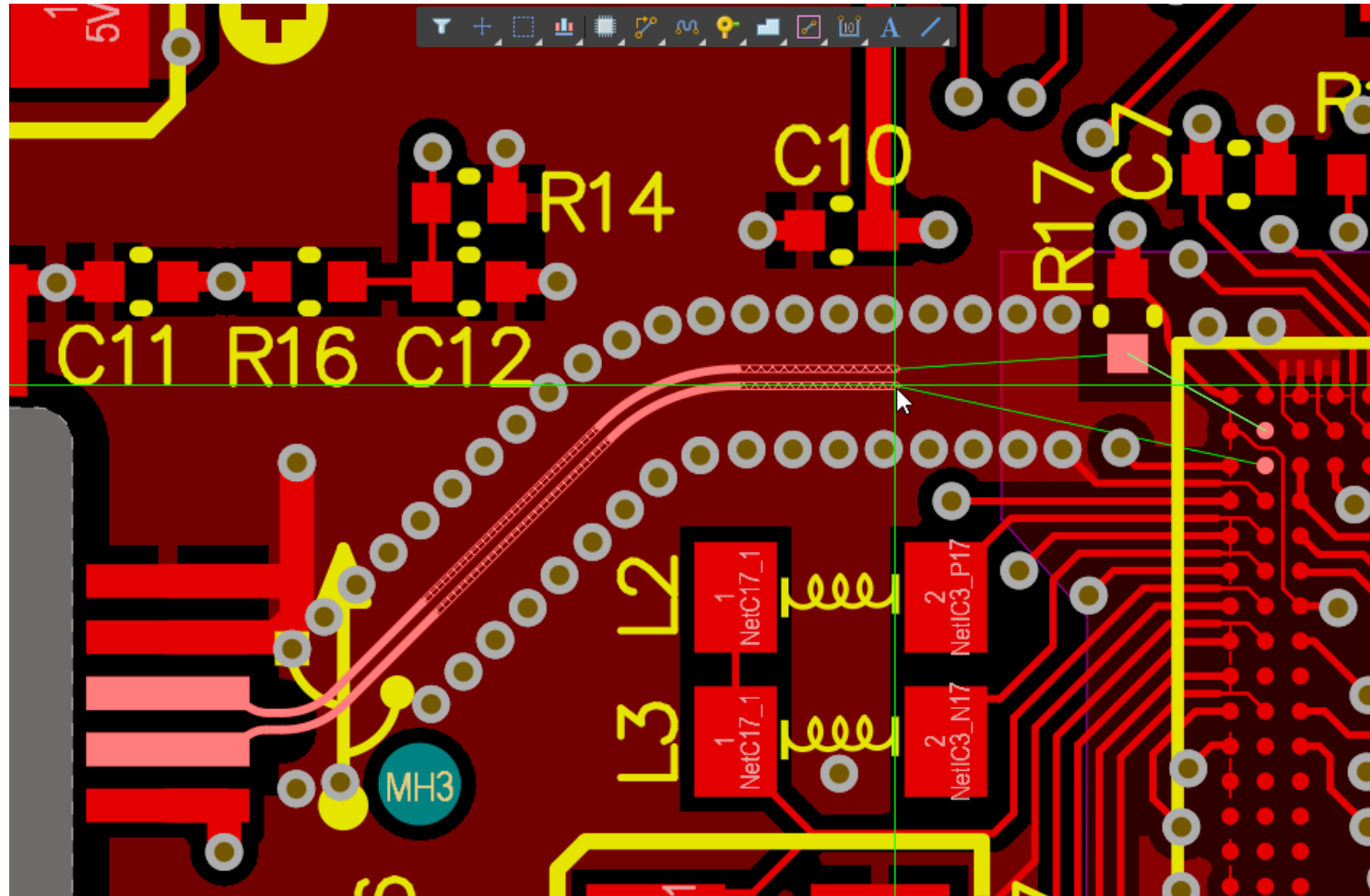
Finally, we need to create a Clearance rule to define the required spacing between the signals as shown.

Yes, more redundancy!



The BIG payoff...

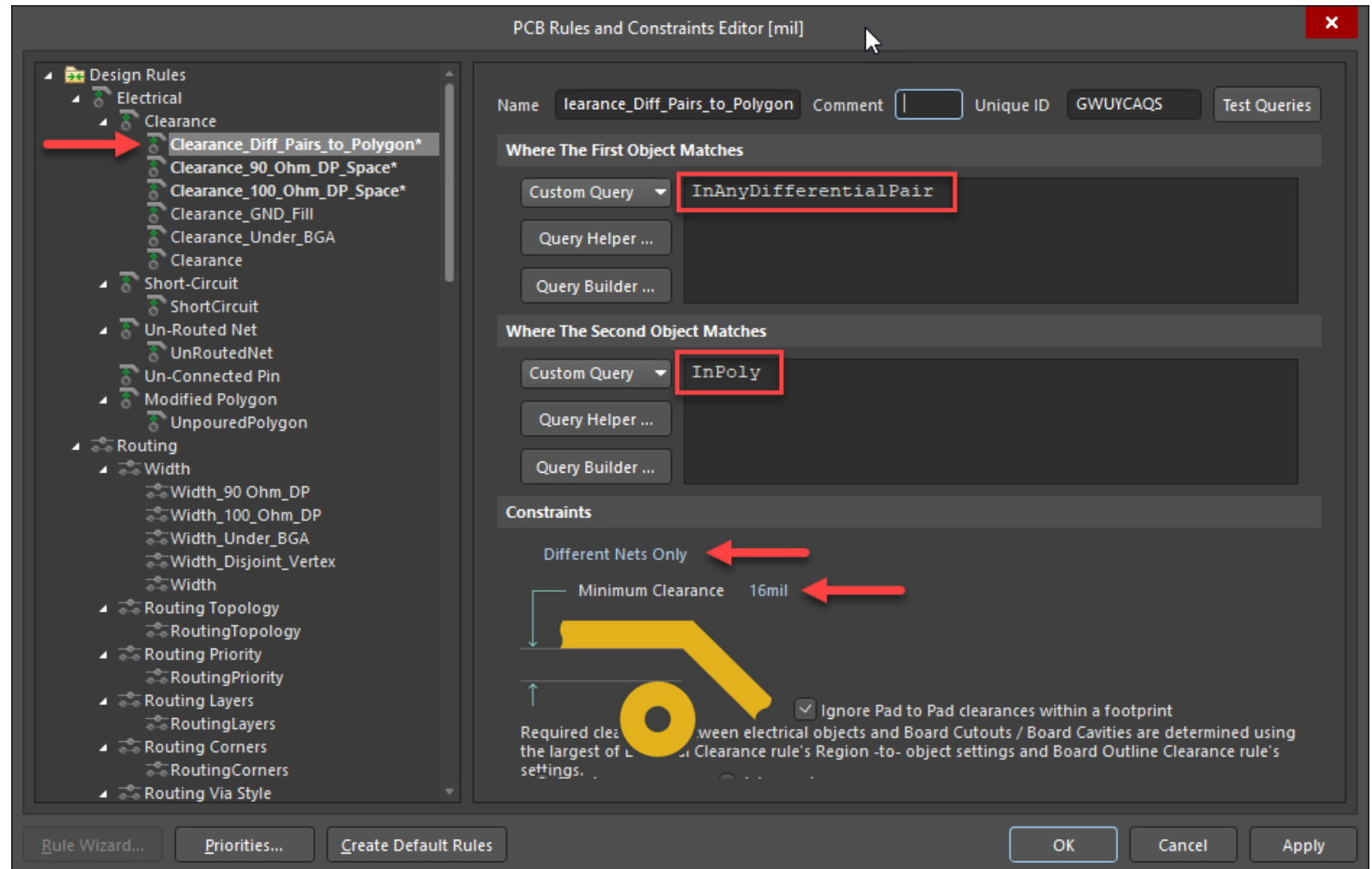
Now, using the 'Interactively Route Differential Pair Connections' command, we get a perfectly paired 90 ohm route as shown!



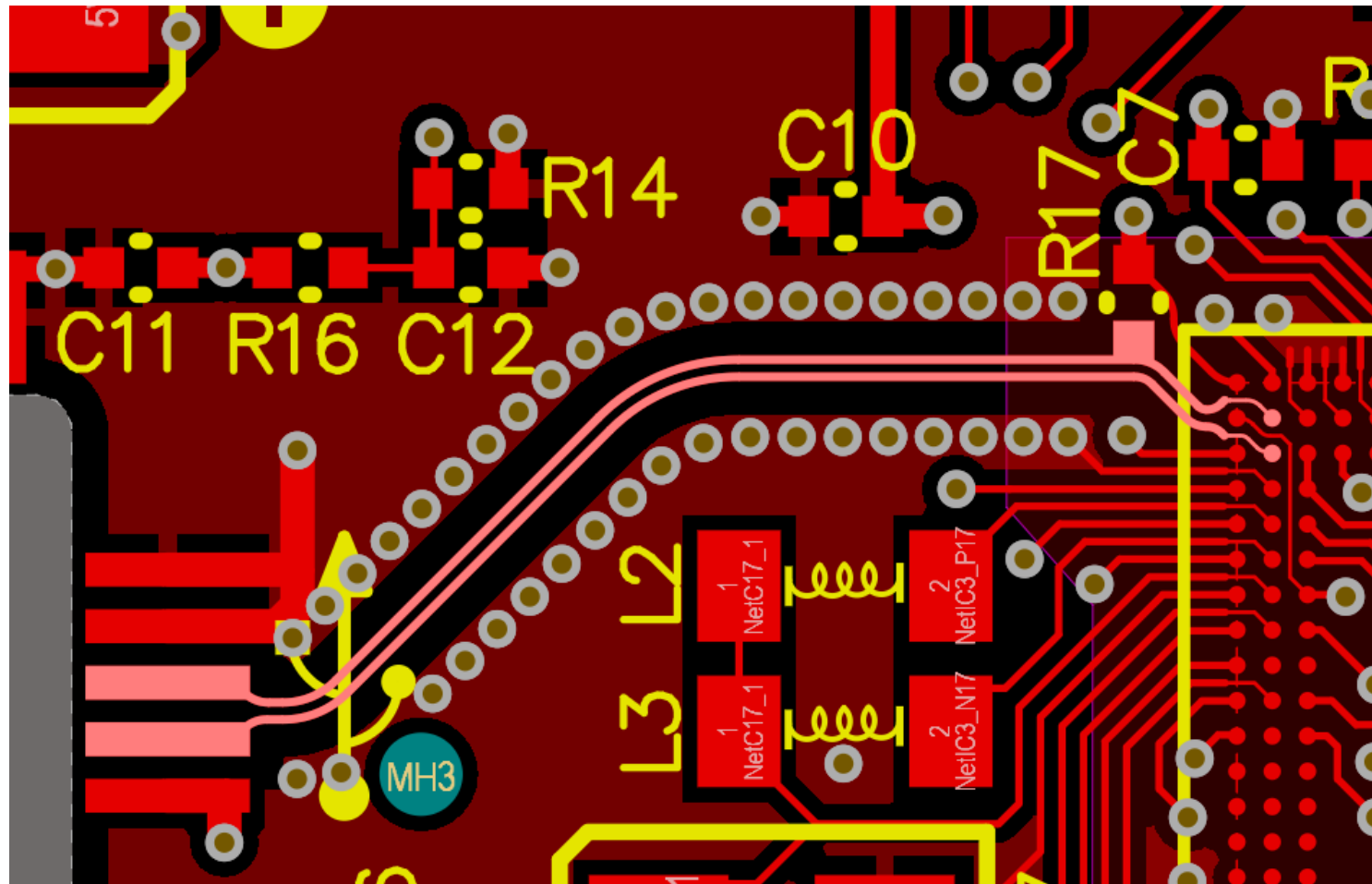
Still one more consideration...

How do we keep the GND plane a sufficient distance to not adversely affect these diff paired signals?

By creating a design rule clearance from any diff pair to any polygon plane as shown.



The resulting plane back-off is a perfectly smooth separation from the 90 ohm signals as shown here.

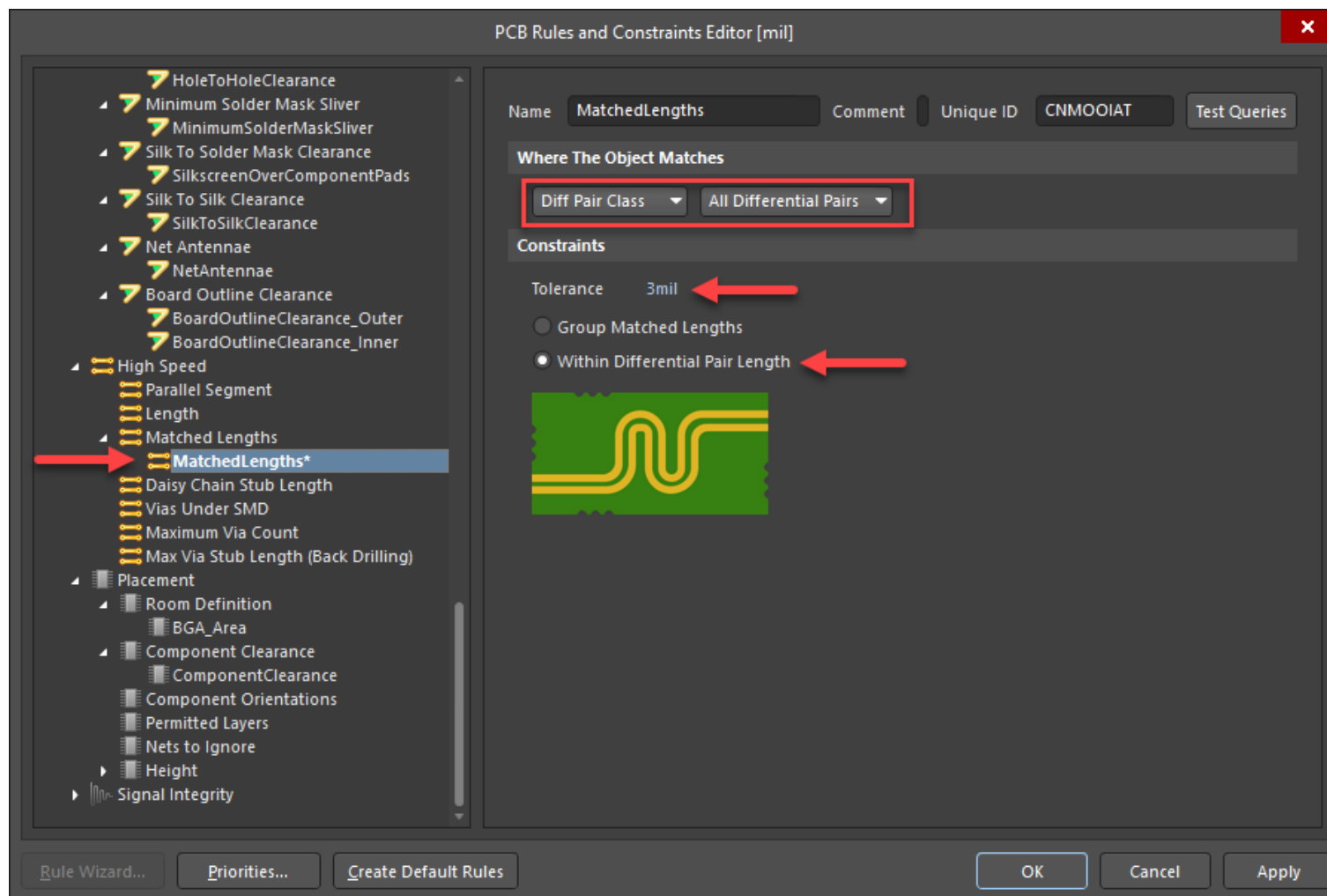


Oh, and one more thing...

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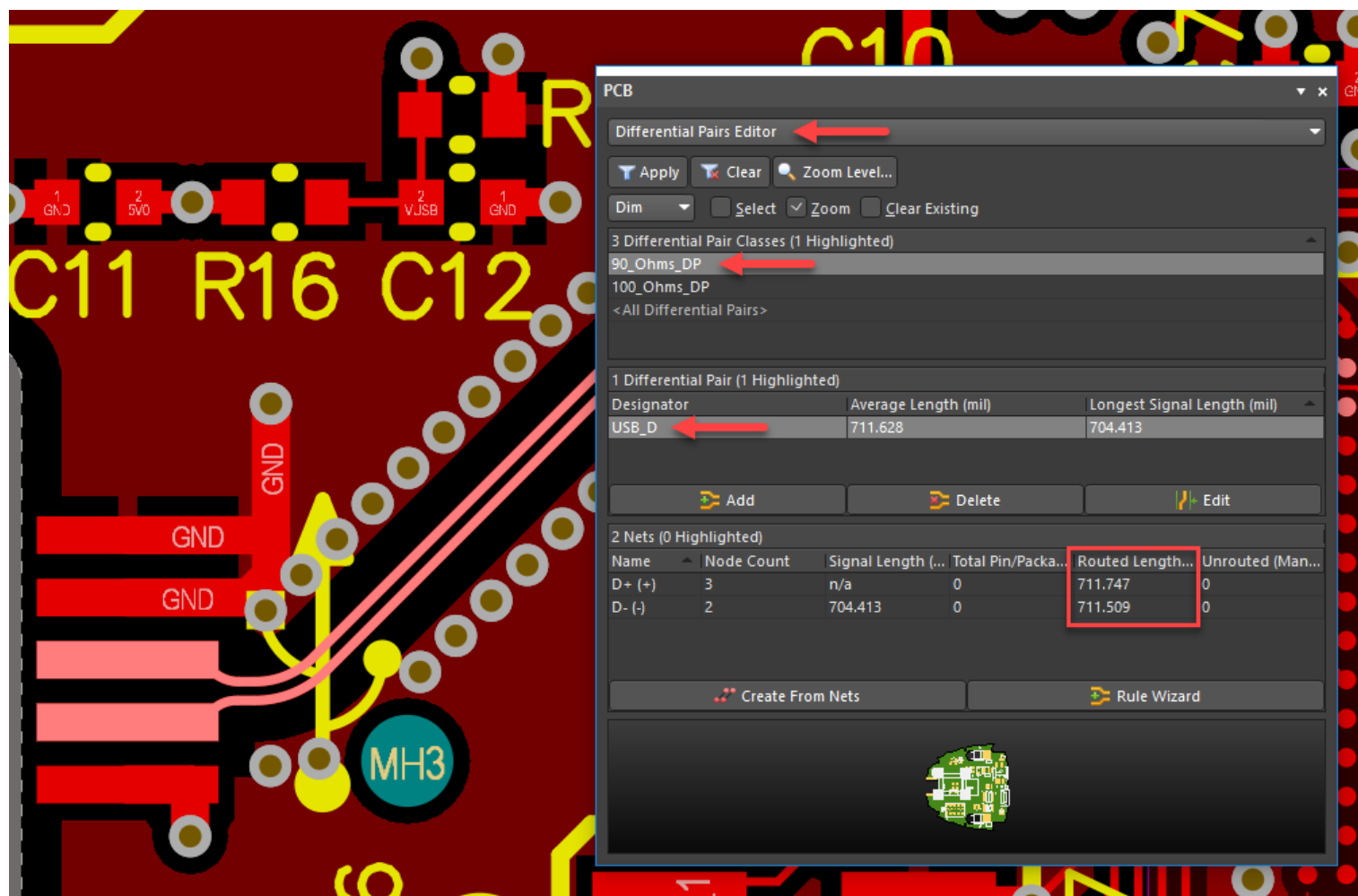
If we wish to ensure the length matching of these diff paired signals, we can add the Matched Length design rule tolerance shown here.

Incidentally, the Group Matched Length option is for single ended impedance controlled nets.



Oh, and one more thing...

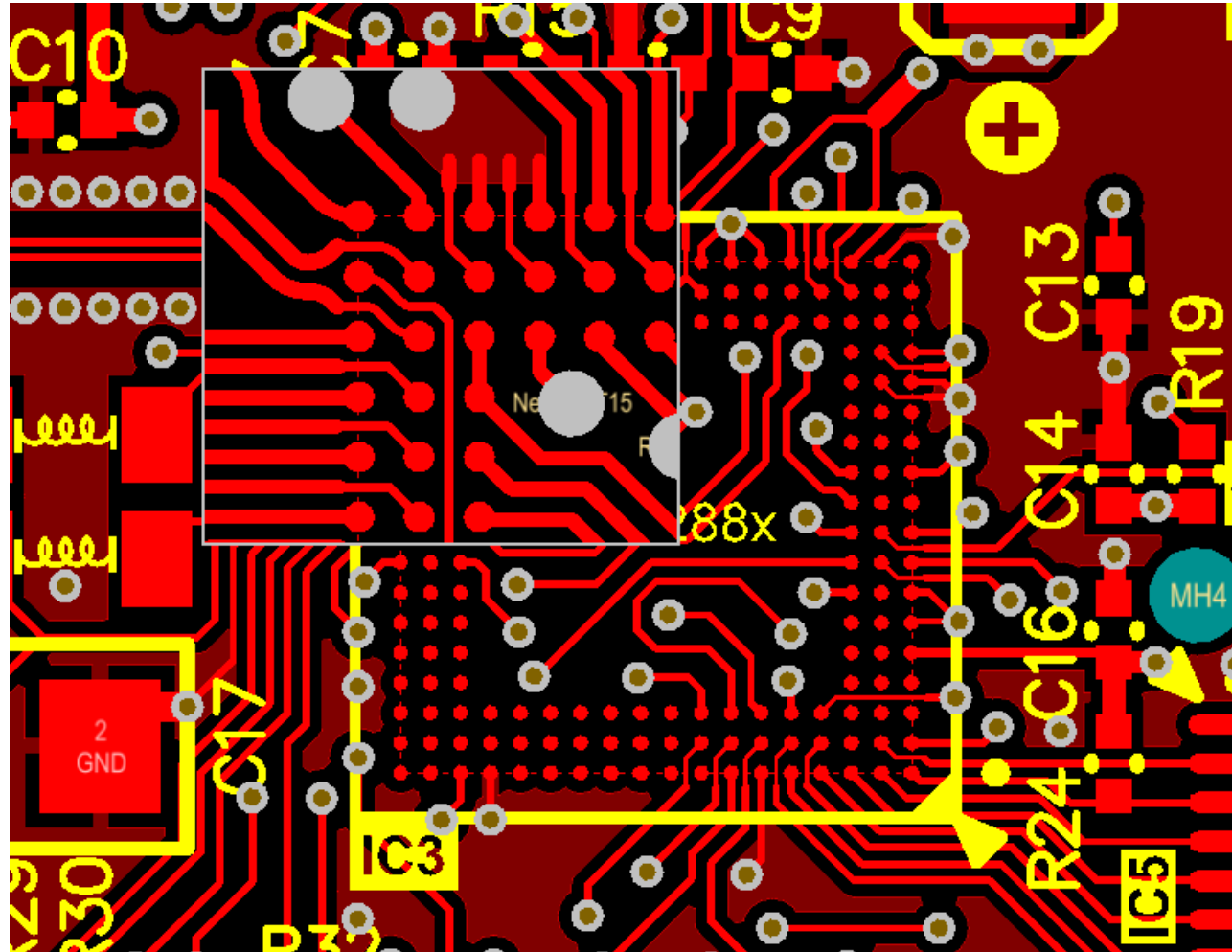
If necessary, the signal lengths can be verified and tuned from the Differential Pairs Editor of the PCB Panel.



Now what to do about the spacing under the BGA...

The 0.5mm pitch BGA poses a unique DRC challenge because we must neck down the tracks to route between the pads!

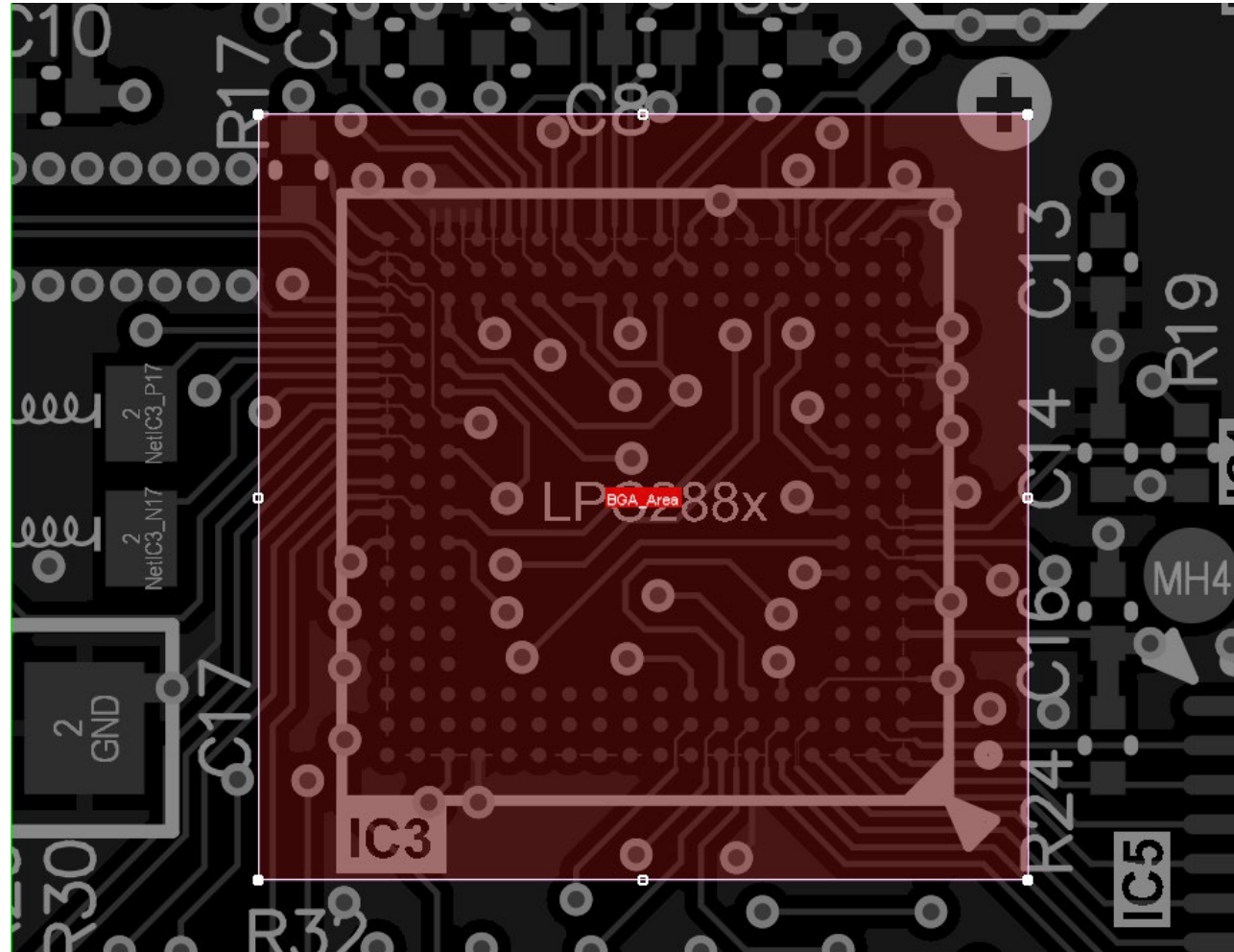
We want to maintain a minimum 5mil trace and space rule everywhere but under the BGA.



Now what to do about the spacing under the BGA...

To define separate design rules specific to the BGA area we must place a room delineating that area as shown here.

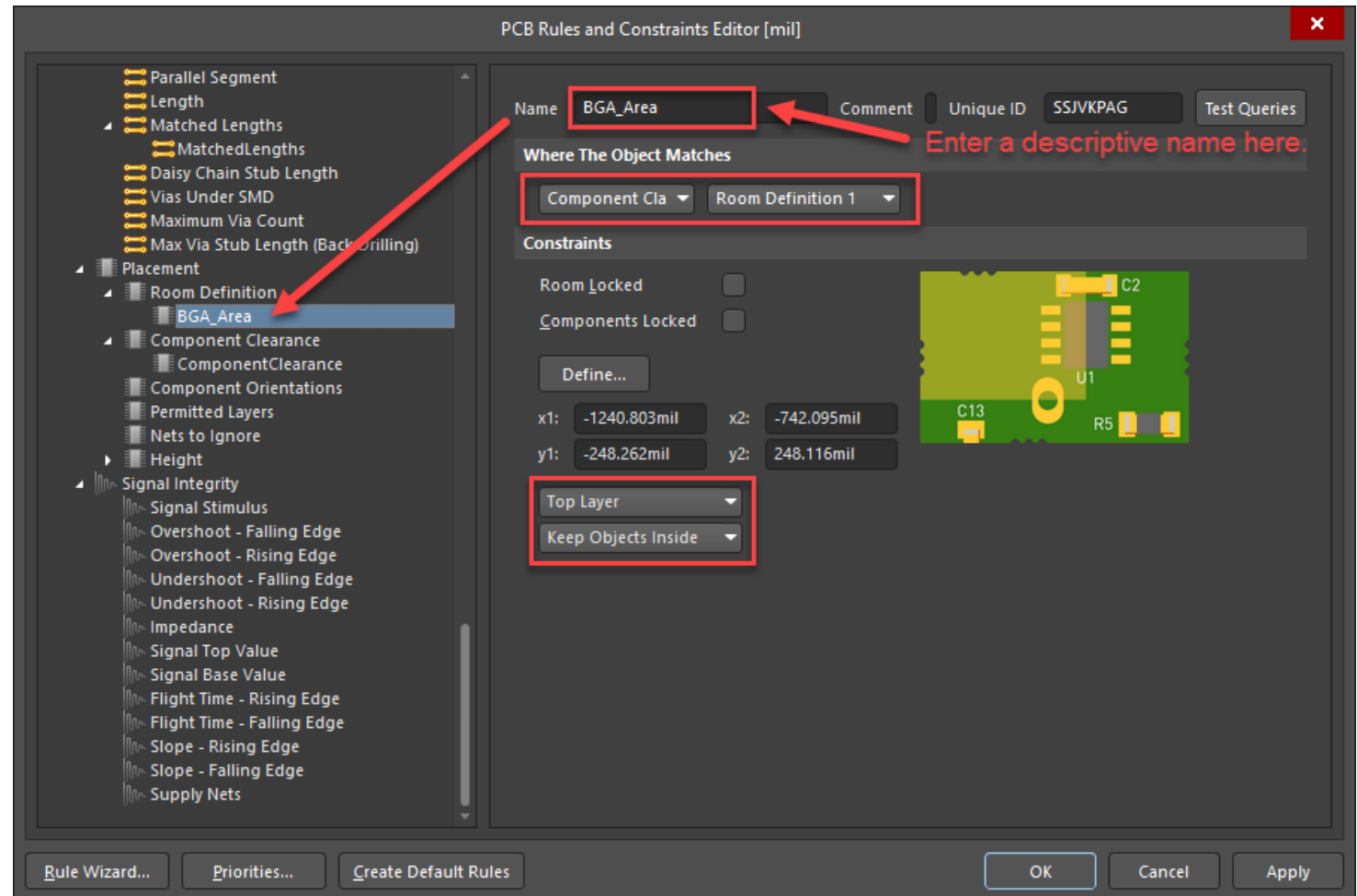
Be aware that you can only edit rooms with those options under the Design/Rooms command.



Now what to do about the spacing under the BGA...

Now give this room a descriptive name in the Room Definition section of the design rules dialog box as shown here.

Next, define this room under Component Class as 'Room Definition 1' in the pull down selection box.



Now what to do about the spacing under the BGA...

Next, create a new clearance rule for this room definition and set the smaller clearances as shown here.

The screenshot shows the 'PCB Rules and Constraints Editor' window. On the left, a tree view shows 'Design Rules' expanded to 'Electrical' > 'Clearance', with 'Clearance_Under_BGA' selected. The main panel shows the rule configuration:

- Name: Clearance_Under_BGA
- Where The First Object Matches: Custom Query with value 'WithinRoom('BGA_Area')'
- Where The Second Object Matches: All
- Constraints: Different Nets Only, Minimum Clearance N/A, Ignore Pad to Pad clearances within a footprint checked.
- Mode: Simple
- Clearance Table:

	Track	SMD Pad	TH Pad	Via	Copper	Text
Track	4.5					
SMD Pad	3	4.5				

Required clearances between electrical objects and Board Cutouts / Board Cavities are determined using the largest of Electrical Clearance rule's Region -to- object settings and Board Outline Clearance rule's settings.

Now what to do about the spacing under the BGA...

Finally, we can create a minimum 3 mil width rule for the necked-down tracks under the BGA as shown here.

This allows for maximum width and clearances everywhere else.

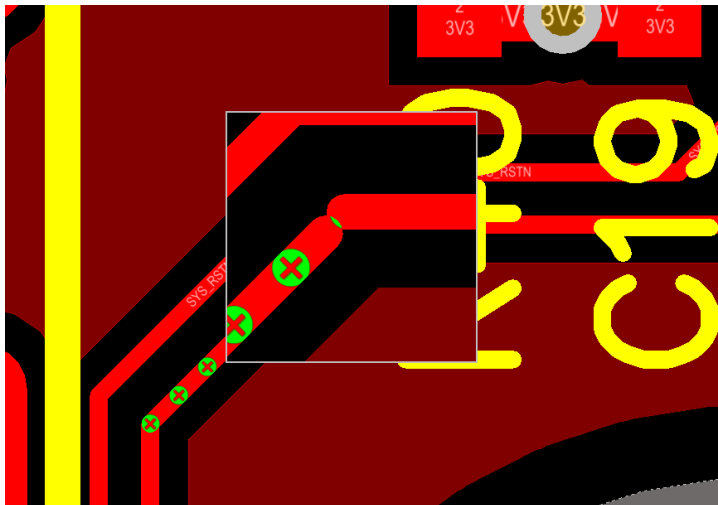
The screenshot shows the 'PCB Rules and Constraints Editor' window. The left pane shows a tree view of rules, with 'Width_Under_BGA' selected and highlighted by a red arrow. The right pane shows the configuration for this rule:

- Name: Width_Under_BGA
- Comment: (empty)
- Unique ID: WLHJQNE
- Test Queries: (empty)
- Where The Object Matches: Custom Query: WithinRoom('BGA_Area')
- Constraints: Preferred Width: 5mil, Min Width: 3mil, Max Width: 60mil
- Options: Check Tracks/Arcs Min/Max Width Individually, Check Min/Max Width for Physically Connected Copper (tracks, arcs, fills, pads & vias), Characteristic Impedance Driven Width, Layers in layerstack only
- Attributes on Layer table:

Attributes on Layer			Layer Stack Reference		Absolute Layer	
Min Width	Preferred S...	Max Width	Name	In	Name	In
3mil	5mil	60mil	layer 1 - Top	32	TopLayer	1
3mil	5mil	60mil	layer 3 - VCC	33	MidLayer1	2
3mil	5mil	60mil	layer 4 - Bottom	34	BottomLayer	32

Finally, let's check for disjoint vertices...

This rule option checks for tracks that have disjoint vertices as shown below.



PCB Rules and Constraints Editor [mil]

Name: Width_Disjoint_Vertex Comment: Unique ID: GMLPVLSE Test Queries

Where The Object Matches

Custom Query: All and Not WithinRoom('BGA_Area')

Query Helper ...

Query Builder ...

Constraints

Preferred Width: 5mil

Min Width: N/A Max Width: 60mil

Check Tracks/Arcs Min/Max Width Individually

Check Min/Max Width for Physically Connected Copper (tracks, arcs, fills, pads & vias)

Characteristic Impedance Driven Width

Layers in layerstack only

Attributes on Layer			Layer Stack Reference		Absolute Layer	
Min Width	Preferred SI	Max Width	Name	In	Name	In
3mil	5mil	60mil	Layer 1 - Top	32	TopLayer	1
3mil	5mil	60mil	Layer 3 - VCC	33	MidLayer1	2
3mil	5mil	60mil	Layer 4 - Bottom	34	BottomLayer	32

Rule Wizard... Priorities... Create Default Rules OK Cancel Apply

Well, this is great information, but...

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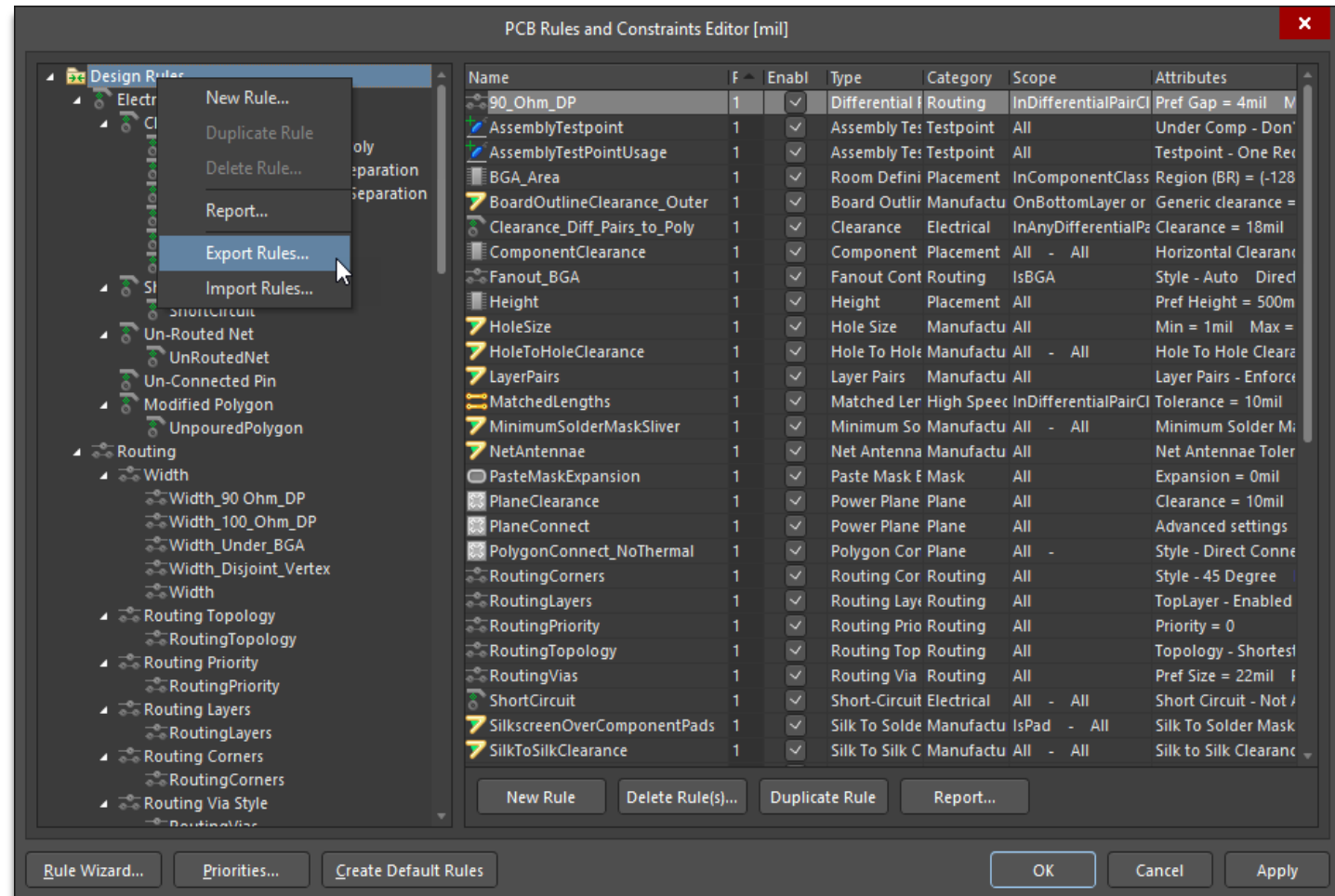
...how do I integrate these rules into my PCB as needed and applicable?

The key to successful design rule integration is to compile a comprehensive set of DRC rules that you can port from one project to the next.



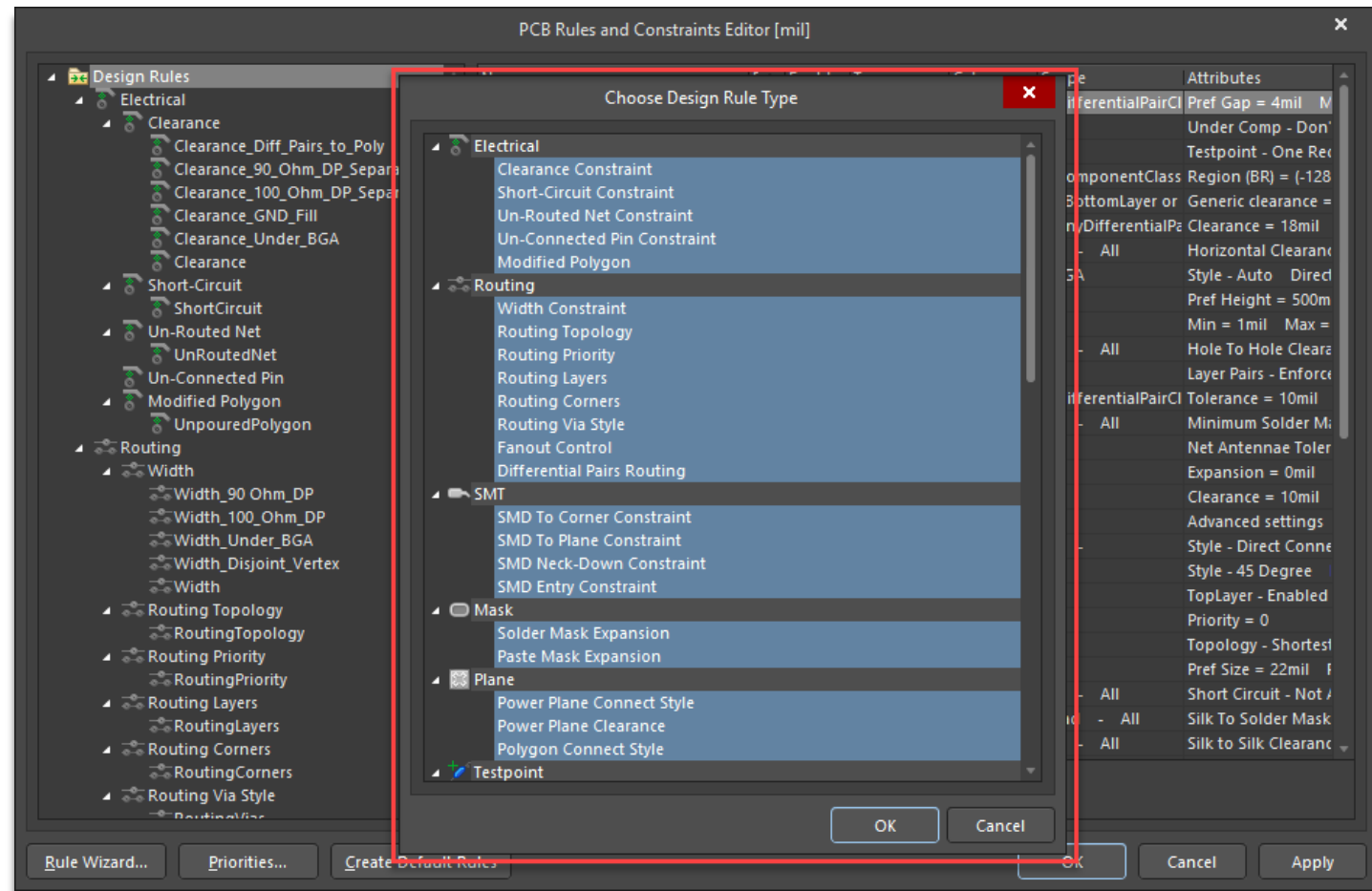
Name	Priority	Enabled	Type	Category	Scope	Attributes
90_Ohm_DP	1	<input checked="" type="checkbox"/>	Differential Pairs Routing	Routing	InDifferentialPairClass('90_Ohm_DP')	Pref Gap = 4mil Min Gap = 4mil
AssemblyTestpoint	1	<input checked="" type="checkbox"/>	Assembly Testpoint Style	Testpoint	All	Under Comp - Don't Allow Solder
AssemblyTestpointUsage	1	<input checked="" type="checkbox"/>	Assembly Testpoint Usage	Testpoint	All	Testpoint - One Required Min
BGA_Area	1	<input checked="" type="checkbox"/>	Room Definition	Placement	InComponentClass('Room')	Region (BR) = (-1286mil, -248.2
BoardOutlineClearance_Inn	1	<input checked="" type="checkbox"/>	Board Outline Clearance	Manufacturing	OnLayer('Layer 3 - VCC')	Board Clearance = 25mil
Clearance_Diff_Pairs_to_Poly	1	<input checked="" type="checkbox"/>	Clearance	Electrical	InAnyDifferentialPair -	Clearance = 16mil
ComponentClearance	1	<input checked="" type="checkbox"/>	Component Clearance	Placement	All - All	Horizontal Clearance = 10mil
Fanout_BGA	1	<input checked="" type="checkbox"/>	Fanout Control	Routing	BGA	Style - Auto Direction - Alter
ShortCircuit	1	<input checked="" type="checkbox"/>	Short-Circuit	Electrical	All - All	Short Circuit - Not Allowed
HoleToHoleClearance	1	<input checked="" type="checkbox"/>	Hole To Hole Clearance	Manufacturing	All - All	Hole To Hole Clearance = 10m
LayerPairs	1	<input checked="" type="checkbox"/>	Layer Pairs	Manufacturing	All	Layer Pairs - Enforce
PasteMaskExpansion	1	<input checked="" type="checkbox"/>	Paste Mask Expansion	Mask	All	Expansion = 0mil
PlaneClearance	1	<input checked="" type="checkbox"/>	Plane Clearance	Plane	All	Clearance = 10mil
RoutingCorners	1	<input checked="" type="checkbox"/>	Routing Corners	Routing	All	Style - 45 Degree Min Setbac
RoutingLayers	1	<input checked="" type="checkbox"/>	Routing Layers	Routing	All	TopLayer - Enabled InternalPla
RoutingPriority	1	<input checked="" type="checkbox"/>	Routing Priority	Routing	All	Priority = 0
ShortCircuit	1	<input checked="" type="checkbox"/>	Short-Circuit	Electrical	All - All	Short Circuit - Not Allowed
SilkToSolderMaskClearance	1	<input checked="" type="checkbox"/>	Silk To Solder Mask Clearance	Manufacturing	IsPart - All	Silk To Solder Mask Clearance
SilkToSilkClearance	1	<input checked="" type="checkbox"/>	Silk to Silk Clearance	Manufacturing	All	Silk to Silk Clearance = 0mil
SolderMaskExpansion	1	<input checked="" type="checkbox"/>	Solder Mask Expansion	Mask	All	Expansion = 0mil
TestPointUsage	1	<input checked="" type="checkbox"/>	Fabrication Testpoint Usage	Testpoint	All	Testpoint - One Required Min
UnpouredPolygon	1	<input checked="" type="checkbox"/>	Modified Polygon	Electrical	All	Allow modified - No Allow sh
UnRoutedNet	1	<input checked="" type="checkbox"/>	Un-Routed Net	Electrical	All	(No Attributes)
Width_90_Ohm_DP	1	<input checked="" type="checkbox"/>	Width	Routing	InDifferentialPairClass('90_Ohm_DP')	Pref Width = 5.5mil Min Wid
100_Ohm_DP	2	<input checked="" type="checkbox"/>	Differential Pairs Routing	Routing	InDifferentialPairClass('100_Ohm_DP')	Pref Gap = 8mil Min Gap = 8

After compiling your favorite design rules, you can export those rules by right clicking on the **Design Rules** header and selecting the **Export Rules...** option as shown here.



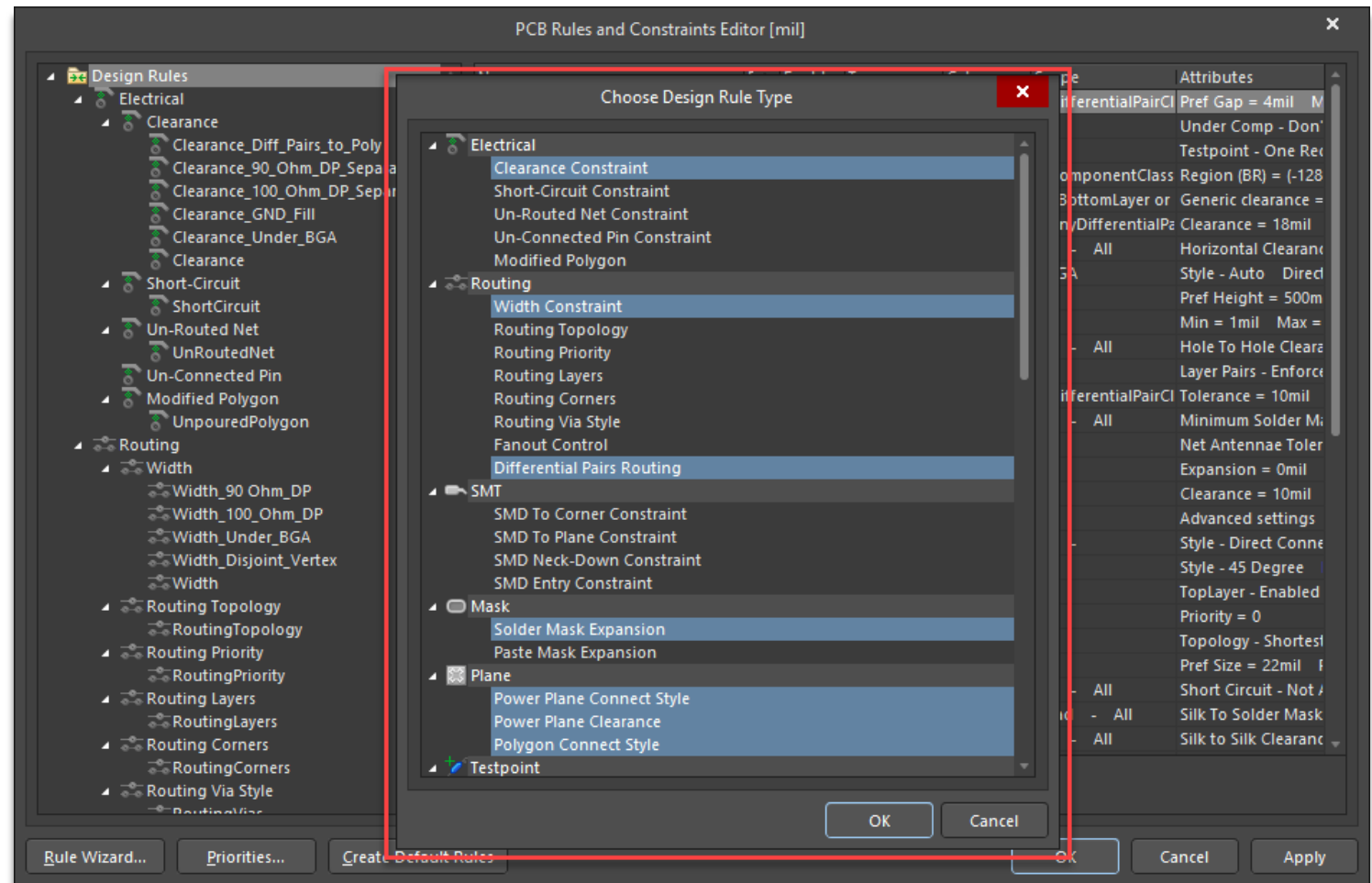
Then, in the dialogue box that appears, select and highlight all the rules to be exported as shown.

You will then be prompted to save the data file.



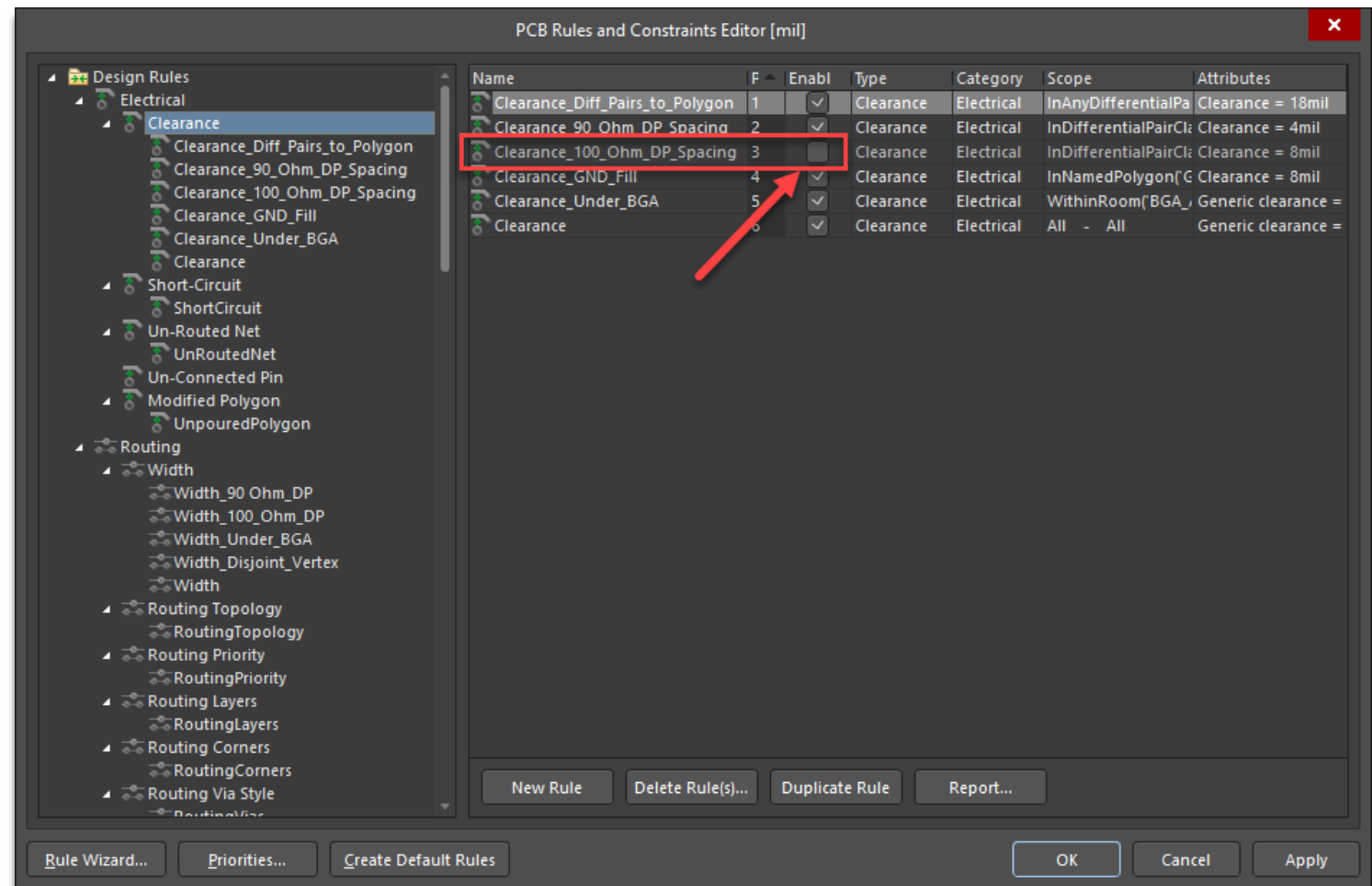
When importing design rules into an existing PCB database, you can then select only those rules that you wish to be imported.

Be aware that those existing rules will be over-written!



What about those design rules that aren't applicable...

With these comprehensive design rules loaded, you can simply uncheck those rules that are not applicable to your particular PCB design as shown here.

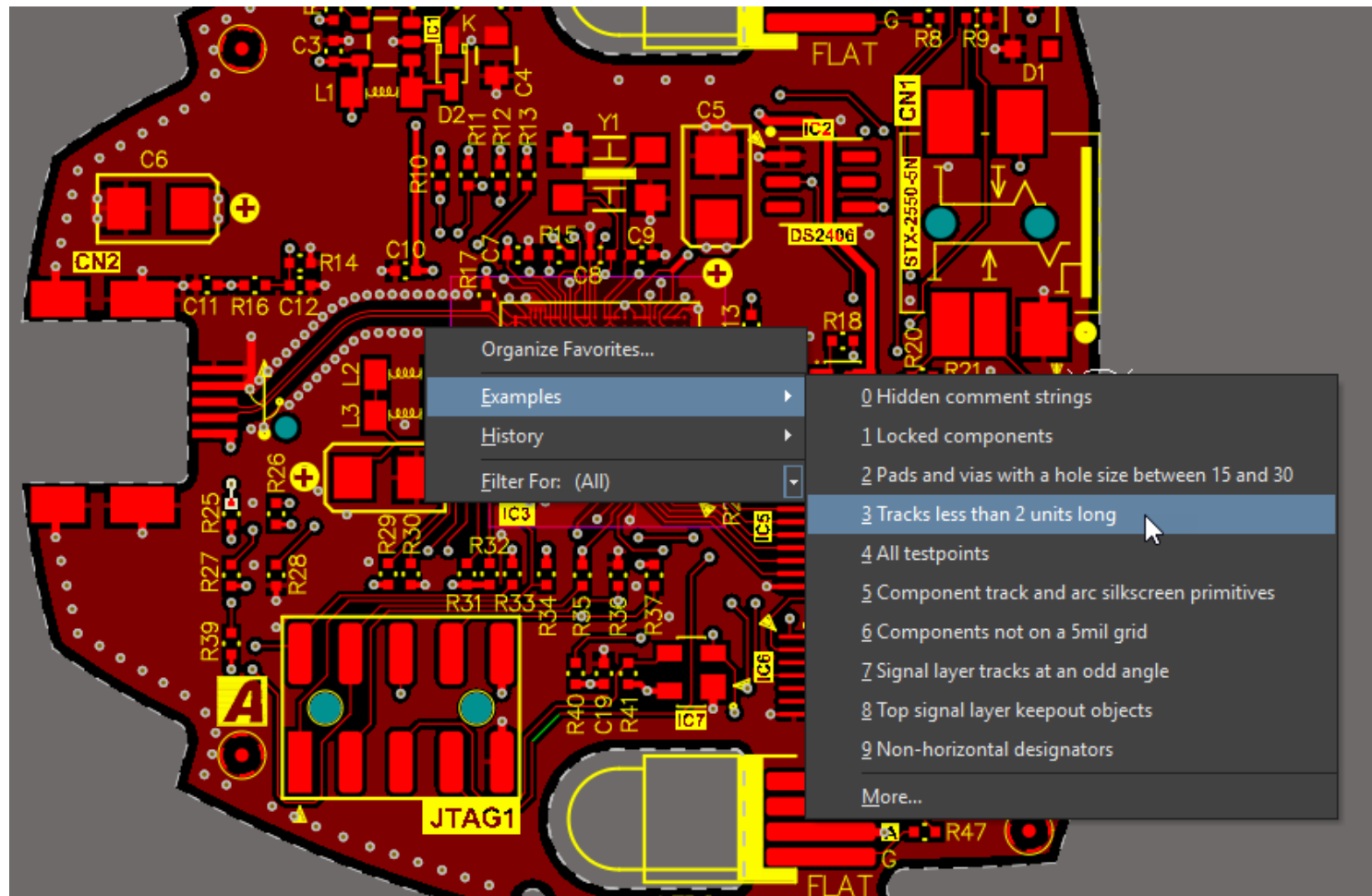


One more bonus tip...

This is an Easter egg that not many are aware of.

Press the 'Y' key in any PCB database.

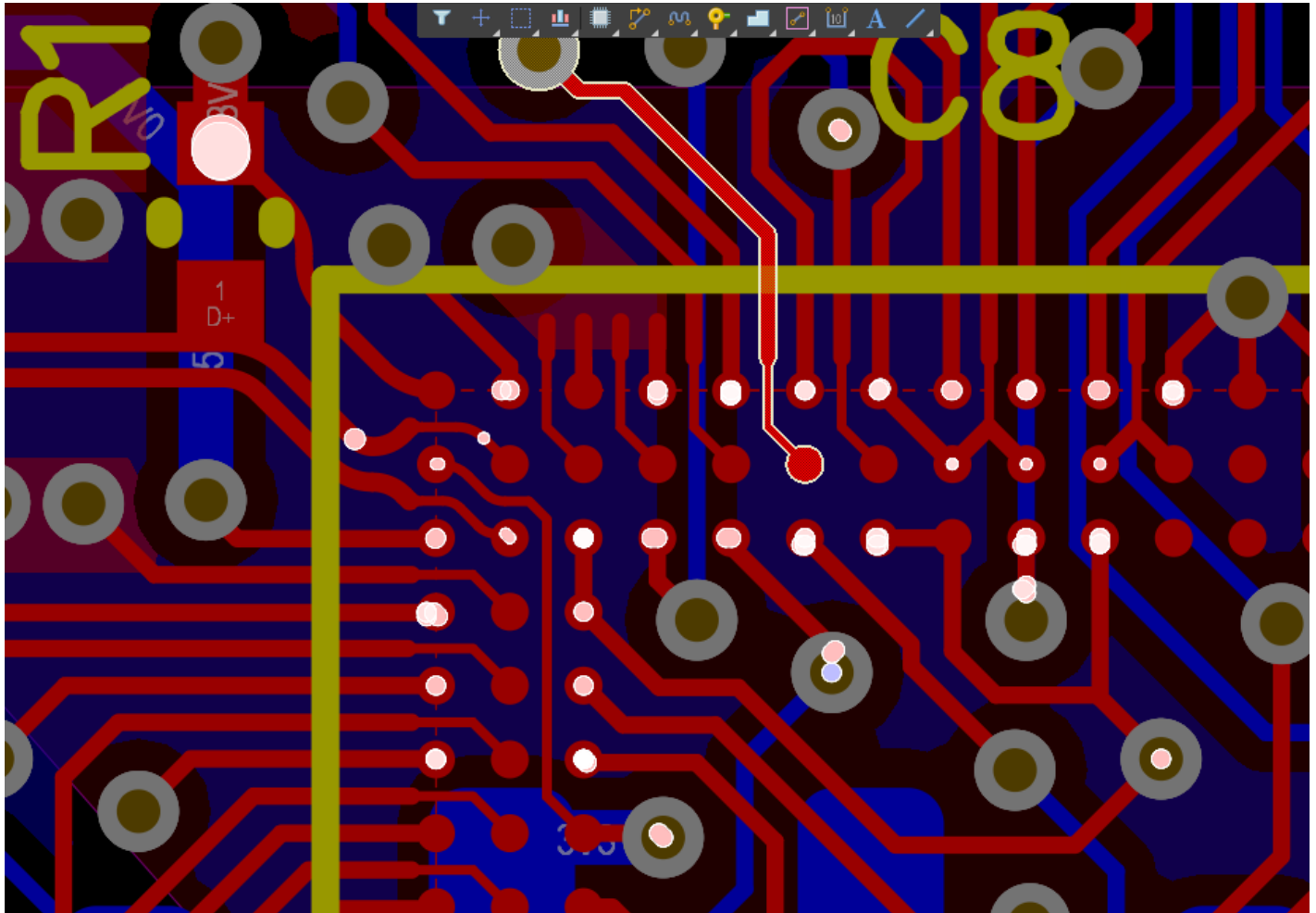
From the dialogue box that appears, select Examples, then option #3 as shown here.



One more bonus tip...

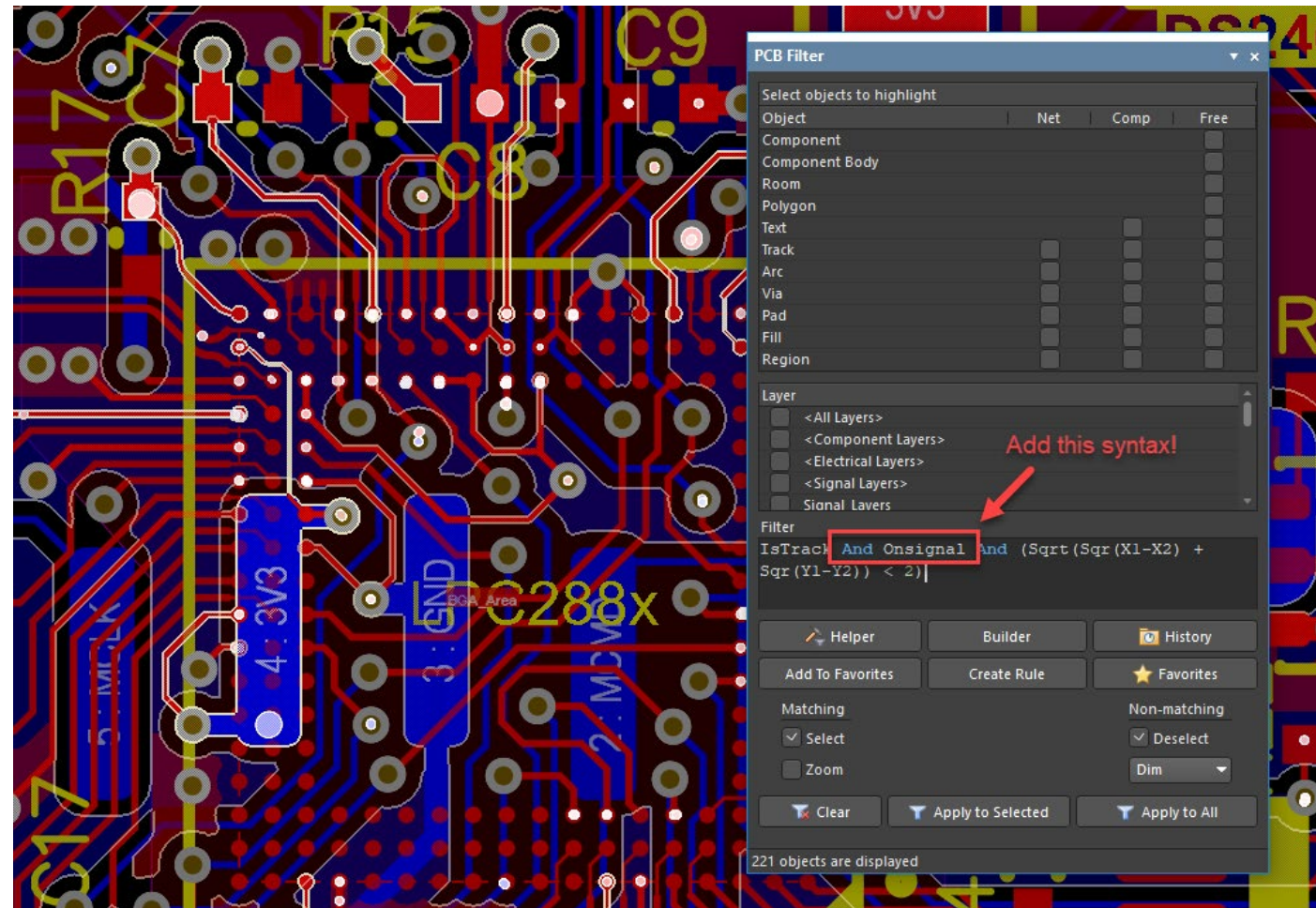
This command selects all those annoying little stubs that seem to accumulate in our PCB designs after routing.

While selected, you can press the delete key to eliminate these stubs!



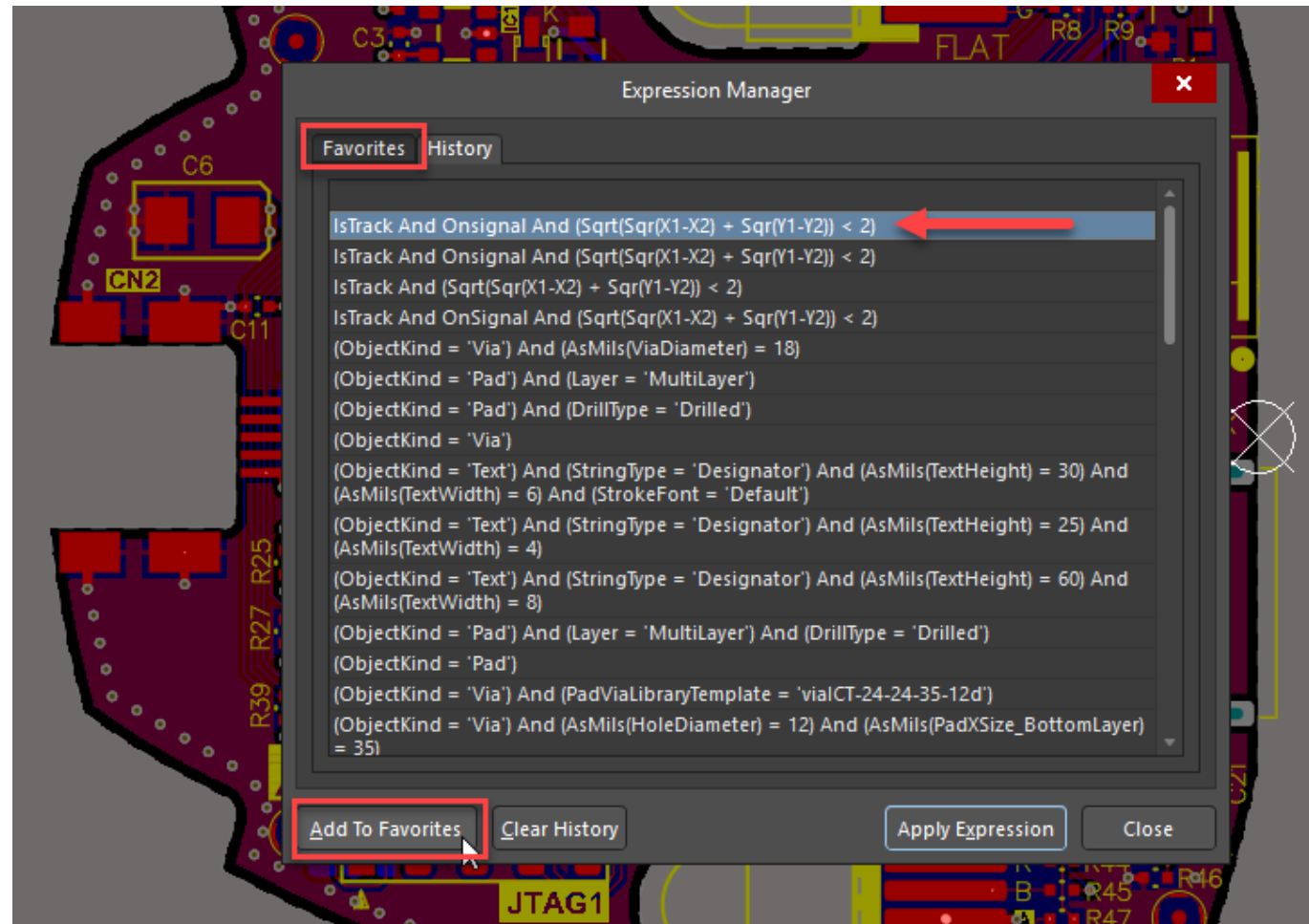
One more bonus tip...

I would suggest however, that you edit this command in the PCB Filter (as shown) so that it only selects those stubs on the signal routing layers.



One more bonus tip...

After executing this new command, press the 'Y' key again and this time select the History option and More... from the sub-menu. Then from the dialog box shown here, select the command and Add To Favorites!

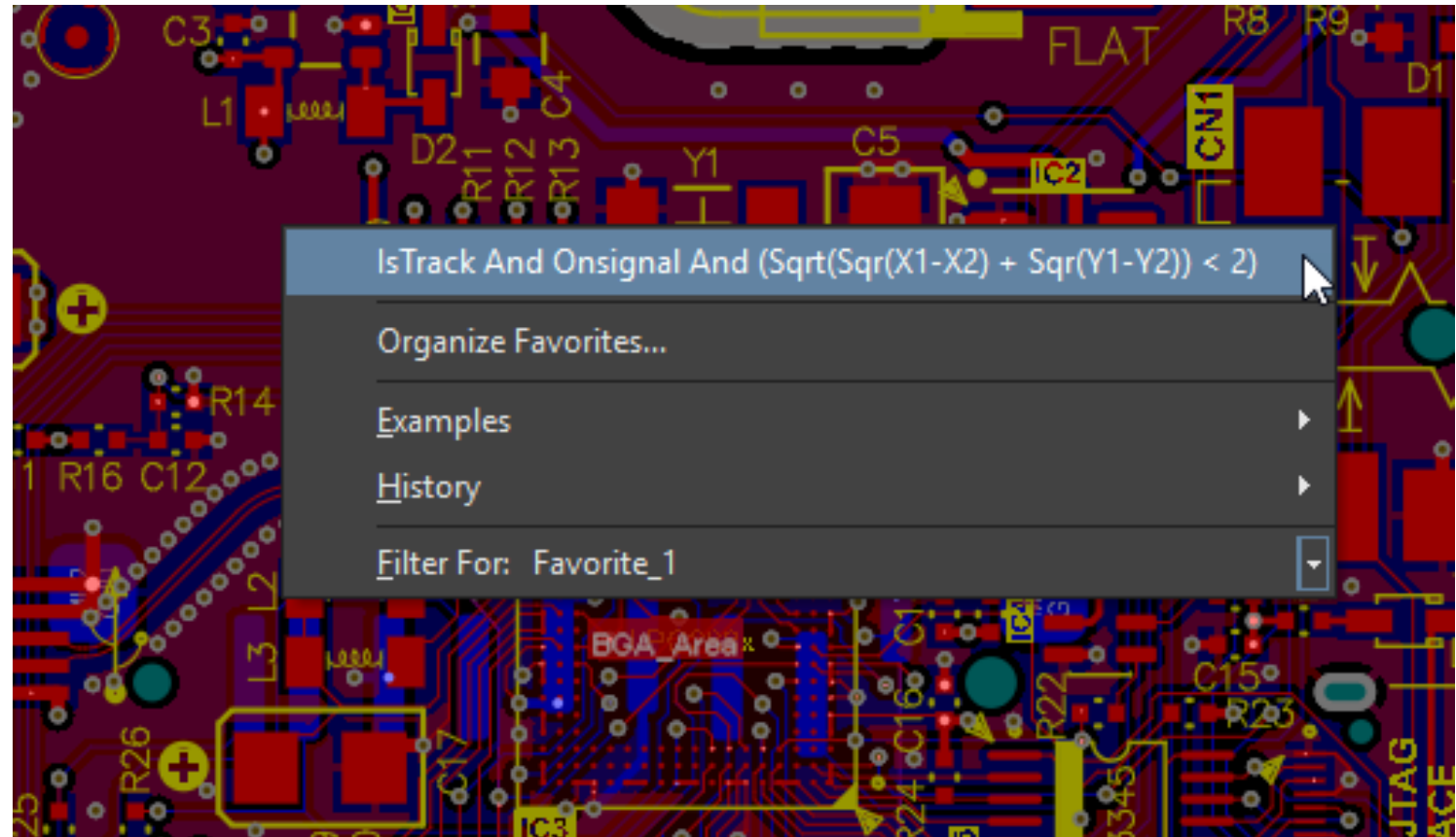


One more bonus tip...

Altium®

Now this short-cut command will always be available to you by simply pressing the 'Y' key!

Enjoy!



May all your PCBs be error free!

Altium®

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Email me if you would like a copy of
my design rule file or this slide deck.