Connecting to Embedded Components Using TLPS pastes in Via Layers

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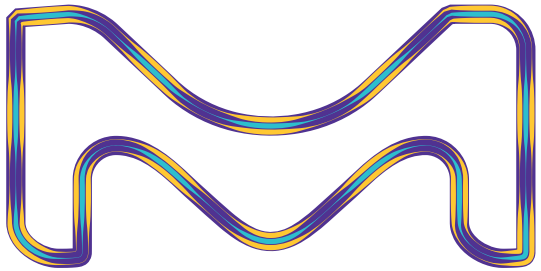
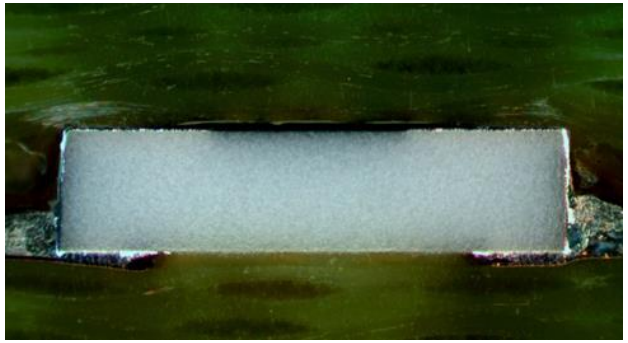
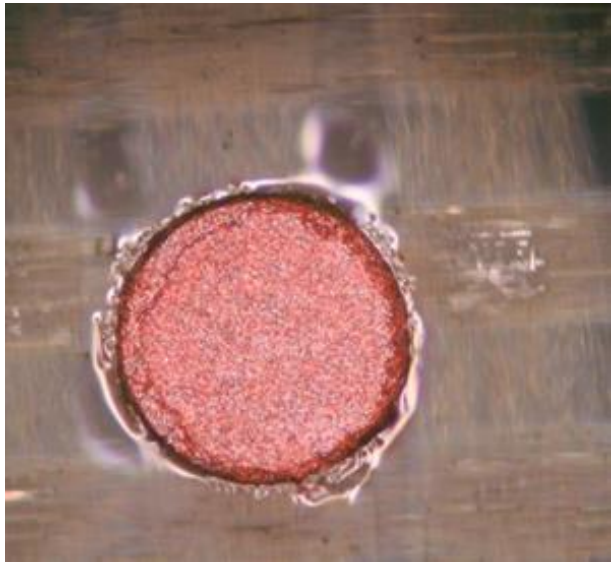
EMD Performance Materials



Introduction

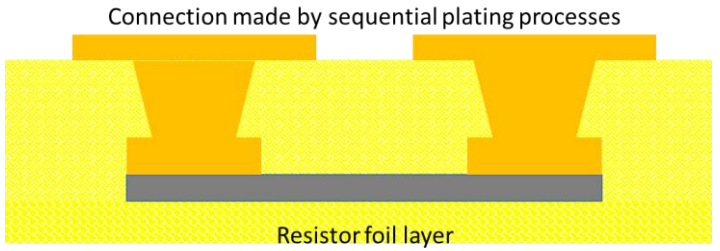
- Embedded passives have long been of interest
  - Freeing top-side real estate
  - Reducing parasitics
- The traditional methods for embedding passives has limitations
  - Embedded layer approaches can have multiple process steps
  - Layer approaches also have limitations in the values that can be achieved
  - It is difficult to embed discrete passives on multiple layers with conventional technology
- Filled TLPS paste vias have been successfully used to interconnect circuit layers in a parallel process
- The parallel-build approach with TLPS vias may provide a path to embedding discrete passives in multiple layers within a PCB
- A test vehicle was developed and an initial feasibility study was performed
- The results and future actions will be reviewed

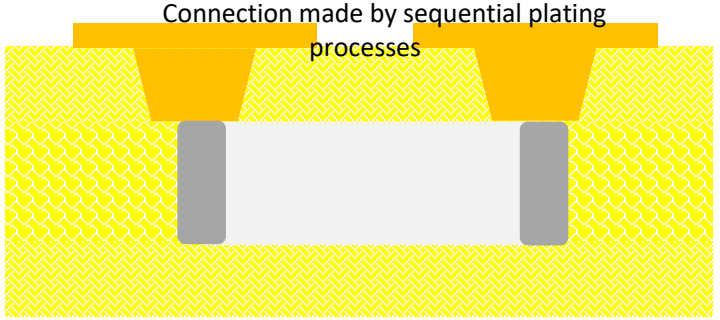




Traditional methods for embedded passives

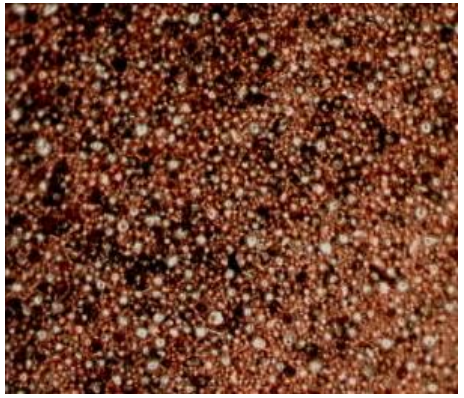
- Traditionally, embedded passives are incorporated into circuit boards by layer-type methods or by embedding discretes that are interconnected by plated-microvias
- In the layer method:
  - Embedded resistor foils are selectively etched and laser trimmed to achieve the desired values
  - For capacitance, there is a continuous layer embedded with limited ranges available
- In the embedded discrete method:
  - Each layer of embedded discretes requires a layer of plated microvia interconnect
    - Increases the thickness of the PCB
    - Increases the number of lamination cycles required

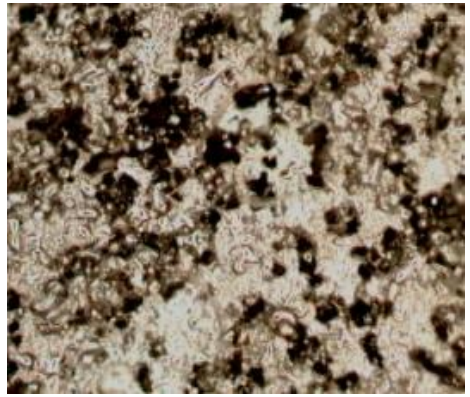


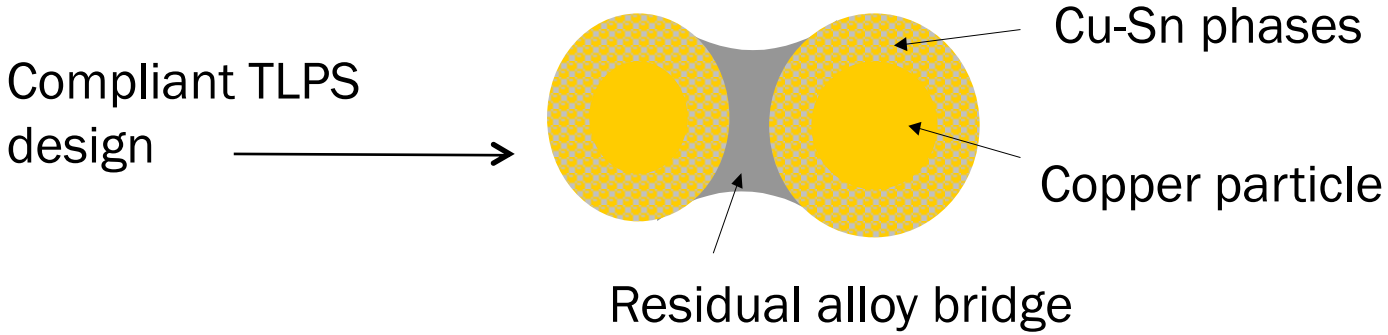


Technology definition: Transient Liquid Phase Sintering (TLPS)

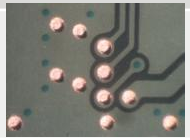
- Copper and tin-alloy particles in a flux mixture
- During a SAC-type reflow the tin-alloy melts and reacts with copper particles and solderable surfaces
  - *Inert environment required (N2, press, vacuum, reducing)*
  - *Pressure not required*
- Continuous metal joint after thermal process
  - *No remelt*
  - *Wide variety of rheologies available*
  - *Electrical, thermal and mechanical properties similar to solders*


Before reflow


After reflow

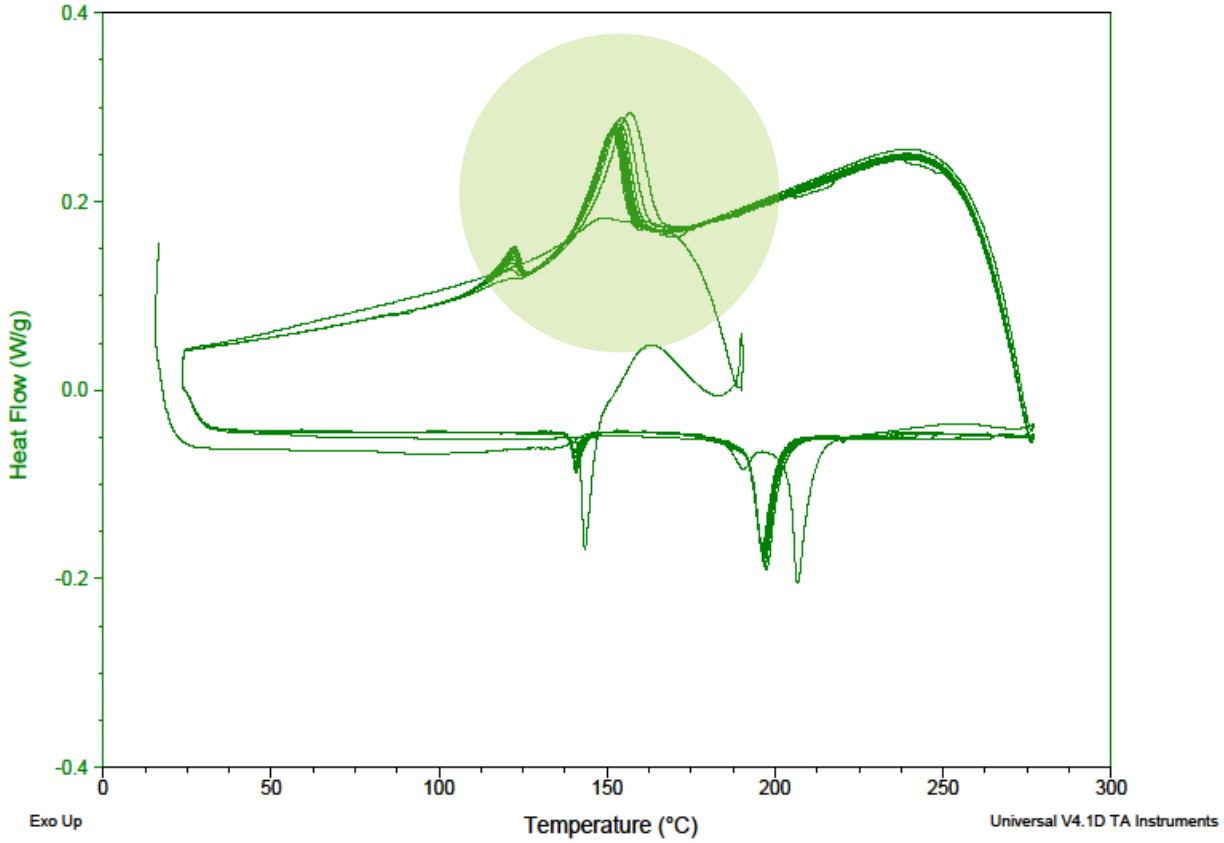


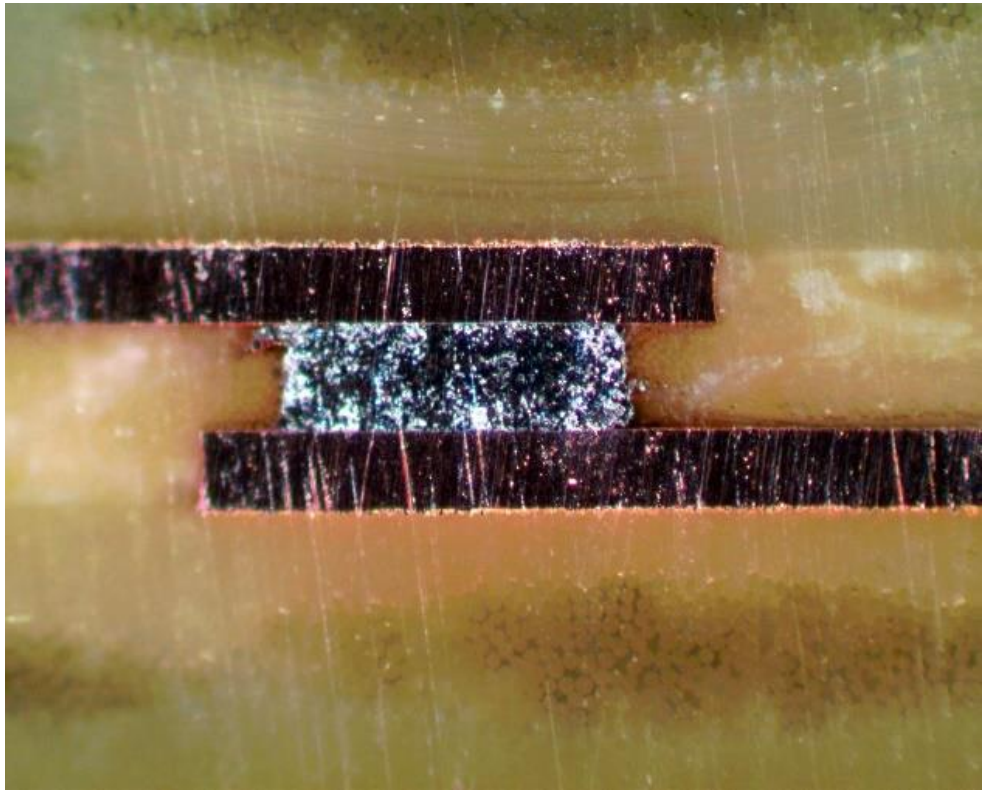
TLPS pastes in a variety of applications

Application	Image
Microvia fill	
Stenciled Interconnect	
Through hole fill	
X-Y Traces	
Component Attach	
Die attach paste	

TLPS pastes have been used for 20+ years in high reliability, high performance PCB applications

TLPS paste joints are highly reliable

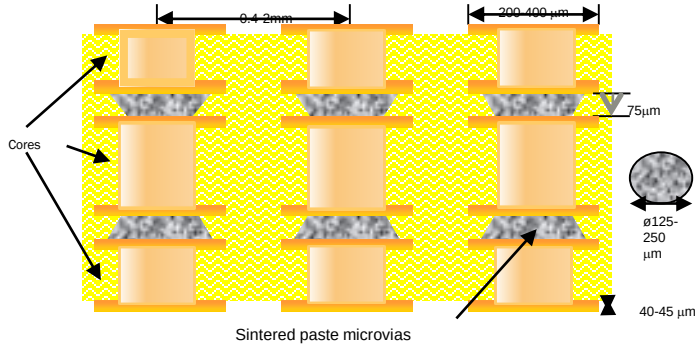


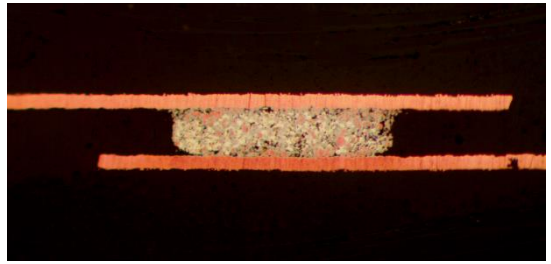


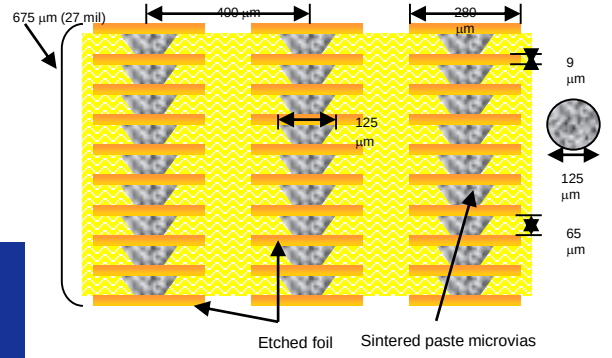
A ductile phase is built into the joint to manage the high CTE in the z-axis

When are TLPS vias typically used in PCB interconnect?

- Electronic devices require that high layer count PCBs are compelling Ormet targets
  - High end computing
  - ATE (test cards)
  - Military applications
- High interconnect density drives high-aspect-ratio PTHs
  - Complex drilling and plating processes,
  - Low yield by conventional processing
- Using TLPS paste breaks up high-aspect-ratio through holes
  - Manufacture subassembly 'cores'
  - Interconnect using paste via layers
  - Proven reliability and good yield
  - Simplified process = lower cost
- TLPS paste vias are a well established solution for the high end PCB market





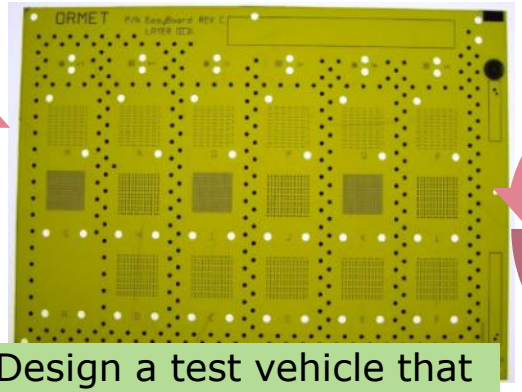


Better performance, shorter cycle time and higher yield than conventional technology for complex substrates

How was the TLPS technology for Z-axis interconnection developed?

Design formulation to satisfy initial key target characteristics

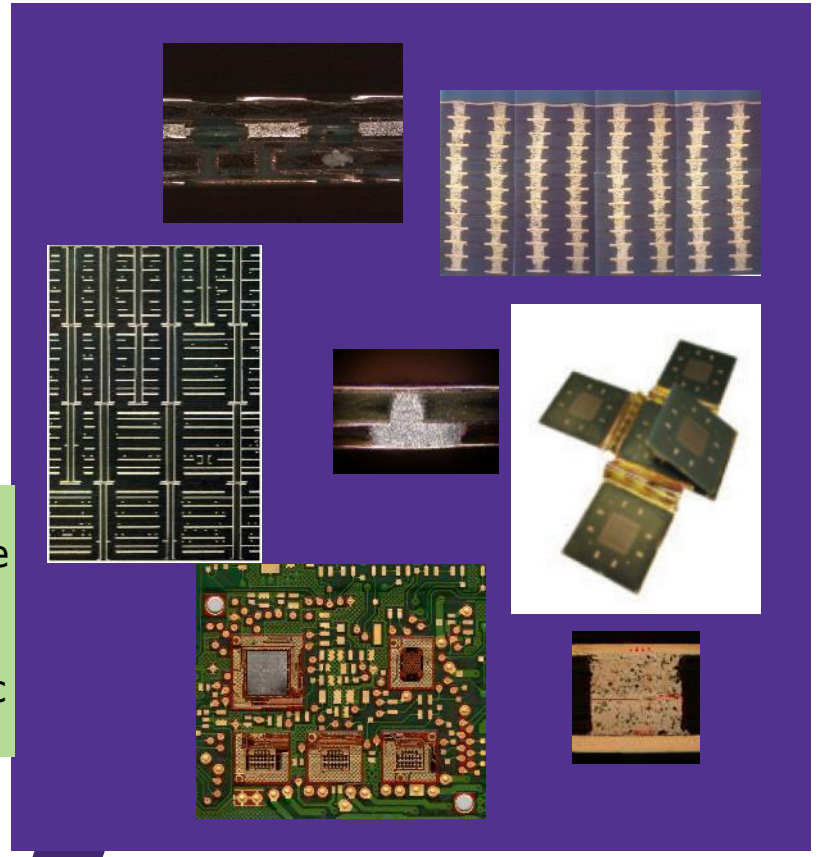
Iterate to clarify and meet key characteristics



Design a test vehicle that captures the key features of the application.

Do not drive development through disconnected materials properties

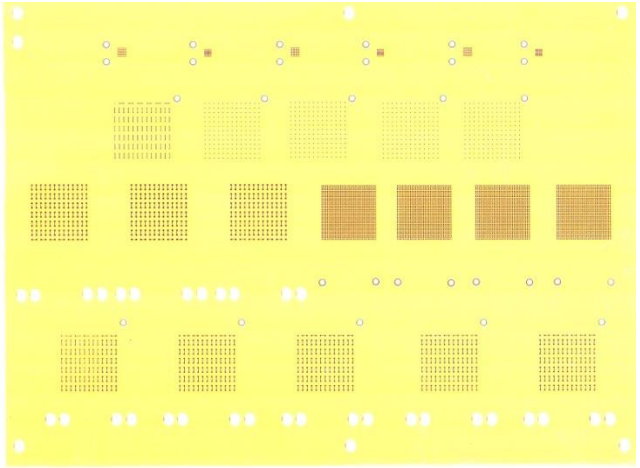
Adapt the test vehicle to resolve key implementation issues on specific applications



Work closely with customers to implement effectively in many different configurations

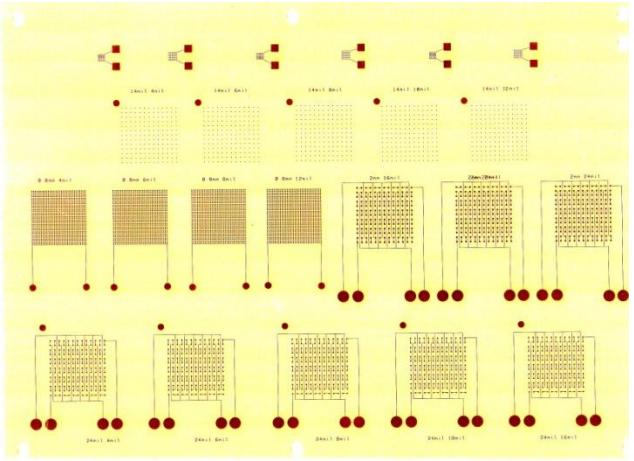
Collect and analyze data to refine key factors and develop improvements/best practices

A daisy chain test vehicle used for development of the TLPS paste via implementation



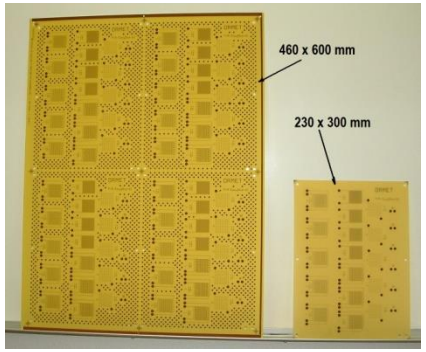
Layer 1 & 2

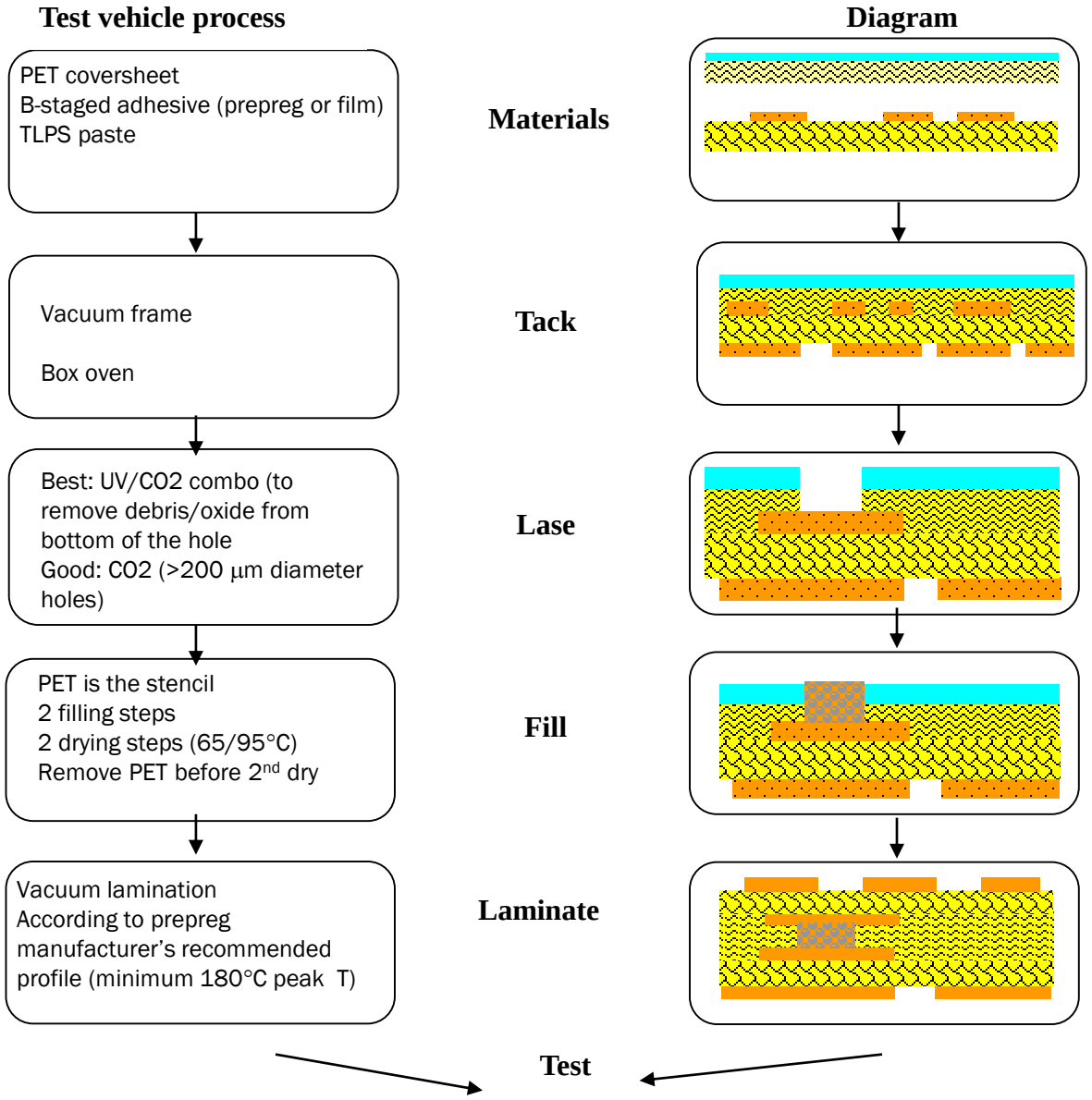
Filled microvia layer



Layer 3 & 4

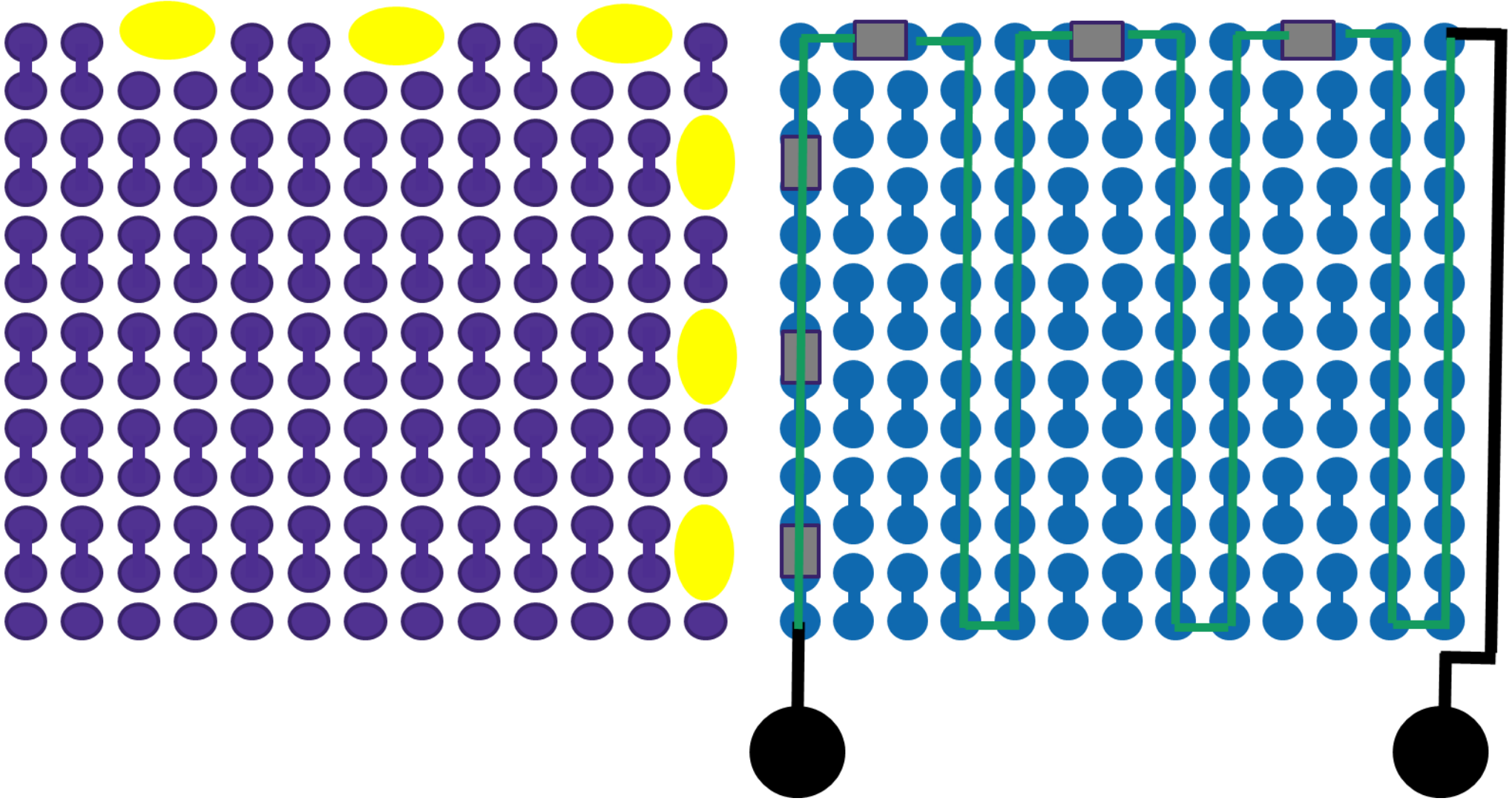
Standard 18” x 24” panel, 9” x 12” board →



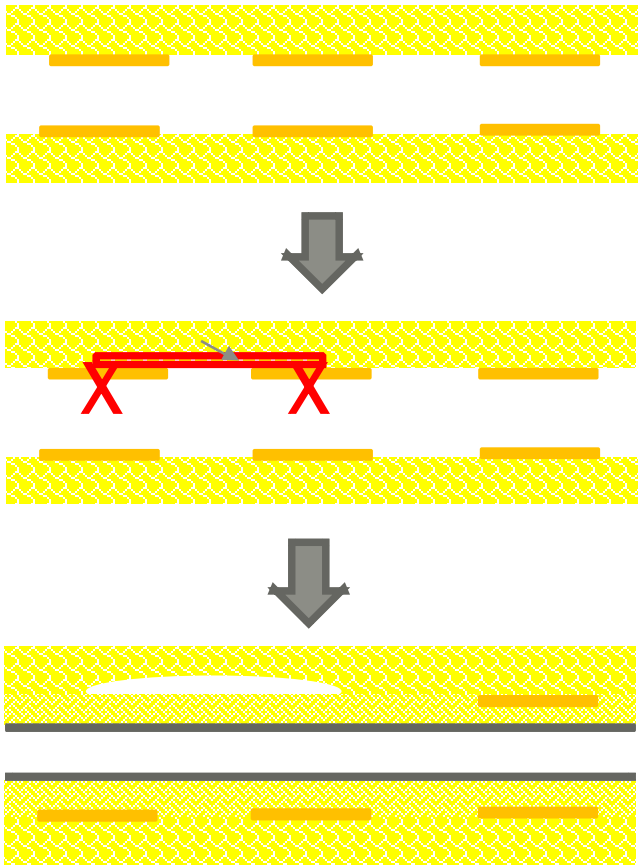


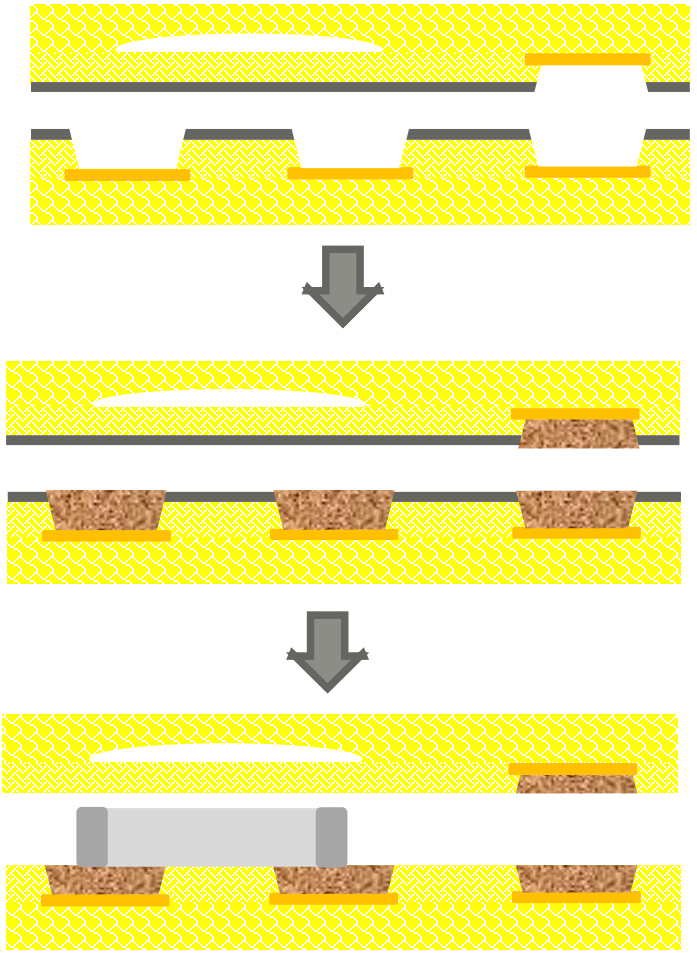
A typical process flow for implementing TLPS paste vias using the daisy chain test vehicle

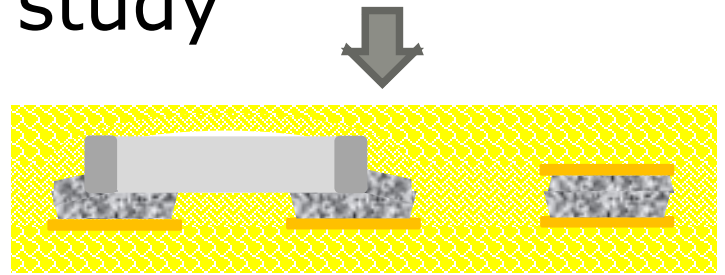
Modifications made to the daisy chain design



The process flow used in the initial feasibility study





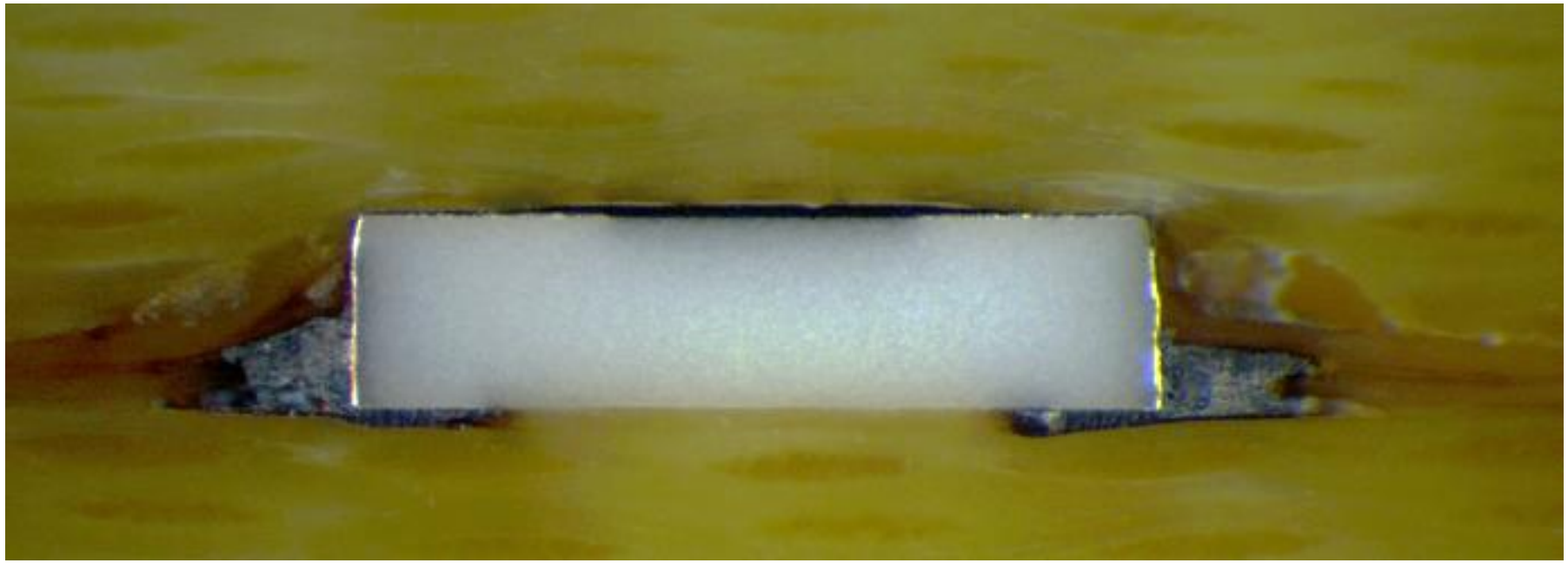


- Obtain cores
- Remove unneeded pads and route relief area for cap body
- Tack laminate adhesive and PET coversheet to both subs
- Laser ablate to accept paste via fill
- Doctor blade paste into openings and remove PET
- Place cap and laminate

- Issue: Relief cut insufficient and deformation around cap body

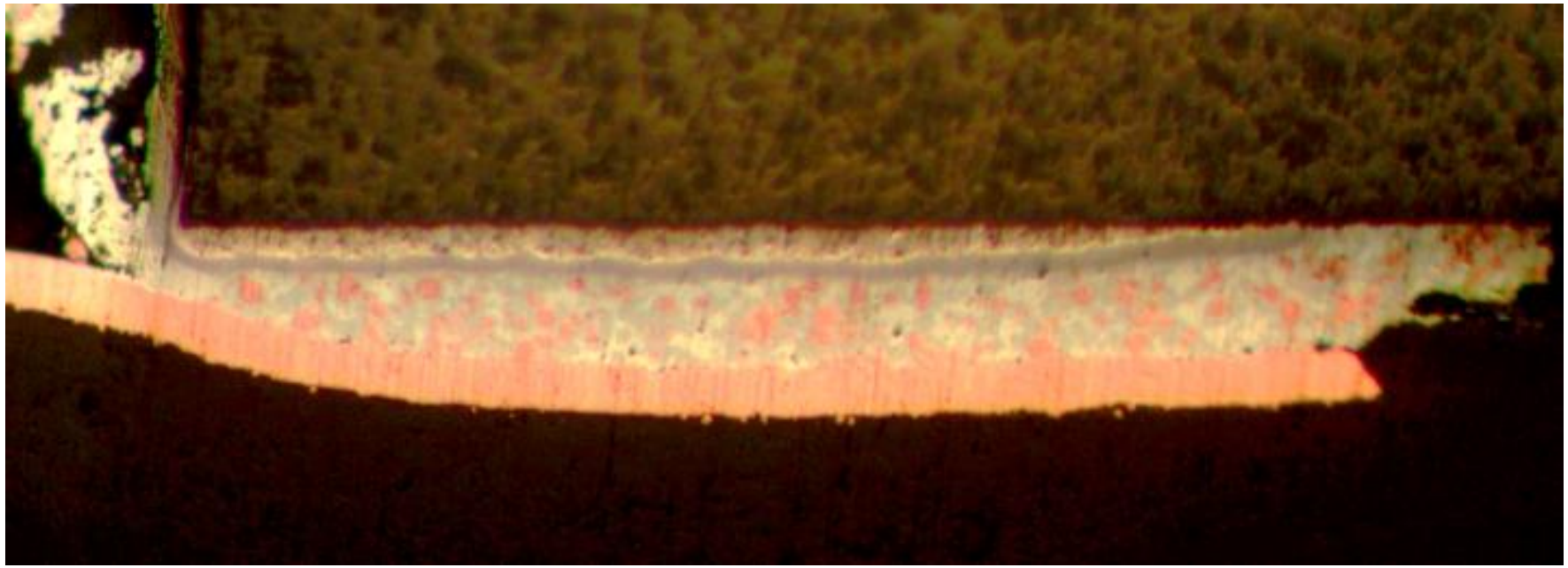
Discrete 0805 capacitors were successfully interconnected in the modified test vehicle

- Cross-sections reveal that good interconnects were formed
  - *The relief area provided for the cap body was insufficient resulting in a localized bulge*
  - *Some of the caps in the series-connected daisy chains cracked and therefore prevented electrical test*



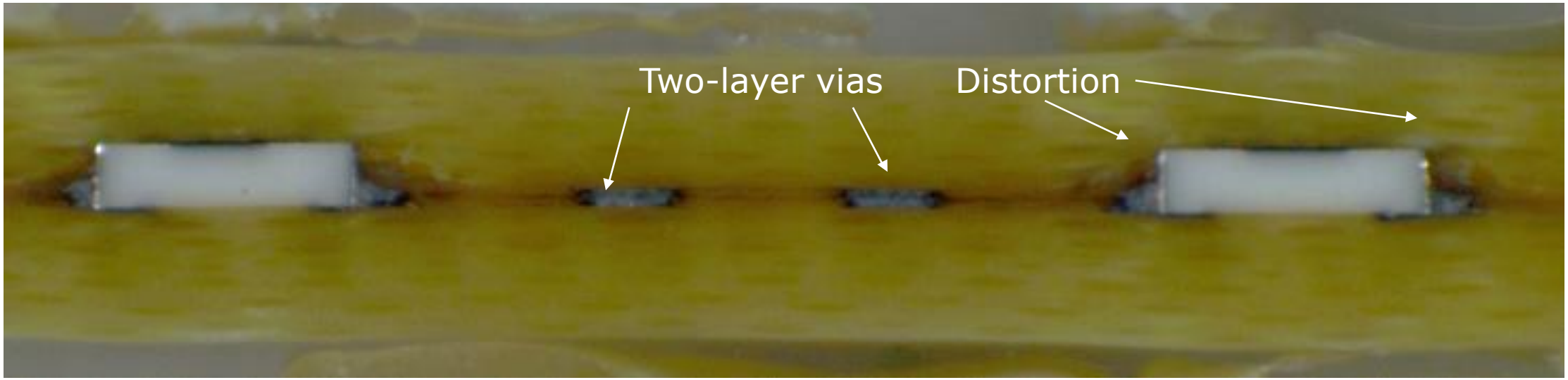
A solid metallic interconnect was formed by the TLPS paste

- A continuous metallic interface was formed at both the tin-plated capacitor termination and to the copper pad
  - *The copper pad has a standard oxide replacement treatment for adhesion to the prepreg*
- The metallic joint is nearly void free

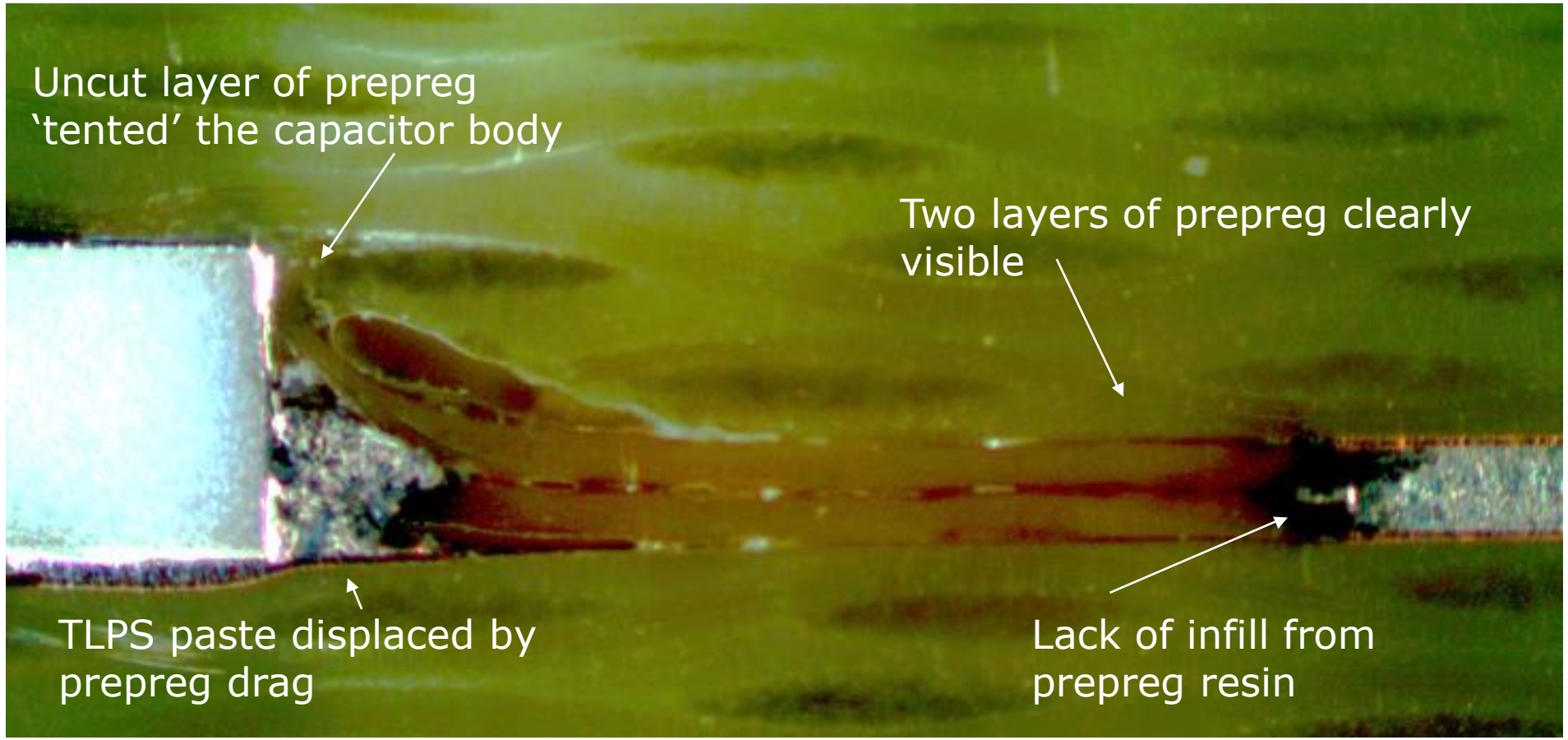


Z-axis interconnects between layers in the PCB were formed simultaneously with the capacitor interconnects

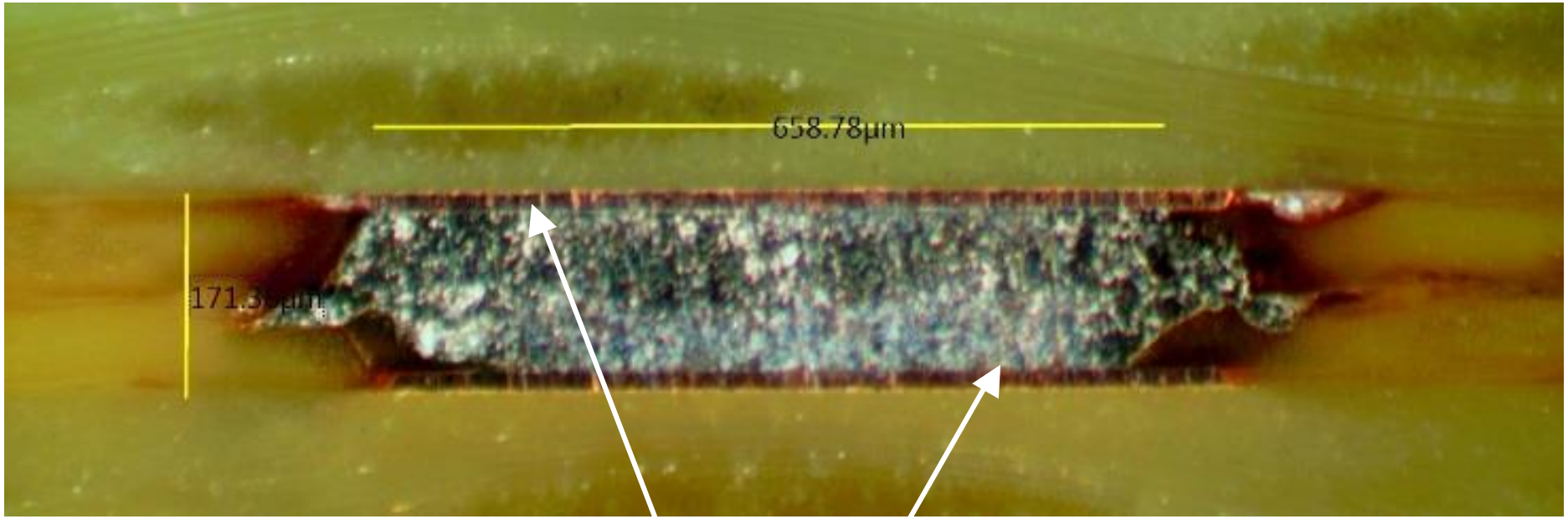
- Despite the localized distortion around the capacitor bodies, the nearby z-axis interconnects were successfully formed



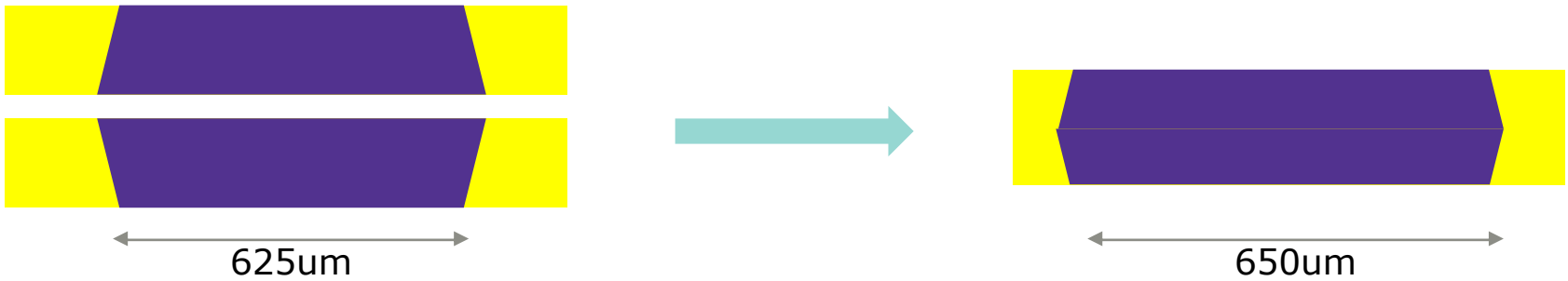
Despite the distortion and lack of in-fill of the prepreg resin, the TLPS joints maintained integrity and sintered well



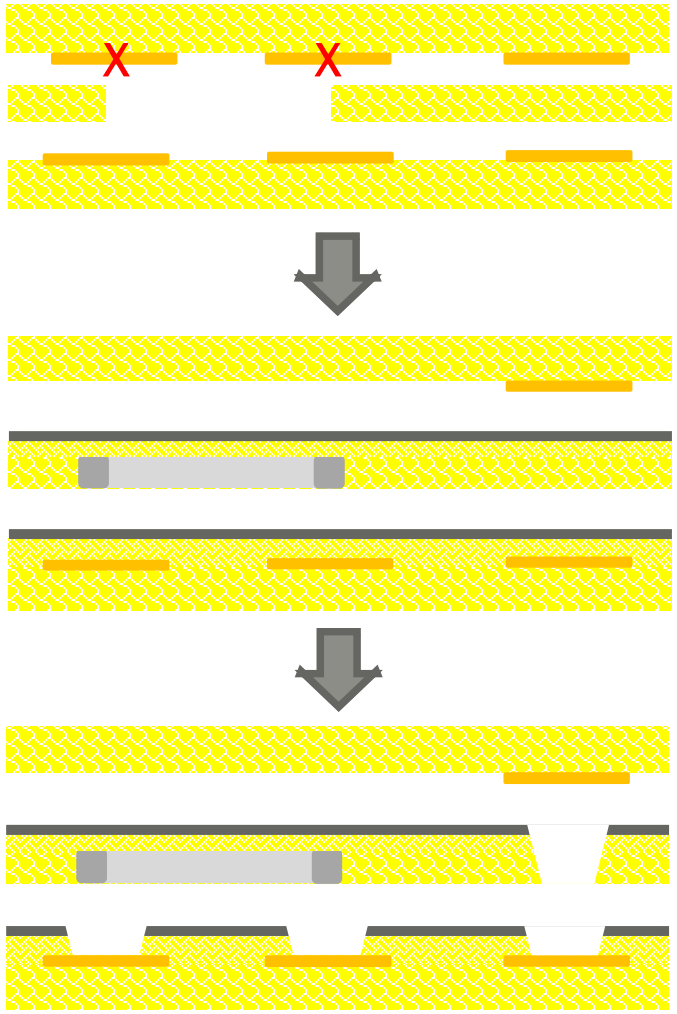
The TLPS paste installed into vias in opposing layers joined to form monolithic structures

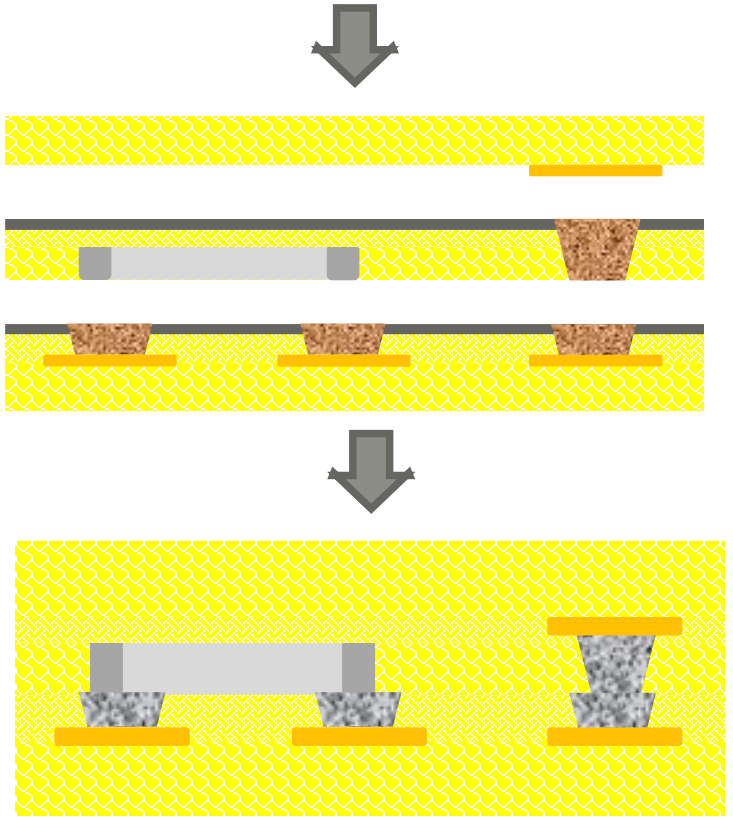


Good retention of via shape, consistent sintering throughout and to both interfaces



Next steps: Repeat the experiment with adequate relief for the capacitor bodies





- Obtain cores
- Remove unneeded pads on upper core
- Route a cavity in a thin interposer core to accept the cap
- Tack laminate adhesive and PET coversheet to the bottom sub and interposer (install cap to form a tack bond to the adhesive)
- Laser ablate to accept paste via fill
- Doctor blade paste into openings and remove PET
- Align and laminate

- Issue: Interposer core needs to be similar in thickness to the caps
- Issue: Will tack-bonded caps stay through handling processes of lasing, filling and lay-up?

Summary

- Embedded passives have long been desired in substrates to free up topside real estate and reduce parasitics
- Existing technologies to embed passives have limitations
  - *Layer types are cumbersome and provide only a limited range of values*
  - *Embedded discretes require a separate interconnect layer and exacerbate the sequential lamination problem*
- TLPS pastes interconnects have been used in z-axis joining operations for over two decades
- The use of TLPS pastes interconnects enables parallel fabrication
- The parallel fabrication strategy can potentially be used to incorporate discrete passives simultaneously with forming z-axis interconnects
- A feasibility study was conducted and simultaneous embedding of discrete passives and formation of z-axis interconnects was demonstrated
- Based on the results of the initial study, a refined embedding scheme has been proposed
- It appears feasible to use this type of methodology to embed discrete components

Thank You!