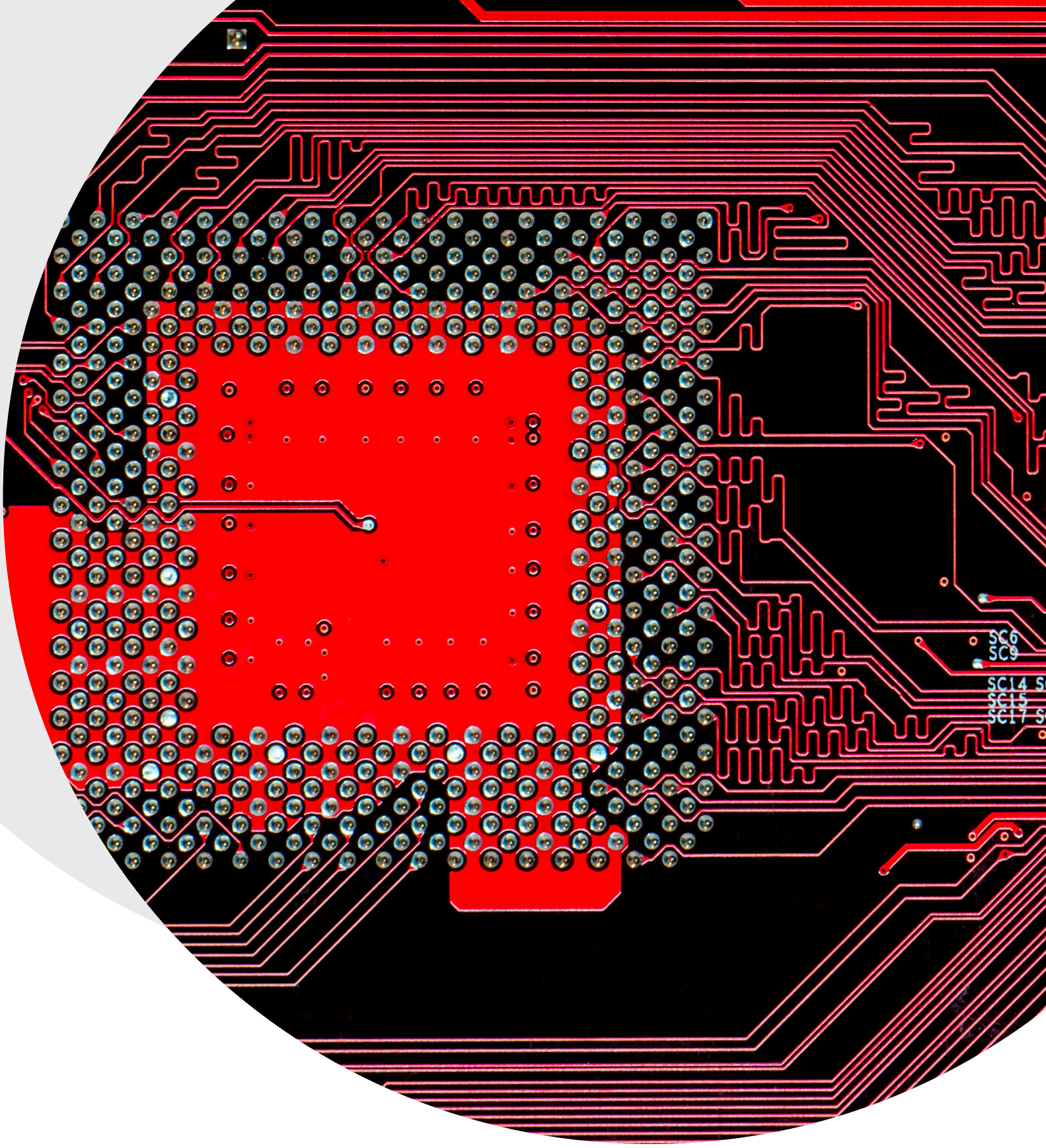

PDN Simulation and Analysis Guide

Fundamentals and Industry-Standard SimulationProgram

Altium®

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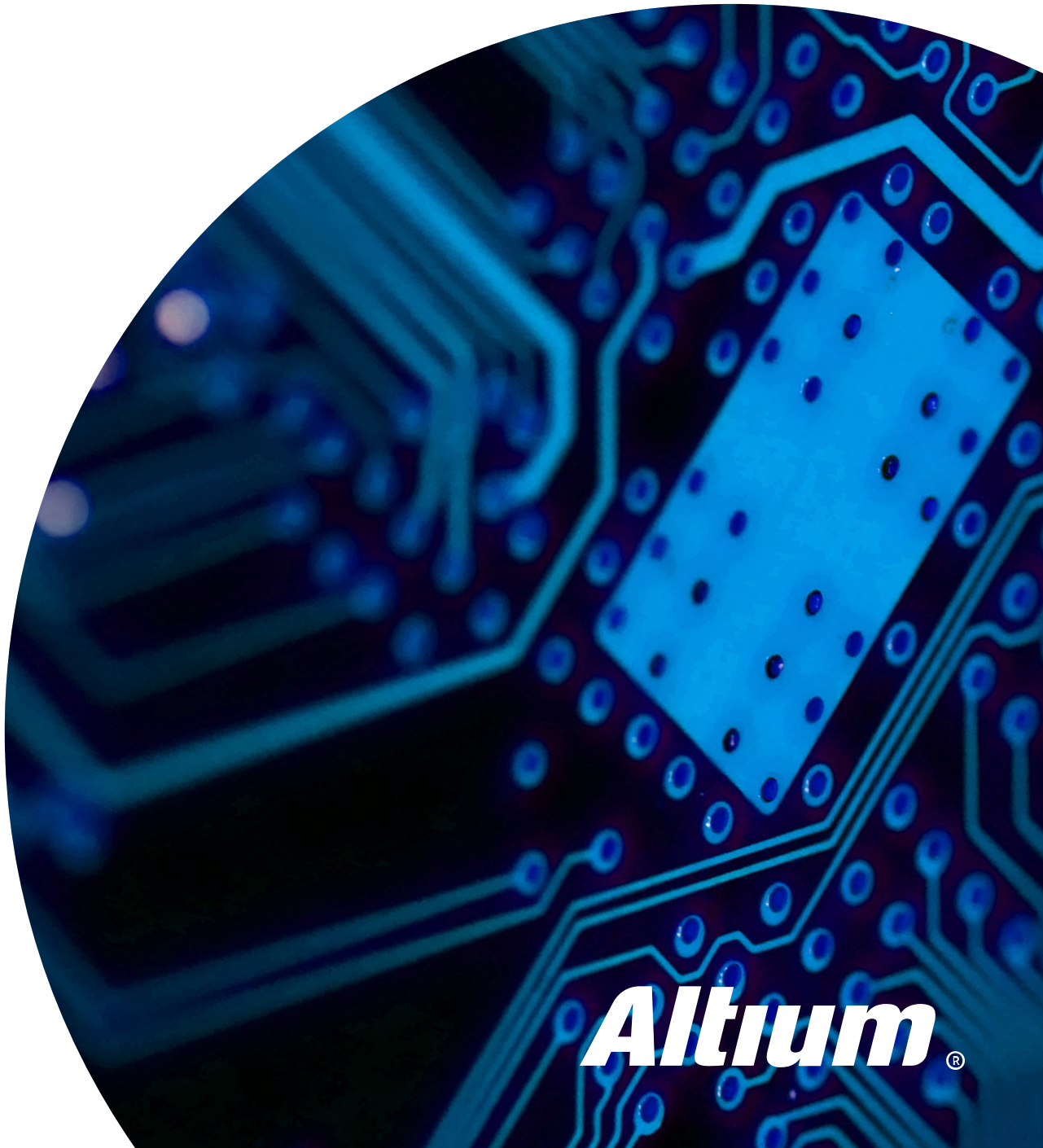
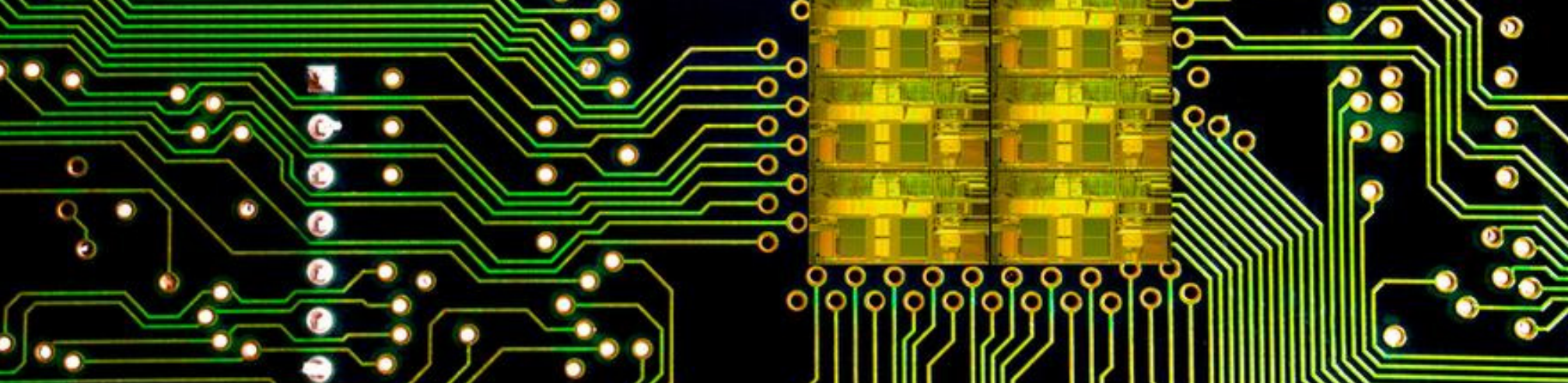




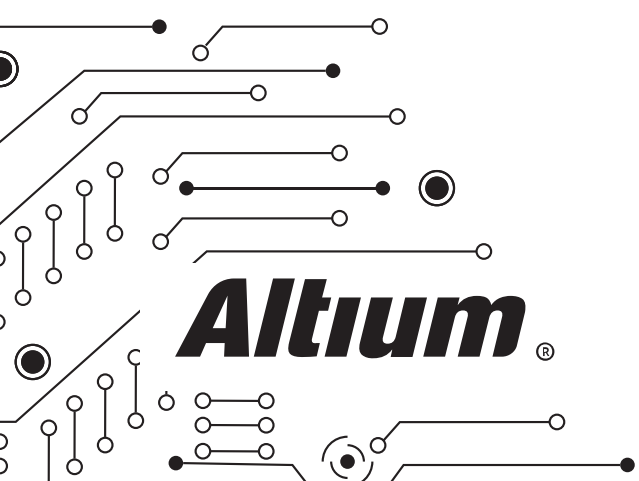
PDN Impedance Analysis and Modeling: From Schematic to Layout

Power integrity affects many performance aspects in PCBs, and ensuring power integrity in a digital design starts by ensuring the PCB layout has low PDN impedance. There are several basic aspects of PDN impedance and some basic design steps that help a designer reach relatively low PDN impedance in a PCB. Without low impedance, power glitches can cause components in a board to operate incorrectly due to large voltage swings on the power rail, which can then propagate to signals and appear as jitter along the rising or falling edges.

PDN analysis occurs in two regimes: the time domain and in the frequency domain. If you can build some reasonably accurate models for PDN impedance, you can then compare transient responses on the PDN with the power fluctuation limits in modern components. PDN analysis also occurs in the frequency domain, which will allow a designer to determine the signal bandwidths and power levels that can be supported in a digital or analog system.

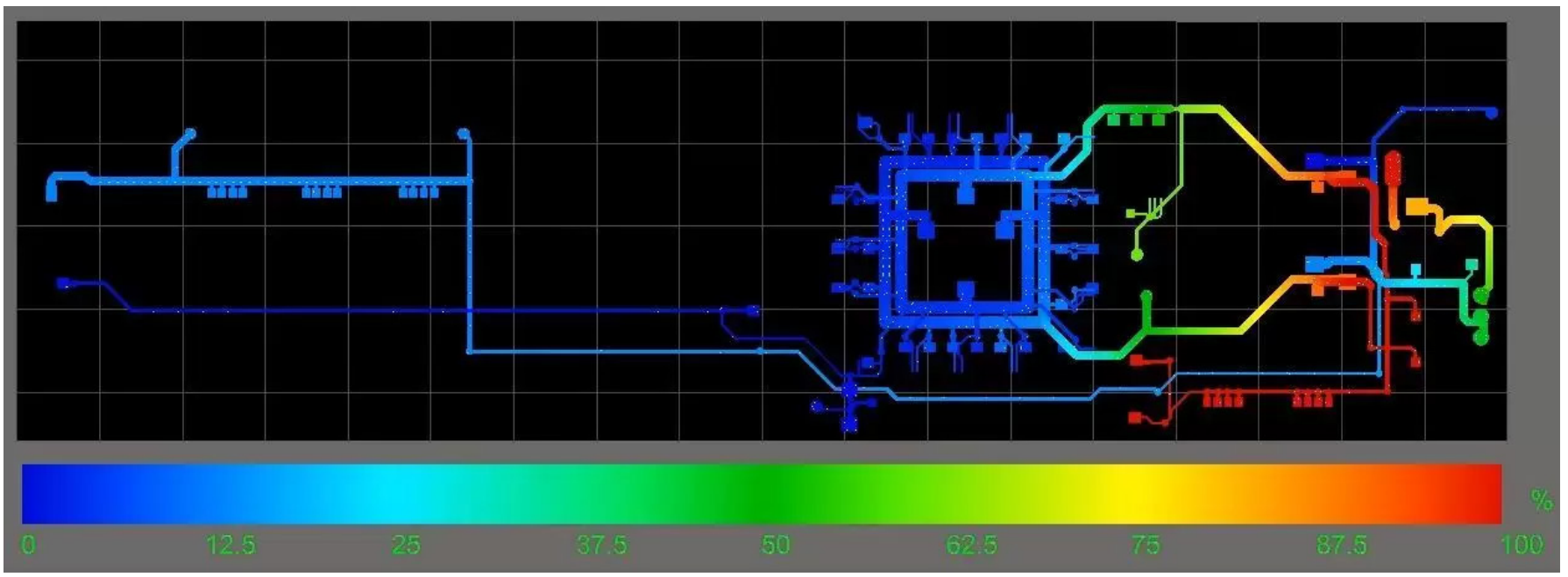
Why Conduct PDN Impedance Analysis?

The goal in designing the power delivery network in a PDN is to ensure DC and/or AC power can get to where it's needed. Power regulators have low-impedance output, thus we would want to create a low-impedance path that can supply power to load components on the PDN whenever power is needed. How power is delivered and dissipated depends on whether we look at AC or DC systems. High-speed digital systems and analog systems will have both components present in some region of the system, so we need to consider power integrity from both aspects.



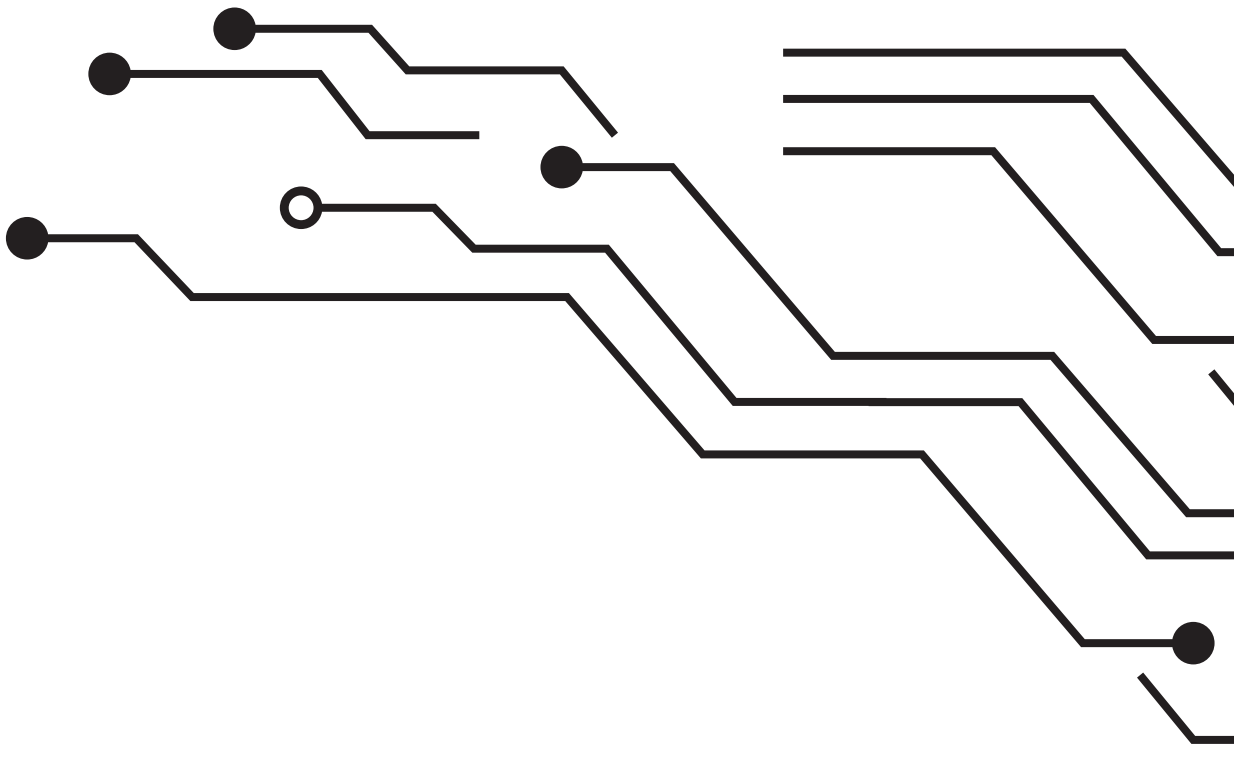
DC PDN Analysis

In DC systems with resistive components, power delivery is a relatively simple concept; power is dropped over a load based on the load's resistance. For this reason, DC PDN analysis generally only considers the resistive power loss (IR drop) throughout the conductors leading to loads in the PCB. This requires some calculations of current density in the planes and power rails used for power distribution, which can then be visualized as a color-coded map in the PCB layout.



Example DC PDN Analysis result showing where maximum and minimum power losses occur throughout the PDN.

DC PDN analysis is often ignored as part of digital systems design, but it is still important as modern digital systems supporting large ICs with many high speed IOs (such as FPGAs) will need to draw large bursts of current at any moment. To ensure noise-free power delivery, digital systems rely on AC power integrity analysis.



Why Conduct PDN Impedance Analysis?

Delivery of the AC portion of power is more complex and is prone to noise problems. In the past, with TTL components running at high core voltages (5 V saturation logic), it was possible to ignore many power integrity problems because the noise margins on logic circuits in these components were very large. Today's digital components generally run at 3V3 or lower core voltages with thinner noise margins and higher IO count.

In short, the AC PDN impedance will affect the following aspects of your circuits:

- **Power bus noise.** Ripple in the PDN voltage is created by transient currents in your PCB that interact with high reactive impedance at certain frequencies. Note that, because your PDN impedance is a function of frequency, the voltage ripple caused by a switching will also be a function of frequency. Note that these transients arise regardless of the level of switching noise in the output from your voltage regulator.

- **Damping in power bus noise.** The amount of resistance and loss in the dielectric laminate will determine whether ripple on the power bus appears as ringing (i.e., an underdamped transient oscillation) or whether it is overdamped. This is one problem that can occur if your decoupling capacitor is incorrectly sized or if you do not account for your decoupling capacitor's self-resonance frequency in your decoupling network.

- **Required level of decoupling.** Most capacitors can be insufficient for ensuring decoupling in PCBs with fast logic due to their relatively low self-resonance frequencies (~100 MHz to ~1 GHz). Therefore, designers use small-case/high-Dk capacitors (e.g., 0201 MLCCs) and interplane capacitance to provide sufficient decoupling.

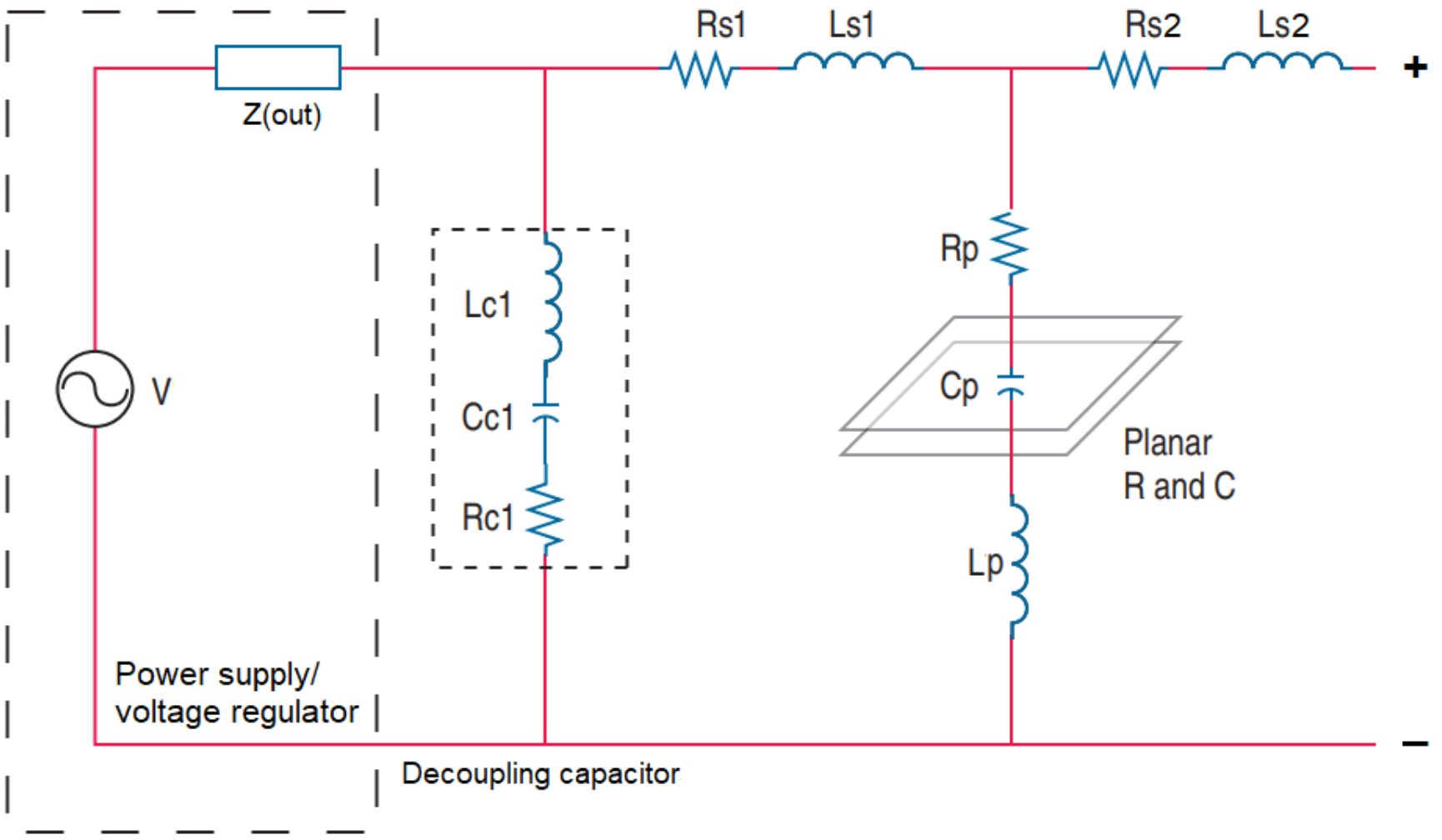
- **Current return path.** Your return current will follow the path of least resistance (for DC current) or least reactance (for AC current). The impedance in your ground network will vary in space, which depends in part on parasitic coupling between signal traces and the PDN. To create the tightest return current loop in the PDN, it is best to use planes to ensure minimal spreading inductance and maximum plane capacitance throughout the PDN.

- **Timing jitter.** Because signals have finite propagation time, the current burst drawn from decoupling capacitors and the regulator will take some time to reach a switching component. When a transient burst of current propagates to IOs, the transient fluctuation will interfere with the output signal, effectively creating some jitter in the rise time for your signal. In general, timing jitter due to power rail noise increases with noise intensity and the length between the regulator and the component. On large boards, RMS jitter might reach on the order of nanoseconds.

These problems can be reduced by routing power using plane layers, with power and ground planes placed adjacent to each other in the PCB stackup, and by using multiple planes in parallel. High-Dk laminates with lossy characteristics between plane layers are preferred, such as embedded capacitance materials. When plane pairs are included, it is important to understand how to model and simulate the effects of planes and decoupling networks on power integrity and the overall PDN impedance.

Circuit Models for PDN Impedance Analysis

You can model the impedance spectrum of your PDN and its transient response directly from your schematic, as long as you account for parasitics in your PDN. In the model below, you'll notice several circuit elements, but this model only contains two real components. The first is your power supply/regulator, which has some specified output impedance Z(out) and is typically an RL series. The second is the decoupling capacitor, which has an ideal capacitance of Cc1. The remaining circuit elements are parasitics. The Rs and Ls values are intended to model the inherent conductor resistance and parasitic power plane inductance, respectively. The Rp, Lp, and Cp elements account for parasitic coupling between power and ground planes (i.e., interplane capacitance).

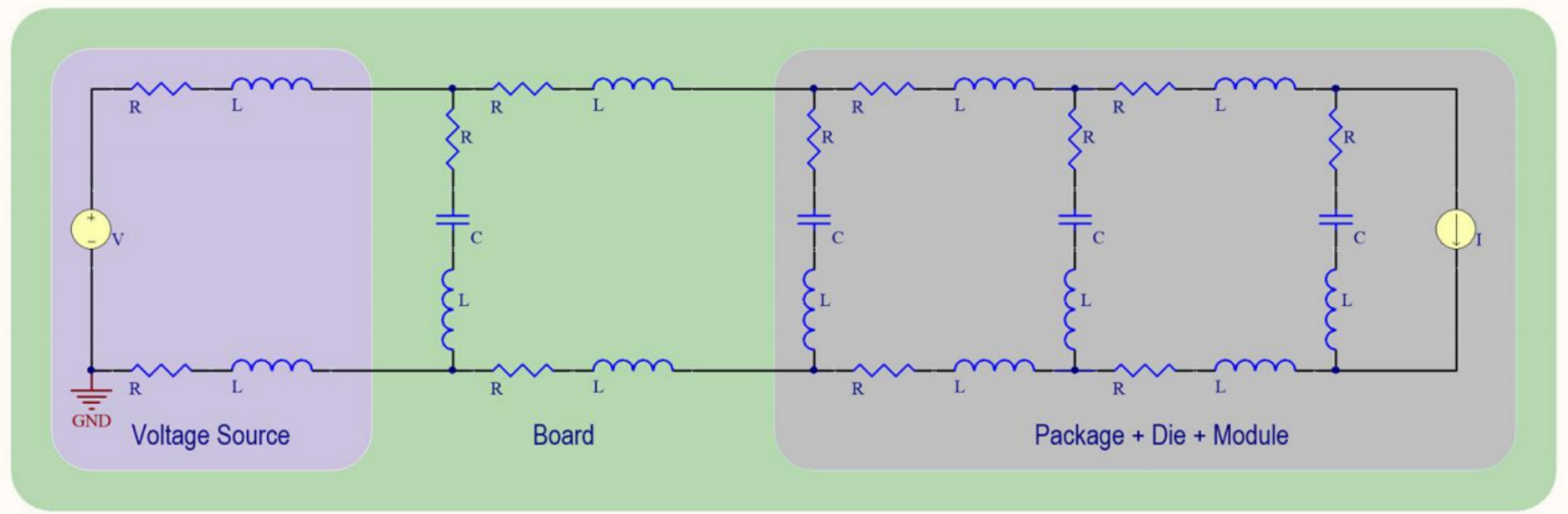


A simplified model for PDN impedance analysis. [Source]

The Lp element in the plane can be eliminated or greatly reduced by routing multiple supply/return vias into the plane pair. This is effectively what is done to supply power and ground connections to high pin count components, such as large BGAs that supply many high speed signals. Therefore, many PDN impedance models in SPICE will ignore this element.

Die and Package Parasitics

Hopefully, the astute designer has noticed that the contributions from package and die impedance have not been included in the above analysis as they are built-in to the load in the PDN. These also need to be accounted for in the PDN as they contain capacitive and inductive parasitics.



PDN model with package and die parasitics.

In a PDN simulation, such as in SPICE, we normally ignore the package parasitics because we care only about the voltage that reaches each the end of each rail in the PDN. If we want to start linking the PDN rail voltage to the behavior of the output, then we need a model for the package parasitics and the actual logic circuits that require power. For a PCB designer, insufficient die capacitance is overcome with a bypass capacitor between the PWR and GND pins on the package. The capacitance can be chosen by first looking at the frequencies of any poles in the PDN and targeting these with matching SRF capacitors.

Analysis Goals

Before analyzing this model, you need to determine or estimate the values of the various elements in your model. The decoupling capacitor values are easy; just get them from the datasheet for your desired capacitor. The interplane capacitance is also easy to roughly estimate; just use the dielectric constant for your substrate, the area of your overlapping ground/power planes, and the distance between them in your stackup, and you know the interplane capacitance Cp. The remaining R values can be calculated using your intended trace dimensions. The L values need to be estimated from the approximate loop inductance for each portion of the circuit; these values are generally on the order of pH to a few nH.

Your goal in analyzing this model is two-fold:

1. Determine the impedance between the + and - terminals on the right side as a function of frequency. This can be done with a simple frequency sweep.

2. Check that the PDN impedance is less than your target impedance. One simple wat target impedance is calculated using the current a switching IC will draw into the PDN and the allowed voltage ripple:

$$Z_{target} = \frac{(V_{supply}) \cdot (ripple\%)}{I_{transient}}$$

An equation for estimating target impedance.

3. Examine the behavior of transients by adding a current source in parallel with the power supply output (put the positive terminal before Z(out)). Set the current source to supply a delta-function impulse with total charge Q shown in the equation below, or to supply a stepped current. This would effectively tell you the amount of total capacitance needed to provide a burst of current to a switching IC.

$$Q_{impulse} = (I_{transient})(t_{rise})$$

Impulse magnitude you can use to simulate the transient response in your PDN.

4. Check that the lowest-frequency structural resonance is greater than the bandwidth required by your switching ICs. The idea is to minimize ripple and EMI over the broadest possible frequency band.

Note that point #3 is intended to model the transient response due to downstream switching ICs. If you have 10 ICs that will switch simultaneously and they all draw the same transient current into the PDN, then your impulse magnitude will be a factor 10 larger, and your target impedance needs to be a factor 10 smaller for a given ripple voltage. Once you've examined these three points, you can move on to interpreting your results and determine what design steps you can take to suppress power fluctuations in your PDN.

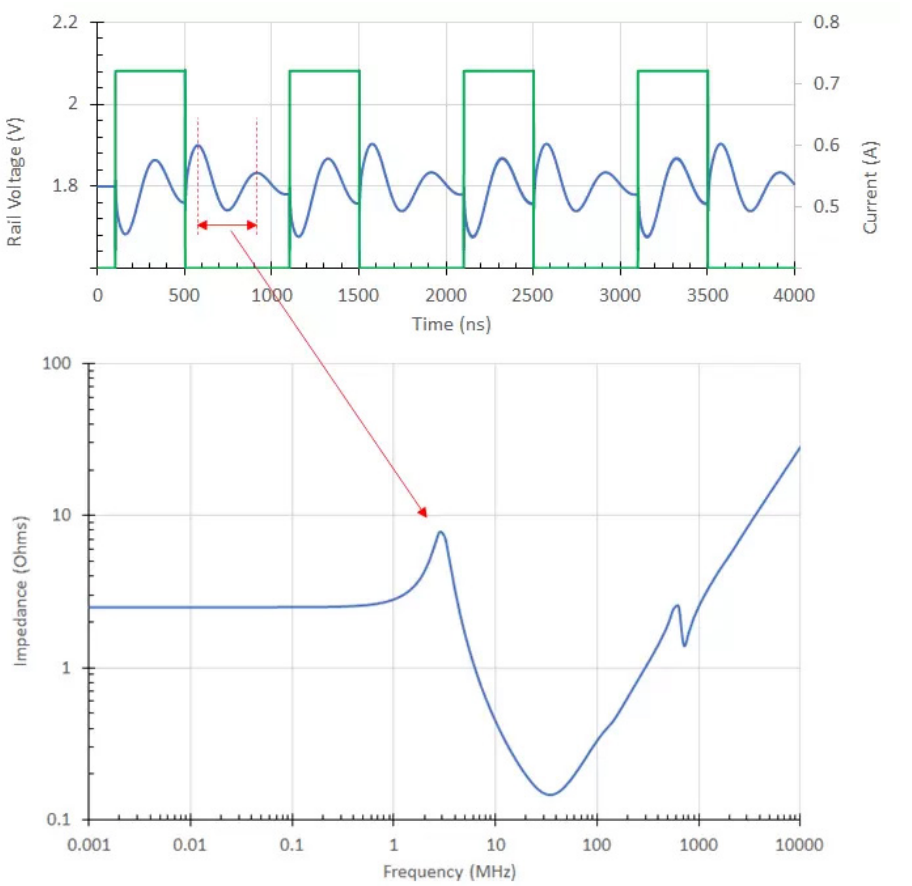
How to Interpret Your PDN Impedance Analysis Results

SPICE simulations in the schematic are the first step in analyzing the effectiveness of the PDN in a PCB. Different data should be extracted and analyzed in each domain; Points #1-#3 above can be examined in the schematic or the PCB layout, but Point #4 can only be accurately determined in the PCB layout.

SPICE Results From Circuit Models

Regarding Points #1 and #2 above, you can use SPICE to check that the PDN impedance is less than the target impedance at all frequencies up to some maximum bandwidth (for digital signals) or within the relevant frequency range you'll be using (for analog signals). If this is the case, and you have calculated your impedance based on the case where every IO switches simultaneously, then your PDN has a greater chance of working as intended without any resulting signal integrity problems.

Point #3 can be examined by simulating the transient response in your PDN. Specific peaks in the impedance spectrum are poles in an LTI system, and these will appear as an underdamped oscillation in the transient analysis results. If the transient response is underdamped, then you need to bring this oscillation into the critically damped/overdamped regime, or you need to set these poles to low impedance with a specific capacitor value. This requires using a larger decoupling capacitor, or using a capacitor with lower effective series inductance. Your decoupling capacitor should be sized to provide the impulse charge listed above, but you can certainly try to use a larger decoupling capacitor in order to change the conditions for the lowest PDN resonance so that the transient response is overdamped or immeasurably small.

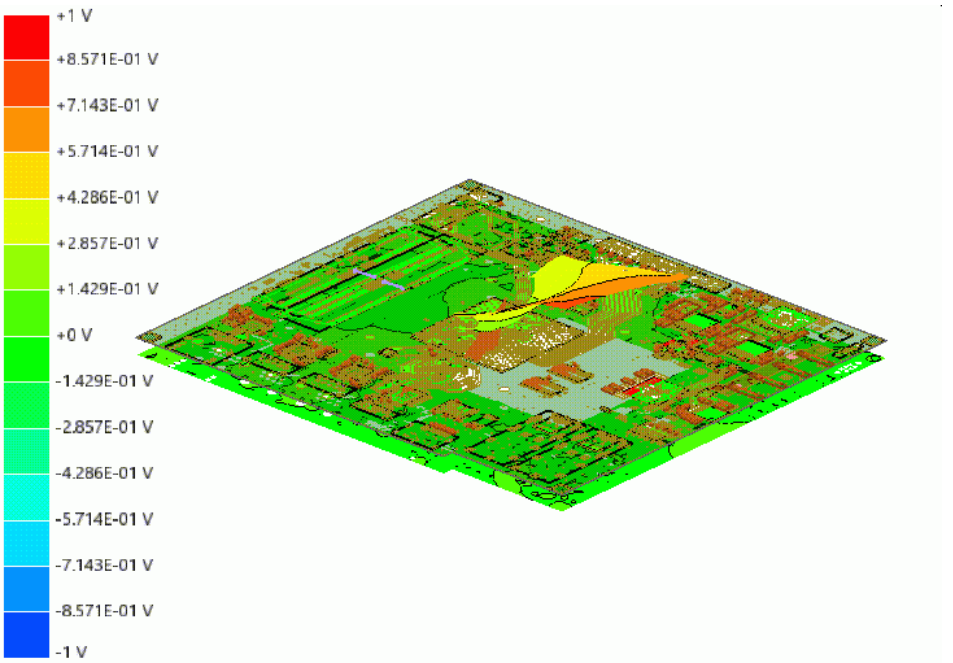


The transient response on the PDN can be linked to impedance peaks in the PDN.

In addition to the decoupling capacitor sizing and self-resonance issues mentioned above, the results from point #3 should illustrate why interplane capacitance listed as a requirement for properly decoupling ICs with 1 ns or faster logic. Aside from using very large decoupling capacitors with very high self-resonance frequencies (these are available on the market), placing the ground and power planes on adjacent layers was historically about the only way to provide the required level of decoupling in a PDN. Note that, whether you increase the interplane capacitance or decoupling capacitance by using multiple capacitors, making this capacitance sufficiently large will bring the transient response into the overdamped regime, effectively eliminating it.

Post-Layout Results

Point #4 must be examined from the PCB layout because it depends on wave propagation. The plane arrangement in a PDN can act like a large patch antenna that becomes a source of EMI when supplying transient bursts of current. The switching action in the PDN could excite resonances leading to strong emission from the board edge. This requires, at minimum, a 2D frequency domain field solver to simulate wave propagation within the interior layers of the PCB and subsequent near-field or far-field emission.



EMI identified in a PCB layout using Ansys SIwave.

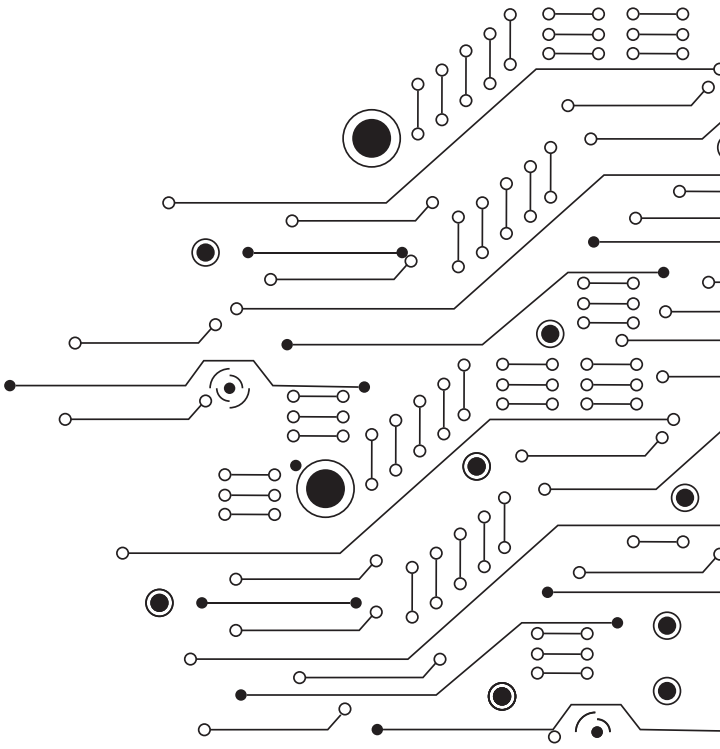
When certain regions of the PDN are found to resonate strongly, it indicates the PDN impedance in that region may be very high. Therefore, you would want to decrease the impedance in this region, either by adding more capacitance, or by identifying and fixing some high impedance element in the PCB layout. This can be as simple as eliminating a return path discontinuity in the PDN.

With the powerful PCB design and analysis tools in Altium Designer®, you can analyze all aspects of your schematics and layout, and you can identify signal integrity problems that can arise in complex PCBs. These tools are built on top of a unified rules-driven design engine, allowing you to perform important DRCs throughout the design process. You'll also have access to a complete set of manufacturing planning and documentation features in a single platform. When you're ready to send your design to a collaborator or to your manufacturer, use the Altium 365 platform to share your design files and stay productive.

What Target Impedance Should You Use in Your PDN?

A number of us on this blog and in other publications often bring up the concept of target impedance when discussing power integrity in high speed designs. Some designs will be simple enough (and slow enough) that you can take a "set it and forget it" approach to designing a functional prototype; as long as you follow a few general guidelines, power integrity is generally assured and the design can be fine-tuned to bring it to production level. For more advanced designs, or if you're fine-tuning a new board that has existing power integrity problems, target impedance is a real consideration that should be considered in your design.

One question I've been asked is simple, and yet it's overlooked by so many of us who write about power integrity: what should the target impedance be for a particular design or component? It's a fair question, and some SI/PI guidelines will just tell you to set a target impedance anywhere from 1 to 100 mOhm. The better option is to calculate a target impedance to ensure you don't over-design or under-design the PDN. Once you calculate the target impedance, you also need to calculate the deviation in the measured (or simulated) impedance from your measured impedance. We'll look at both points in this article.



How to Calculate Target Impedance

There is no single value of target impedance you should use in your PDN. Although there are several factors to consider when determining an appropriate target impedance, and not all of these will take precedence in your design. The goal of setting a target PDN impedance is to ensure that switching events in your digital ICs or high-frequency analog circuits do not produce excessively large transient oscillations on your PDN (supply and ground bounce).

Remember from discussions of ground bounce and supply bounce that switching signals in an IC will draw pulses of current into the PDN, which can excite a transient oscillation in the power bus voltage seen at the IC in question (supply bounce) and create high-frequency transient oscillations seen on the outputs from the IC (ground bounce). If you look at the article linked above, you'll see an excellent example of a measurement showing both effects in the same oscilloscope trace.

Since we know current draw into the PDN creates some voltage fluctuation on the output port of the PDN, we can relate the current being drawn into the PDN to the impedance of the PDN and the voltage disturbance seen on the main power bus via Ohm's law:

$$\Delta V = \Delta I Z_{PDN}$$

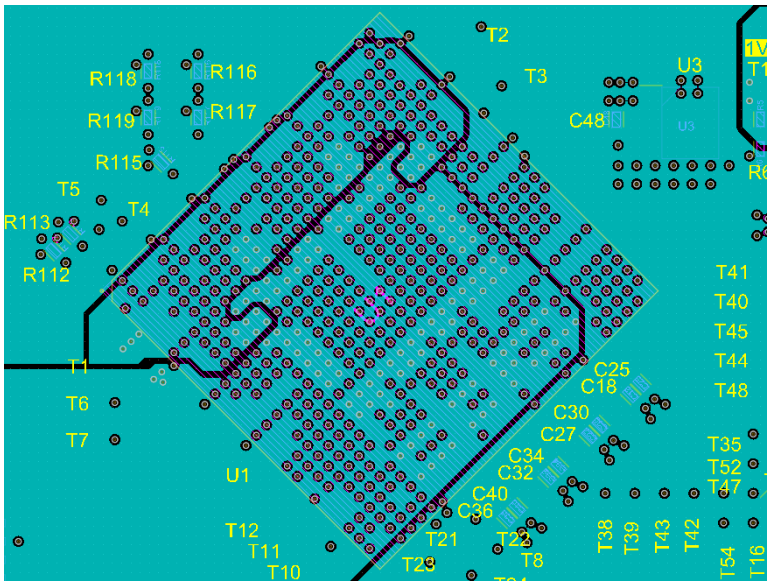
In essence, if you measure your voltage on the power bus with respect to the PDN's reference plane, you would measure the nominal DC voltage plus ΔV. I've used the Δ notation to indicate these are fluctuations, or rather values that are changing in time. Since the power bus draws in some ΔI during switching, and we want to minimize ΔV, we need to also minimize ZPDN.

This is more complicated than just looking at a single large IC. Some digital designs can have multiple large ICs connected to multiple voltage levels, with the bus for each level shared with other components that might also draw current in fast pulses. Therefore, we need to think about the structure of the PDN to get a reasonable estimate for the target impedance. The best option is to think of the system as a multi-port PDN.

https://www.youtube.com/watch?v=QxdwziRjpTw

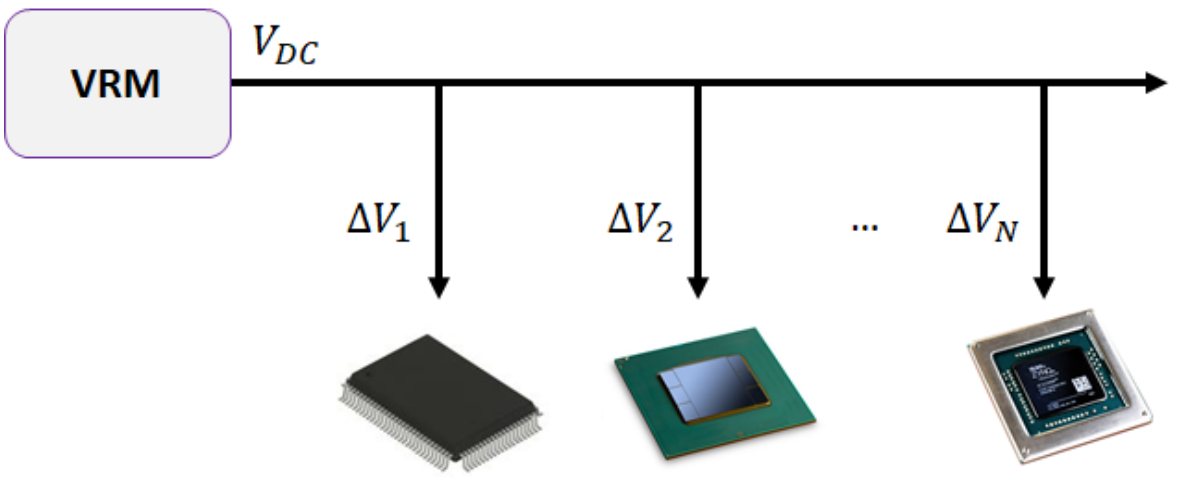
What About Multi-port PDNs?

A multi-port PDN typically has 1 input and N outputs connected to a main power bus, so you have a Z-parameter matrix instead of a single PDN impedance value. Flipping this around, you can even have a single IC (see the BGA component below) that has multiple power levels, each requiring its own bus and regulator. In this way, you technically have multiple subsections in your PDN with each requiring extensive decoupling.



This IC receives power at two different voltages, each requiring different buses to supply current.

The above equation for Ohm's law would now be written as a matrix equation relating the voltage measured at each output port to the current drawn into each port. You would then have to invert this equation to solve for the impedance matrix [Z] for a given tolerable ripple and current.



Common PDN topology involving multiple ICs or subcircuits on a power bus.

Obviously, we could spend an entire article (or more) going into this whole conversion. However, if you realize that the ripple created at 1 port in the PDN superimposes itself onto all other ports in the PDN via Kirchhoff's voltage law, you can find a minimum ripple value and target impedance with the following process:

1. Calculate the allowed ripple seen at each port
2. Use the total expected current draw into the PDN
3. Use the smallest ripple value from Step 1 and the total current from Step 2 to calculate the target impedance

The idea here is simple; just use the lower limit of the target impedance as your design goal in the entire PDN, rather than trying to design every entry in the Z-parameter matrix to have a specific value.

Calculating ΔV and Z

We're now back to the crux of this conversation: what's the best way to calculate the allowed value of ΔV? For a given port on your PDN model, you have a few options to set a target impedance:

- Look at the core voltage level on your IC, and calculate an allowed fluctuation within the core's allowed noise margin using some safety factor or the specs outlined in the datasheet.
- For high-precision applications, consider looking at the jitter imposed on the output. This is more difficult to determine without measurements and can be on the order of 1-10 ps/mV. High precision applications could require much less than 100 ps jitter to ensure accuracy (e.g., lidar ranging and imaging).
- Calculate the voltage fluctuation on any output due to current drawn into a buffer circuit during switching. For this, you'll need the pin inductance value from the component datasheet and the inductance of any via going back to GND.

Assuming you've determined an appropriate range, and you've built a prototype, you should then test it while measuring output signals from IOs and the power rail voltage. In the event you find that a specific component has too much jitter and noise on the output, the above limits simply might not work for your design. No matter what you calculate as your limit on ΔV, you should test the design to make sure it works to specs. If the noise on your signals can be comprehensively linked to excessive PDN impedance and power rail ripple, then you need to find some solution. This article by Kella Knack examines one case where excessive noise on IOs in a poorly decoupled PDN and some possible solutions to the problem.

Next, assuming you know the current levels in the high and low states, you can now determine the target impedance from Ohm's law using your determined ripple and maximum current draw into the PDN:

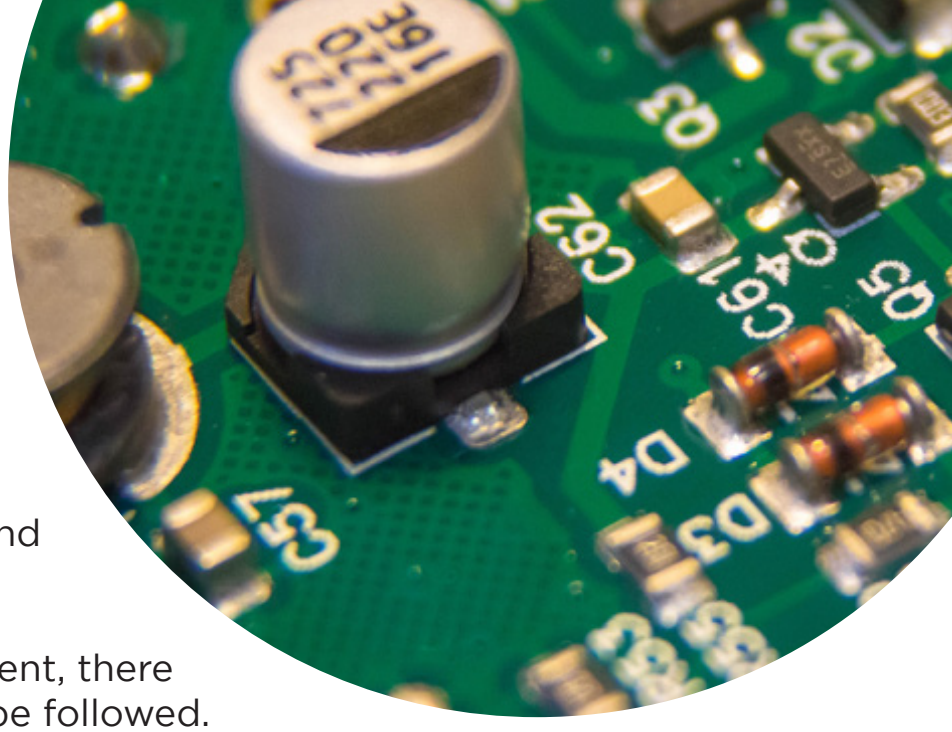
$$Z_{target} = \frac{V_{supply} \cdot (\%Ripple)}{\max[I_{transient}]}$$

Target impedance for a single voltage level on a power bus.

This is a rather conservative value for target impedance you can aim for in your design. This is because you're using the maximum transient current, whereas most other guidelines will state to take an arbitrary 50% of this value. This whole process also avoids being unnecessarily accurate. Normally, if you wanted to calculate the target impedance from Ohm's law, you would need to use a convolution (in the time-domain) to get the impedance impulse response, followed by a Fourier transform to get the target impedance spectrum. Instead, the above process doesn't need any integrals!

Once you've determined the target impedance you need to use in your PDN, you can define the right layer stack, PCB layout, cap placement, and much more with the best PCB layout tools in Altium Designer®. When you need to evaluate power integrity and EMI in your PCB layout, Altium Designer users can use the EDB Exporter extension to import designs into Ansys field solvers and perform a range of SI/PI simulations. When you've finished your design, and you want to release files to your manufacturer, the Altium 365™ platform makes it easy to collaborate and share your projects.

What is Spreading Inductance?



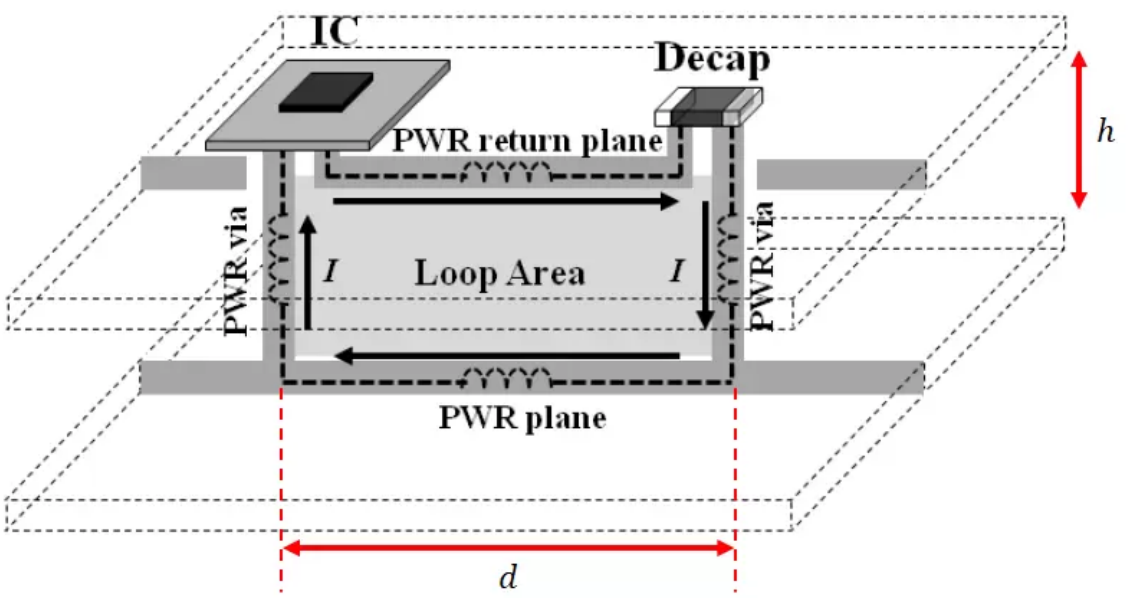
The above image shows a PCB with two large capacitors that might be used as the output caps for a VRM, which then can supply DC power to an integrated circuit. However, this board hides an important source of inductance: the power plane and power rails.

If you're working with a high speed digital component, there are some simple power integrity rules that should be followed. Using plane pairs, decoupling capacitors, and bypass capacitors are the starting point for designing the PDN in your PCB to have the required impedance. There is one quantity that is sometimes ignored when building a PDN impedance simulation: the spreading inductance of your plane pair. This quantity plays a deceptively simple role in determining the inductance leading into the input power pin on a component.

What is Spreading Inductance?

All conductive elements in your PCB can have some parasitic elements, including plane pairs. The one that we normally care about is plane capacitance, which provides additional capacitance to help your PDN decouple at high frequencies. In a DC PDN simulation, we look at the DC conductivity to try and spot power loss. There is one additional parasitic in a plane pair: the spreading inductance.

Simply put, the spreading inductance is the inductance created by the current path drawn along two planes and the circuit elements that connect them. In the PDN of a PCB, the spreading inductance is defined by the current loop spanning from a decoupling capacitor network, along a power plane, into the load input, and back along the ground plane to the capacitor. It is not equivalent to the loop inductance formed by this current path, it is only the portion of total inductance contributed specifically by the plane. The various contributors to plane-pair impedance are shown below:



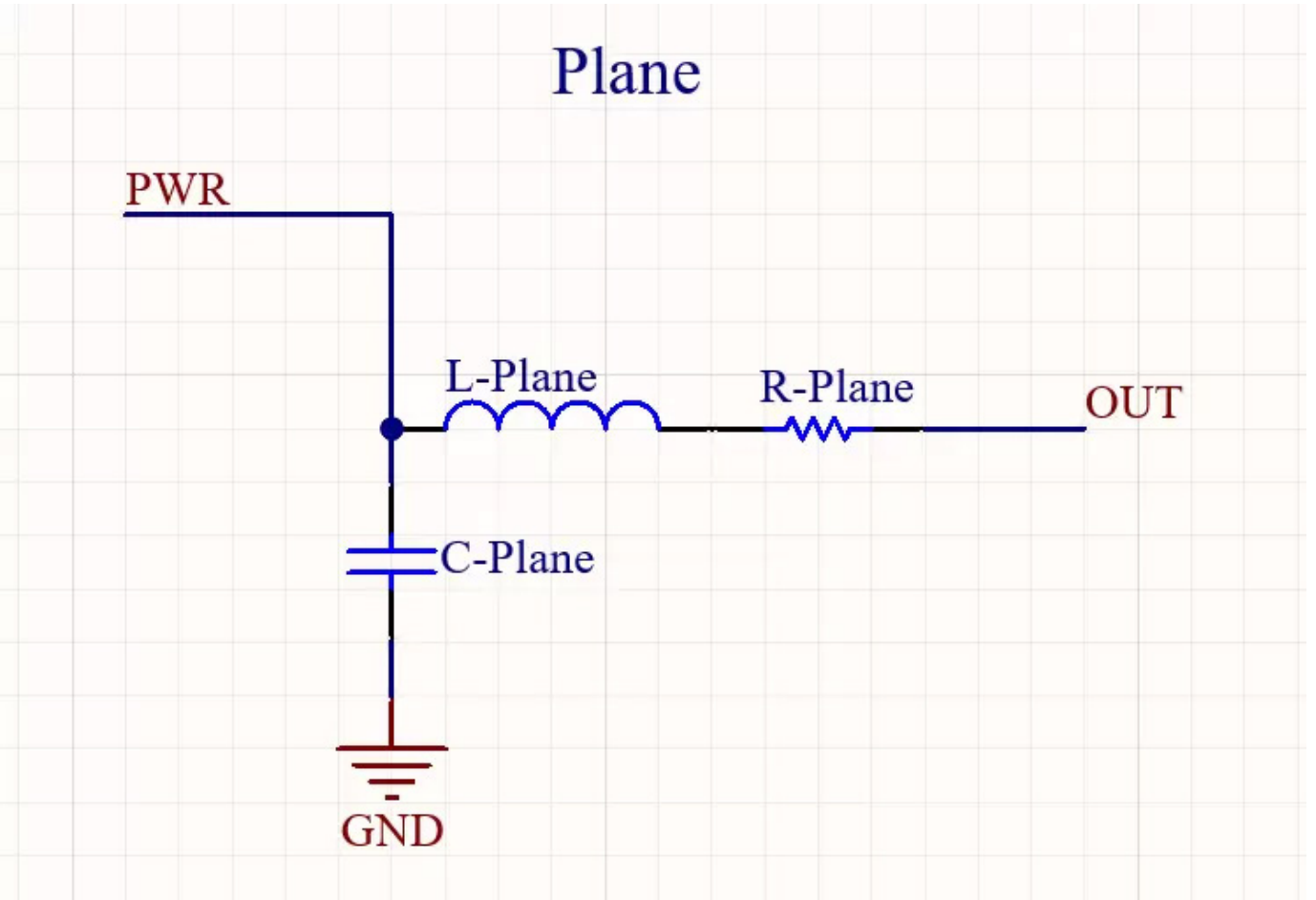
Why should we use the term “spreading inductance”? The term is used to denote that the current “spreads” in the power and ground plane pair, it does not follow a straight line. The current is confined to a narrow region between the decap output and the via input. Rather than following a literal straight line between these two points in the plane, current spreads out in the plane but does not totally fill copper in the plane pair.

This confinement of the current in the plane has an important consequence for PDN design: eventually, increasing the plane area does not necessarily decrease the spreading inductance. This is because, with a large plane, the current will not continue spreading along the current path. Instead, you can only change two other distances if you want to modify the spreading inductance as follows:

- **Reduce d:** Bringing caps closer to the load IC reduces the spreading inductance
- **Reduce h:** Bringing the plane layers closer together reduces the spreading inductance

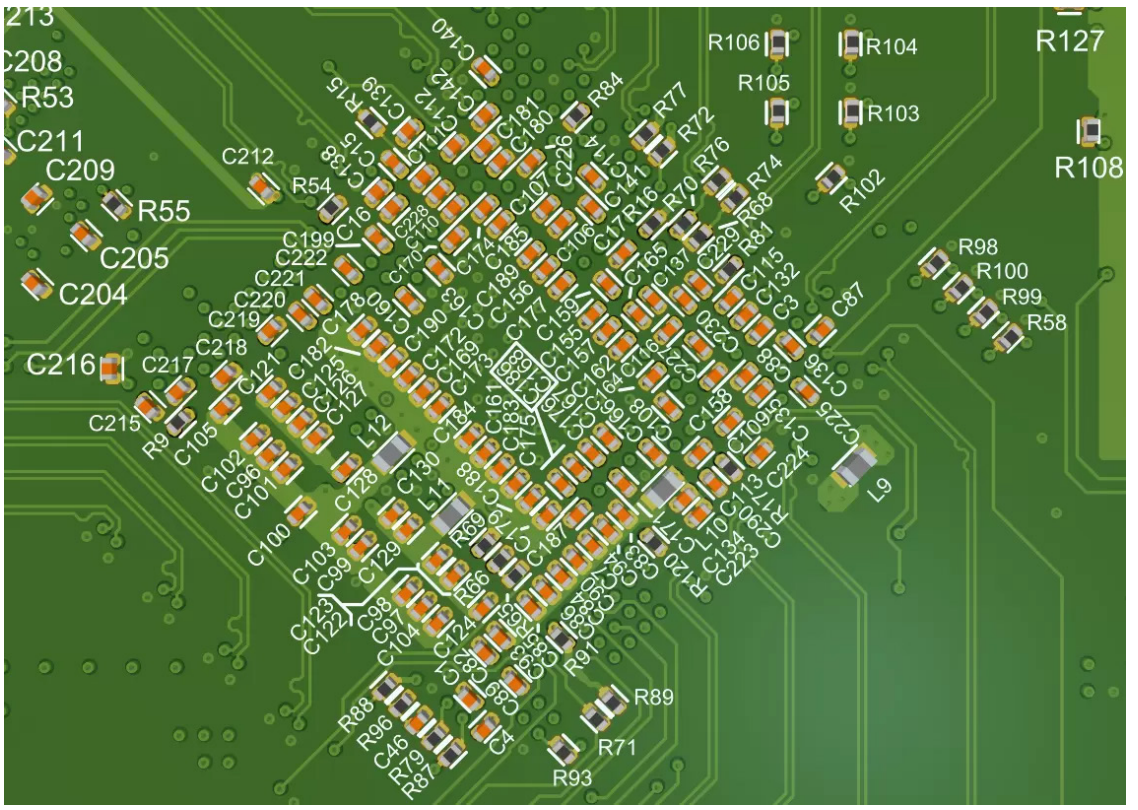
Modeling Planes With Spreading Inductance

In general, linear time-invariant (LTI) electrical systems can be modeled as RLC circuits, and the same idea applies to a plane pair with spreading inductance. The image below shows how the spreading inductance along a power plane would be modeled in a schematic for use in a simulation. The portion of the plane connecting from C-Plane to OUT contains two elements: an inductance (L-Plane) and a resistance (R-Plane). L-Plane is our spreading inductance defined by the current loop formed in the PDN. Together with C-Plane, these three elements contain all parasitics related to a plane pair.



Technically, we would have additional elements along the GND net corresponding to the R-Plane value for the ground plane and an additional L-Plane element for the via connection, but we can lump this into the R-Plane/L-Plane elements if we like. What's important is how connections would be made to other components in the above schematics. PWR is the output from the decoupling capacitor network. The series RL elements spanning from PWR to OUT model the location of the decoupling capacitor network.

Just as we indicated above, this means you have a simple way to reduce the spreading inductance: bring the decoupling capacitors closer to the input power pin on the load IC, or reduce the plane separation. In addition, you can use more vias to intentionally spread out the current in the power plane by placing vias connecting from a decap array to the power input in parallel. Alternatively, if you are using a large BGA component, just place the decaps directly on the back side of the board to minimize the spreading inductance.



Most of these capacitors are connected directly to a power pin on a BGA and the GND plane on the next layer. This provides the lowest possible spreading inductance for these decoupling capacitors.

https://www.youtube.com/watch?v=JHRKkSx3VmU

Decoupling Capacitors Connected to a Plane

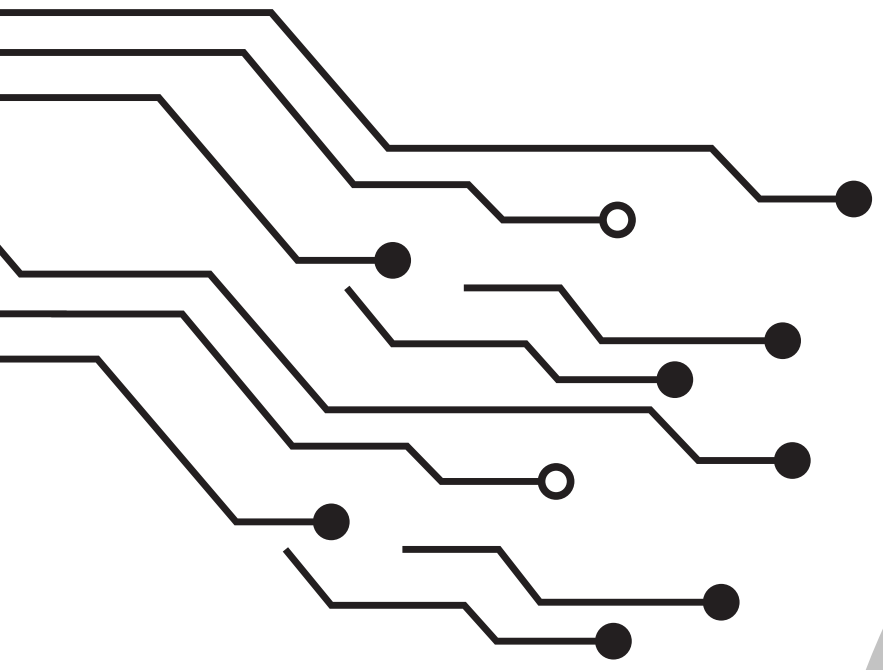
What about decoupling capacitors that are connected to a plane pair? Does the spacing between the capacitors have some inductance? The answer is “yes” it does, but this inductance is easily reduced by placing the caps very close together. We should be able to see this above: placing the capacitors close to each other basically sets d = 0.

A good guideline to follow is to use the smallest case caps that can still hit your required capacitance specs. 0402 case size is a good general-purpose selection for high speed boards unless you’re designing to very high density and need 0201/01005 cases. In these caps, the ESR value will be non-negligible, which can actually be a good thing, and the ESL values tend to be lower.

Unfortunately, there is no closed form equation you can use to calculate spreading inductance. The calculation involves several integrals with an eigenfunction expansion. The fastest way is to export your design into a field solver application. If you want to learn more, there is one comprehensive resource found in the research literature:

- Kim, J., et al. “Inductance calculations for plane-pair area fills with vias in a power distribution network using a cavity model and partial inductances.” IEEE Transactions on Microwave Theory and Techniques 59, no. 8 (2011): 1909-1924.

The built-in SPICE package in Altium Designer® can help you perform a range of simulations, including PDN simulations. When you’re ready to release these files to your collaborators for more advanced simulations, the Altium 365™ platform makes it easy to collaborate and share your projects. Everything you need to design and produce advanced electronics can be found in one software package.



Altium®

PDN Impedance Simulation and Analysis in SPICE

High speed signal behavior, RF signal propagation, and PDN simulations are some of the most difficult aspects of a PCB to simulate. Among these electromagnetic phenomena, high speed signal propagation and RF propagation require electromagnetic field solver tools to extract useful results. There are simply too many parasitics and design-specific effects to account for in a circuit simulation. Try as we might, there is just too much information to attempt to model in these two situations.

PDN simulations are a bit different as the relevant frequency range to be simulated is lower, typically less than 10 GHz for most devices. This means that a PDN supporting moderate speed digital components on a relatively small board can be modeled using SPICE simulations rather than full electromagnetic field solver simulations. As long as the board is small enough or frequencies are low enough that propagation can be ignored, you can get some useful results with a SPICE simulation.

If you've never done this before, I'll show how to set this up and what kinds of results you might expect. By simulating switching action in a load component connected to a PDN, you can extract some useful data to describe your PDN and even calculate its network parameters. In the simulations I'll show below, the goal is to extract:

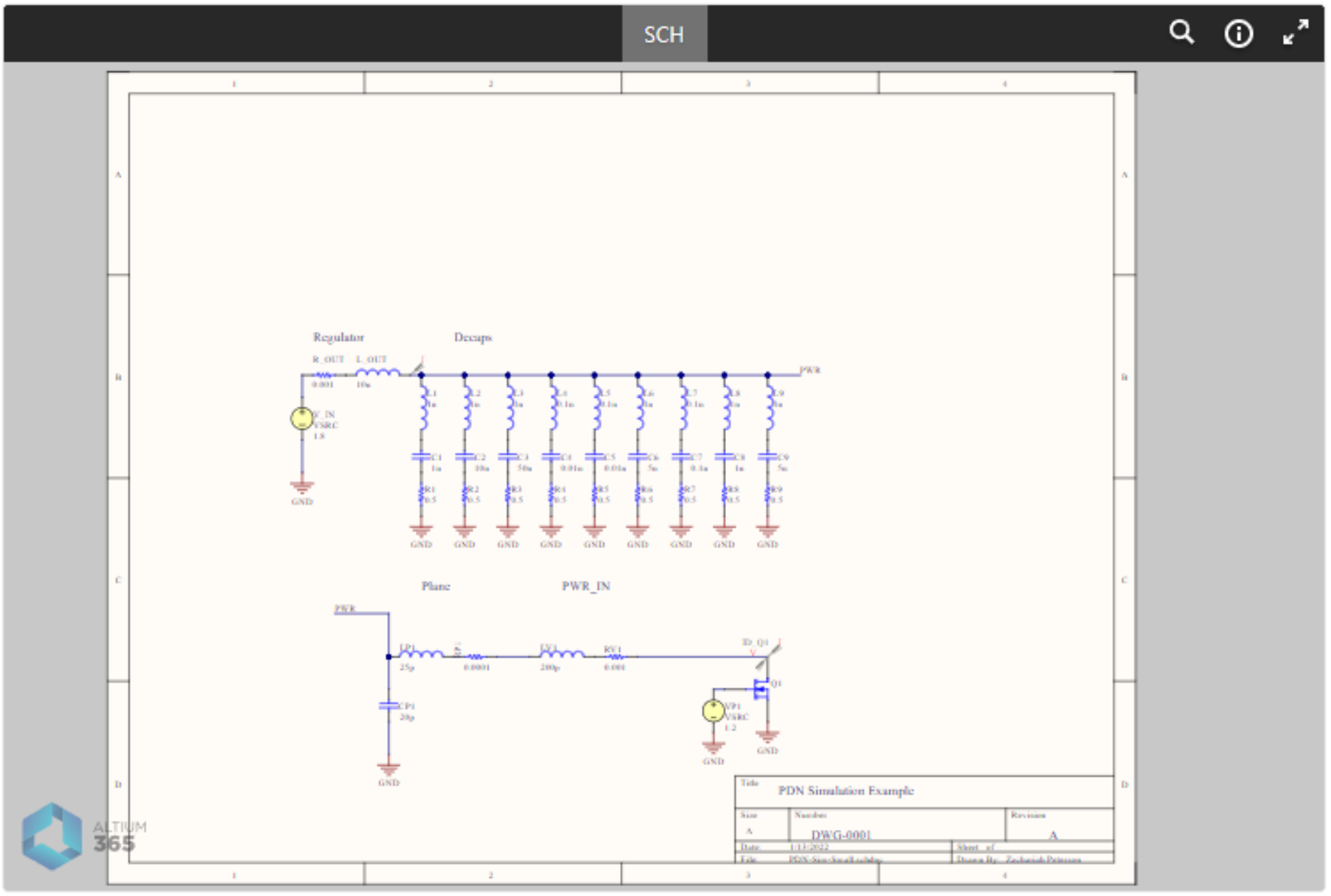
- A PDN impedance spectrum
- The transient response as measured at the input pin of the load component
- How these parameters change as the amount of capacitance changes

The limitation to relatively low-speed and small boards is important, and I'll describe a bit more what this really means as we proceed.

https://www.youtube.com/watch?v=ig9WtFcP4IM

Setting Up a PDN Simulation

A standard simulation used to describe PDN impedance and calculate the transient response is shown in the schematic below. I've placed this in the Altium 365 Viewer so that users can browse through the design and see how the simulation is set up.



The simulation schematic was created with a set of decoupling capacitors that were not chosen in any particular order. I've kept the number low initially, but I'll increase this later in the simulation just so we can see how increasing the capacitance affects the results. We'll adjust the other parameters as well as we proceed.

Equivalent Circuit Model

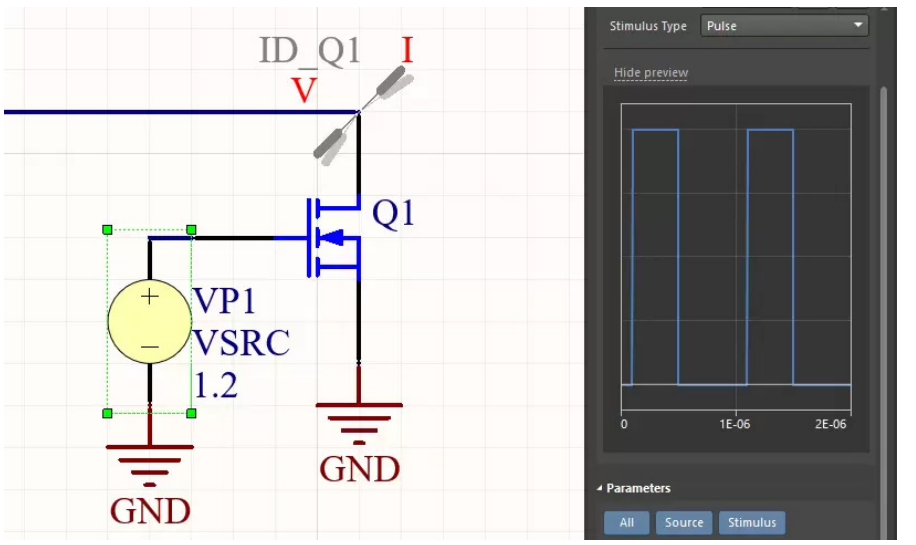
This schematic is set up using components in the Simulation Generic Components library that is built into Altium Designer. If you're not an Altium Designer user, you could certainly recreate this in any other simulation program using generic components in a SPICE package or another schematic editor. The overall simulation consists of four sections as I've indicated in the schematic:

- **Regulator:** This is the voltage regulator module or circuit that supplies power to the PDN. I've included its nominal output resistance and inductance.
- **Decaps:** This is the decoupling capacitor section. The capacitors have ESL and ESR included as discrete components just to show them clearly. Note that you could also define these values as parameters in these components inside the Properties Panel.
- **Plane:** This section defines the capacitance, inductance, and resistance of our power/ground plane pair. The inductance in this section is a spreading inductance, which I've described in another article.
- **PWR_IN:** This is the input power section in our load IC. I've attempted to model the input via inductance, pin-package inductance, and contact resistance at the input. These values are product and package specific, but the values here are typical order-of-magnitude numbers.

This equivalent circuit model requires adjusting the plane capacitance (CP1), plane inductance (LP1), and number of decoupling capacitors. We'll use the transient analysis and AC sweep simulations to get these data. Before that, we should discuss the NMOS component shown above.

Modeling the Load

The PWR_IN section includes a model for the load, which is just a switching n-channel MOSFET. When modeling the load and looking at the transient response on the PDN, the goal is to examine how the PDN reacts to switching action, which then draws in current. Using a fast MOSFET in this way is one method to examine how the load current suddenly switches to a high current state based on some logic input. That logic input is modeled with the VSRC element set to Pulse mode in the Properties Panel. I've set the rise and fall times to 1 ns. This is not in the super high frequency range, although the 1/(rise time) bandwidth is 500 MHz, so the signal could be affected by poor decoupling in the planes and larger capacitors.



PWR_IN section in the simulation.

The other way to do this is with a current source set to pulsed mode. This would effectively perform the same function of switching the load between low and high current states. The simulation will then read the resulting current and voltage given to the MOSFET drain. A more accurate method would be to place a CMOS buffer circuit to model an IO, but that would be better for examining something like ground bounce or jitter, so we'll save that for later. For now, we'll look at the above model to examine what happens when logic circuits switch states and draw current through the PDN.

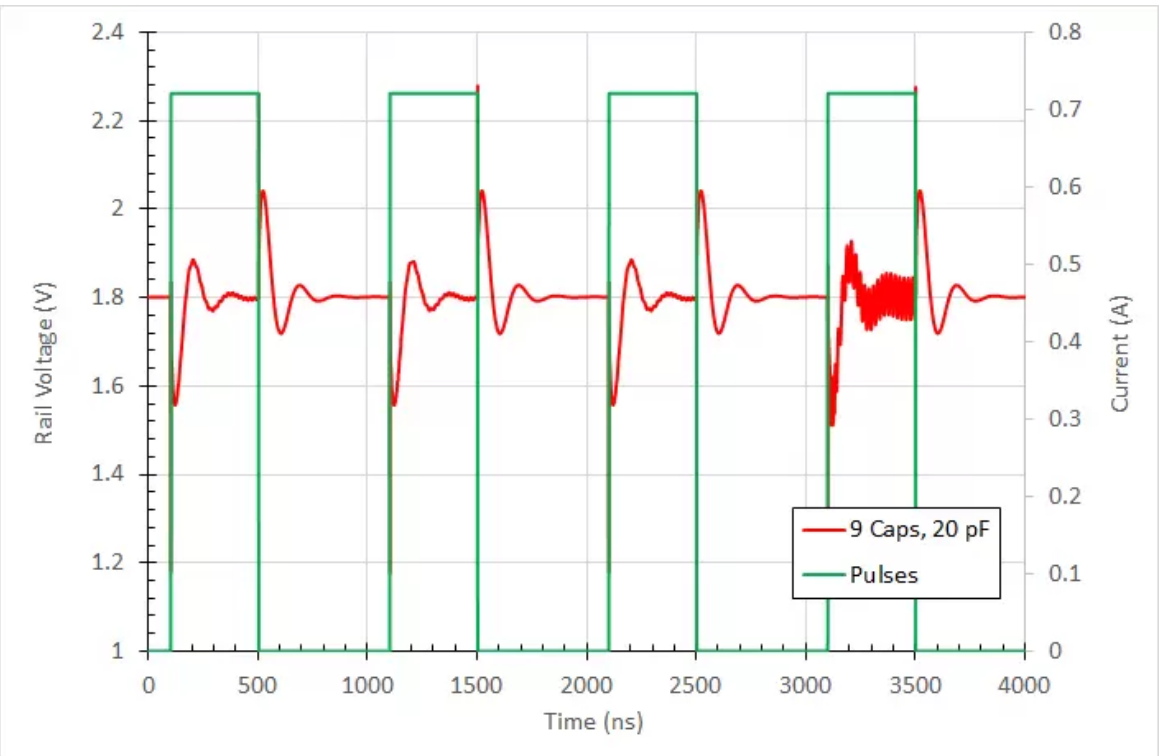
Results

First, I want to look at the results for the above case, where we have 9 decoupling capacitors of various values in parallel, all with similar ESL and moderate ESR values. The ESR value is important here as it helps flatten out the PDN impedance spectrum, as I showed in another article on PDN impedance. The simulation parameters are as follows:

- Transient analysis: 10 ns step size, 5-10 us total simulation time
- AC sweep: 10 GHz maximum frequency, calculating |Z| for the PDN
- Decoupling capacitor number: I'll look at the above block of 9 capacitors and a quadrupled block of 36 capacitors.
- Plane capacitance: Low state (CP1 = 20 pF) and high state (CP1 = 1 nF)
- Core voltage: VDD = 1.8 V

9 Caps, 20 pF Plane Capacitance

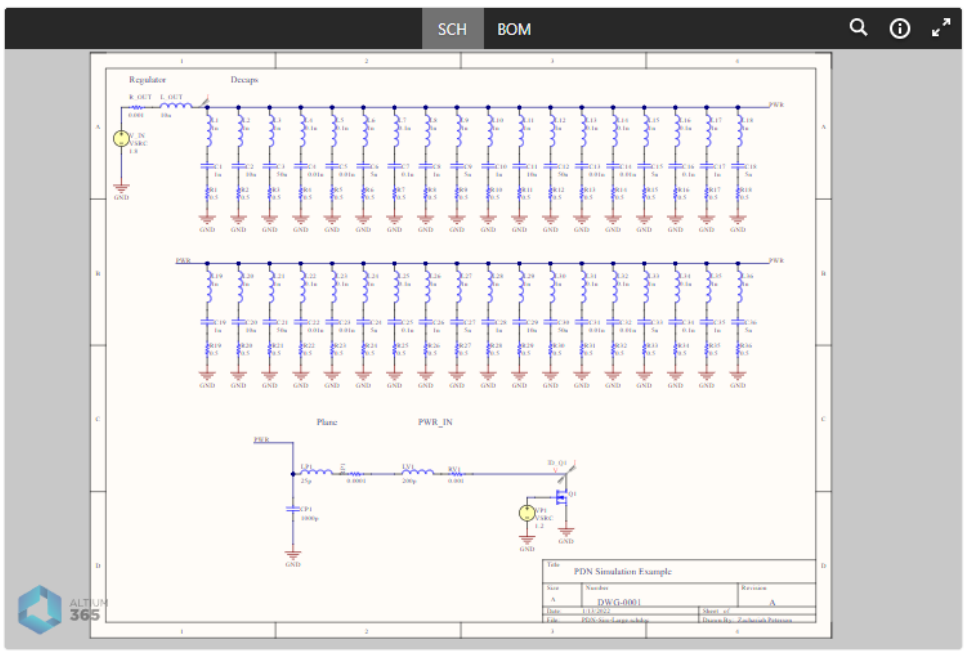
With only 9 decoupling capacitors and 20 pF plane capacitance, we can see very large fluctuations in the transient response reaching ~300 mV in amplitude superimposed on the desired 1.8 V core voltage. This is unacceptably large for any practical application and would produce large glitches on the output. The data shown here were extracted from the .sdf file and exported into Excel format.



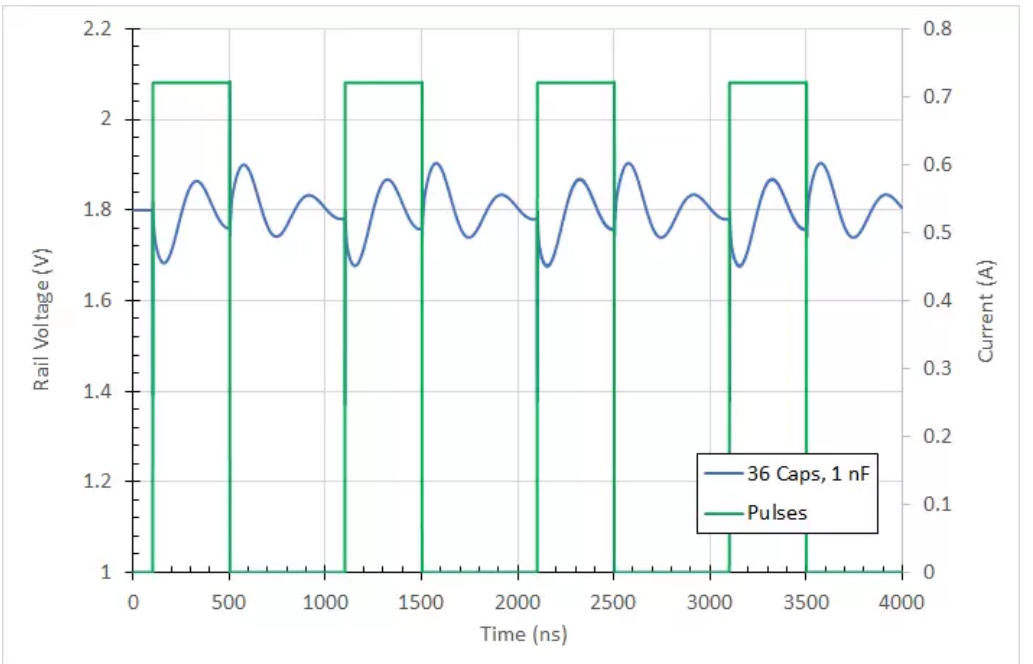
Transient results with 9 decoupling capacitors and 20 pF plane capacitance.

36 Caps, 1 nF Plane Capacitance

Let’s see what happens when we quadruple the number decoupling capacitors and increase the plane capacitance by a factor 50. The new-and-improved version of this design is shown below. The decoupling capacitor block is basically copied to increase the equivalent capacitance of this decoupling network.



The results clearly show the benefit of having power/ground plane pairs and more decoupling capacitors; as the capacitance goes up, the amplitude of the transient response generally goes down, just like we would expect. The power rail response on the PDN fluctuates with only 100 mV amplitude when we quadruple the number of capacitors and increase the plane capacitance.

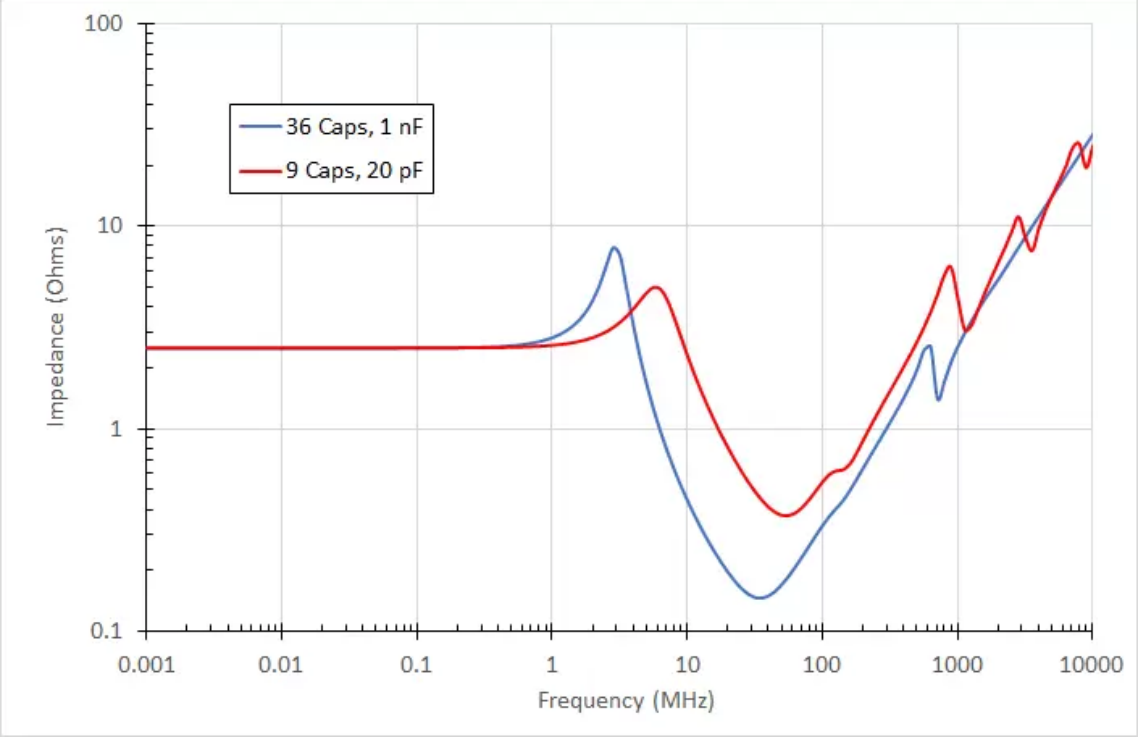


Transient results with 36 decoupling capacitors and 1 nF plane capacitance.

This is still a bit large for a 1.8 V rail, and it might seem that the use of 36 caps should produce a better result. We can get a sense as to why we don’t get significant damping with more capacitors by looking at the impedance spectra in each case.

Impedance Comparison

We can also get the PDN impedance by taking the ratio of the complex V/I response functions in the frequency domain (AC sweep results), followed by calculating the magnitude of this ratio. We can see that the PDN impedance is still a bit large, particularly in the neighborhood of the 1/(rise time) bandwidth limit. We can also see the benefit when looking at the PDN impedance spectrum, as shown below. The graph below compares the current situation with 36 decaps/1 nF with the previous situation of 9 decaps/20 pF.



PDN impedance simulation results comparison.

Note that we only have low impedance (100 mOhms) over about 1 decade. We'd like this band of low impedance to be lower and broader. We also have some peaks around 3 MHz and a high frequency response at 630 MHz. To solve these problems, we may need a greater number and diversity of capacitors. We can use some other tricks like increasing via count during the layer transition into the IC as this would reduce total inductance at PWR_IN input stage, and we could reflect this in the SPICE simulation.

Practically, having 36 low-ESL/low-ESR capacitors is common in high IO count ICs, and certainly in ICs that will draw 720 mA of current in a single pulse. In fact if you look at some reference designs or evaluation products that use high speed components with high IO count, you would find that 36 decoupling capacitors is a low number. Just for perspective, the dI/dt value for this pulse is 720 MA/sec (that's 720 mega-Amperes per second!), which is a huge number requiring many capacitors to discharge very quickly. Embedded capacitance materials on this thin plane separation dielectric will also increase the plane capacitance.

Why “Small” Boards?

What exactly qualifies as a “small” PDN? Remember, when the load switches, a broadband current pulse is pulled into the PDN, and this pulse travels along the PDN at the speed of light. Think of it as a propagating signal, but one that carries power instead of data. In the limit of a small PDN, we can ignore propagation effects just like we would in a transmission line. In fact, the transmission line comparison is apt here and a PDN is sometimes described with the same lumped circuit model used in transmission lines.

When the wavelength with the largest frequency component in the delivered power pulse is much larger than the nominal board size, we can ignore the fact that our delivered power has to propagate from the regulator output to the load input. This is the same logic used to understand why we can define a critical length in a transmission line. Once the design gets too large, or when the relevant bandwidth get to very high frequencies, electromagnetic solvers will be needed to run a complete PDN impedance simulation and extract the transient response.

What’s Missing?

The astute design engineer should notice something important: we haven’t included dissipation in the plane capacitance! This references the imaginary part of the dielectric constant, which would be modeled by adding some resistance in series with the plane capacitance. It basically plays the same role as G in the impedance equation for a transmission line. The size of this resistance requires some additional calculation, which will depend on the amount of loss in the dielectric material separating the plane layer. In the next article on power plane resonances, we’ll be able to see the beneficial effects of high loss tangent in the laminate.

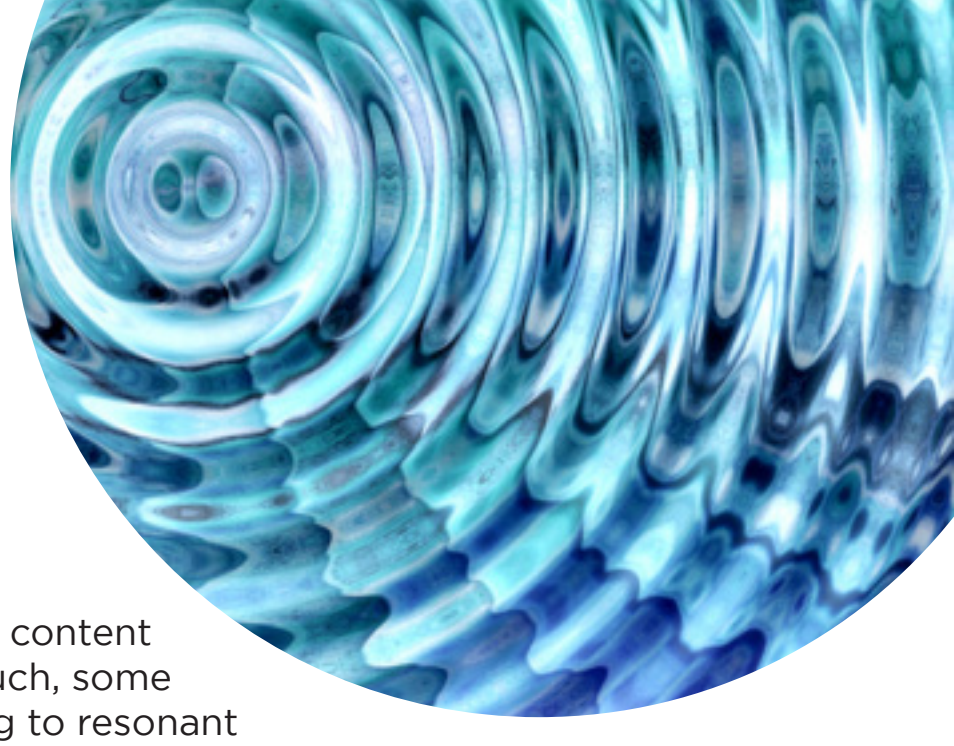
What Else Can We Simulate?

The results shown above clearly show how adding capacitance decreases PDN impedance and helps stabilize the core voltage. The above caps were just selected a bit randomly, they weren’t based on a thorough analysis of targeting specific frequency ranges. We could get better results if we went through that exercise and produced a PDN impedance reduction over a broader bandwidth.

Some other points we could simulate in SPICE include:

- S-parameters for the PDN by calculating the impedance at the input and output ports, which we’ve already done
- Impulse responses for any current pulse pulled into the PDN
- Transfer impedances between multiple rails in the PDN
- The effects of additional inductance, such as adding a ferrite to the power pin; we’ll look at this in an upcoming article
- Addition of a bypass capacitor directly to the power input on the load (in parallel with Q1)

The built-in SPICE package in Altium Designer® can help you perform a range of simulations, including PDN simulations. When you’re ready to release these files to your collaborators for more advanced simulations, the Altium 365™ platform makes it easy to collaborate and share your projects. Everything you need to design and produce advanced electronics can be found in one software package. We have only scratched the surface of what is possible to do with Altium Designer on Altium 365.



When Do PCB Power Plane Resonances Occur?

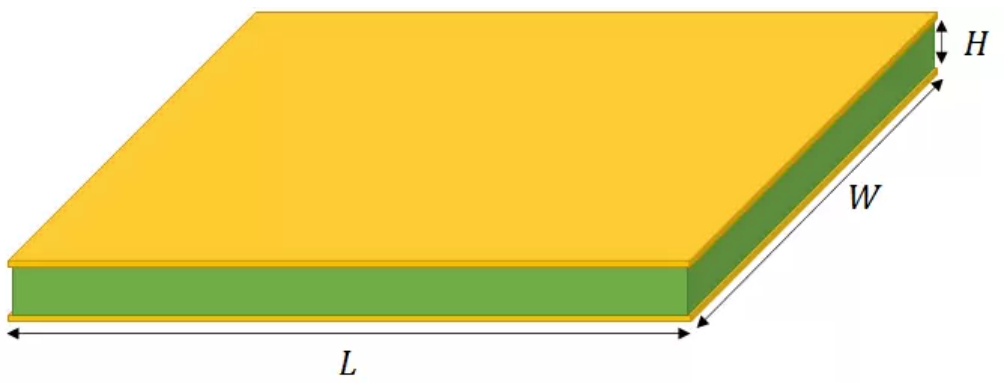
By now, designers should be aware of some important behavior involved in power delivery to components in a PCB, particularly for digital components. All digital components produce and manipulate wideband signals, where the frequency content theoretically extends up to infinite frequency. As such, some radiation may propagate through your PCB, leading to resonant behavior that is not observed on the power rail.

This behavior is better known as power plane resonance. Whenever a power/ground plane pair is excited with a current pulse, that pulse emits some electromagnetic radiation, and that radiation can excite structural resonances at specific frequencies. Which frequencies will excite strong resonances depends on the dielectric thickness of the layer separating the plane pair, as well as the overall cavity size of the PCB. To see why this is important, you only have to look at the PDN impedance spectrum.

When Does a Power Plane Resonate?

The most important elements in your PDN are your power and ground plane pair. All power/ground plane pairs will have a set of resonances that can be excited by electromagnetic radiation. Such radiation arises whenever power is being pulled into the PDN. Remember, the plane pair in a PDN is like a big capacitor; when excited with a current pulse (from a digital signal) or a harmonic wave (from an analog signal), an electromagnetic disturbance develops between the power and ground planes. This disturbance can begin propagating between the planes, just like a large excited slot antenna. As electromagnetic waves propagate in the PDN, they can set up resonances and anti-resonances as different wavefronts interfere with each other.

These resonances happen at specific frequencies, sometimes called resonant frequencies or eigenfrequencies. The various frequencies involved can be calculated by treating the plane pair as an open cavity, better known as a waveguide. At certain frequencies, electromagnetic waves traveling in the plane pair waveguide will resonate, producing peaks and valleys in the PDN impedance spectrum.



Calculating Plane Resonant Frequencies

Unfortunately, you can't easily calculate the resonant frequencies in a PDN exactly, you would need to do it with an electromagnetic field solver. This is because the PDN can have a complex structure, with multiple vias and conductors placed around the design. The plane region could also have a very odd shape that would not be easily solvable by hand.

Luckily, you don't have to solve Maxwell's equations or its corresponding wave equation yourself; the general solution to the wave equation in a cavity or waveguide is well-known and can be used to estimate a set of possible resonant frequencies. For our arrangement above, we would have the following formula for the eigenfrequencies of the plane pair waveguide:

$$f_{i,j,k} = \frac{1}{2\pi}\sqrt{\left(\frac{i\pi}{L}\right)^2 + \left(\frac{j\pi}{W}\right)^2 + \left(\frac{k\pi}{H}\right)^2}$$

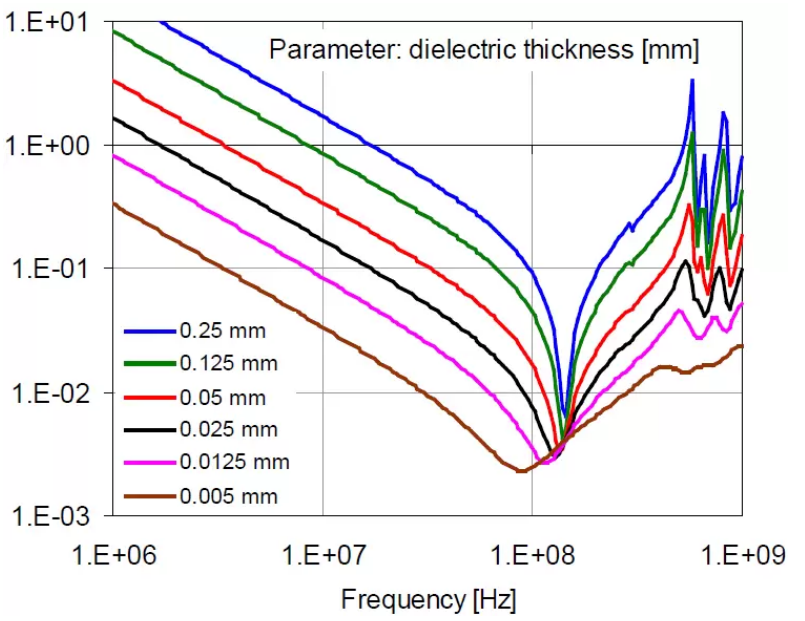
Equation for calculating power/ground plane pair resonances.

Theoretically, there is an infinite set of possible frequencies, and these are indexed by the set of integers (i, j, k). From this formula, we can use some estimates to generate a set of tables defining the waveguide's resonant frequencies. To do this, we typically look at k = 0 for the height direction.

Why worry about k = 0? This is because, for the (0, 0, 1) resonance, the resonant frequencies corresponding to the vertical direction are hundreds of GHz. Just as an example, for an 8 mil thick dielectric with Dk = 4, the lowest order vertical resonance (k = 1) is 375 GHz. It is the lateral resonances that dominate as these resonances can appear around 1 GHz. This is one reason why PDNs with strong high frequency noise emissions can emit strongly from the board edges; they are emitting strongly due to resonant excitation in the power/ground plane pair structure as waves travel towards the edges of the circuit board.

Example PDN Impedance Spectra

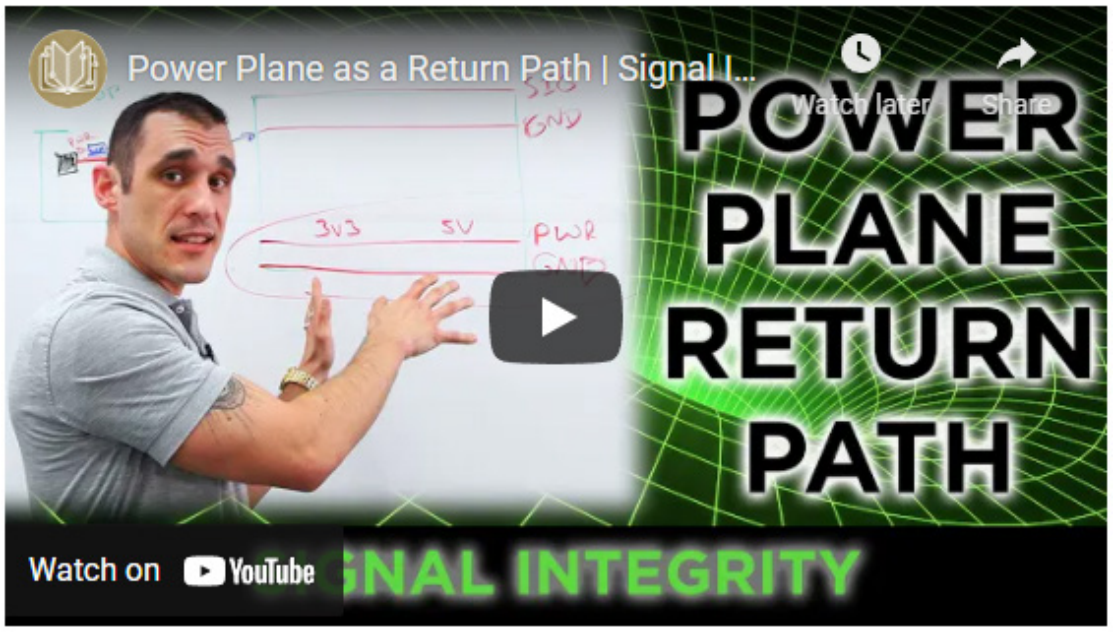
When we look at a measured PDN impedance spectrum, resonances and antiresonances can be clearly identified in the GHz range. An set of example impedance spectra showing the structural resonances due to the power/ground plane pair arrangement is shown below. These resonances are shown for a plane pair with various dielectric thicknesses.



Example PDN impedance spectra with power plane resonances clearly visible near ~700 MHz. [Source: DuPont]

The image above shows how structural resonances and the overall impedance curve are affected by the thickness of the dielectric. As the dielectric gets thinner, we would expect the plane capacitance to increase, thus the overall impedance curve drops down and the impedance minimum (around 100 MHz) moves to lower frequencies. However, we see that the structural resonances are effectively unchanged. This is our cue that the above resonances are all k = 0 resonances, just as we would expect.

However, why are the resonant peaks smaller? This is because, as the thickness is decreased, the loss in the plane pair cavity increases, which dampens traveling waves and reduces the intensity of the electromagnetic field during resonance. This should illustrate the benefits of high Dk laminates. When used in PDN engineering applications, you want the highest Dk value possible to reach low impedance and to dampen resonance.

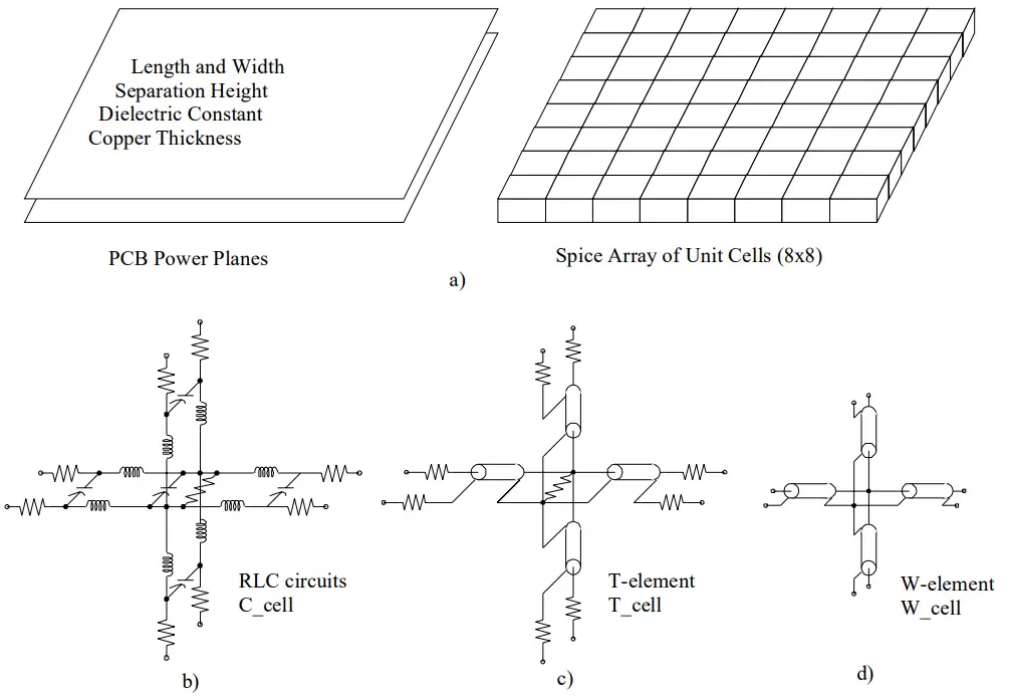


https://www.youtube.com/watch?v=Iv8CZSc0o-c

Simulating Power Plane Resonances

If you wanted to try and simulate power plane resonances, you can't realistically do it with SPICE simulations unless you write a specific model that accounts for propagation and reflection of an electromagnetic wave. One would essentially need to write all the important field solver results into a SPICE subcircuit and attach this to a PDN "component" as it were. Unless you're a SPICE expert, you're out of luck on this front.

There is one interesting IEEE paper from 2001 that provides a SPICE model for lumped element circuits, just like you might do in SPICE to simulate a transmission line. The model basically lumps RLC elements into "cells" that have their own resonance and coupling, creating a large set of possible resonances to be observed in the resulting PDN impedance spectrum. This type of lumped element model and a link to this paper can be found below.

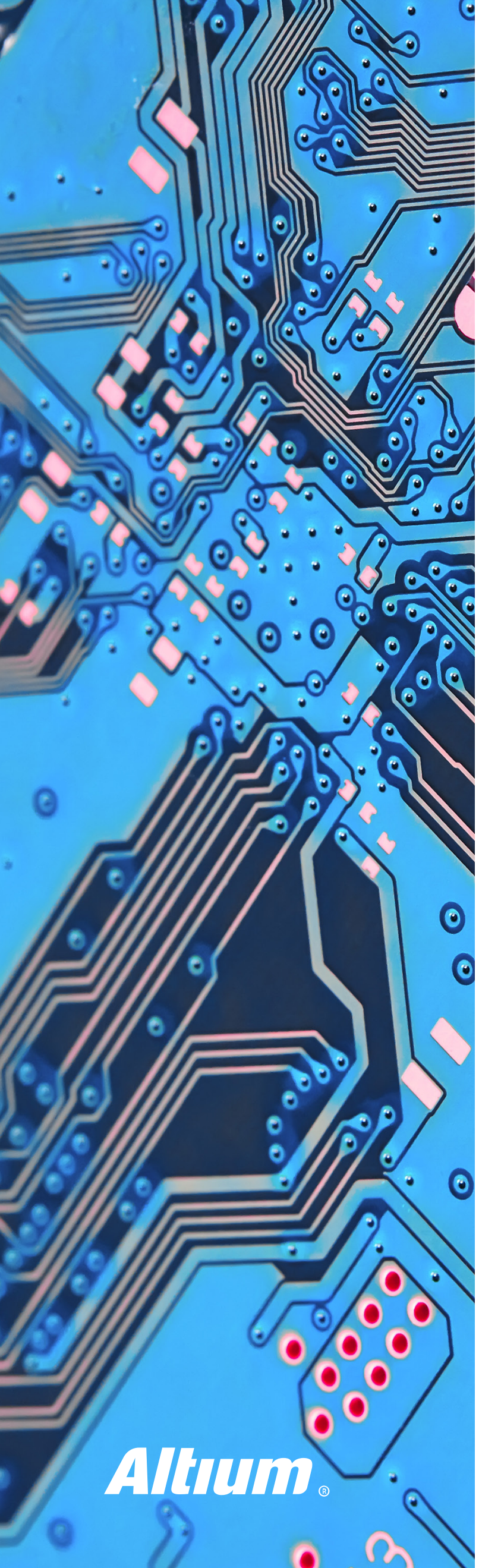


Example lumped element circuit arrangements that can be used to model plane resonances in a PDN impedance spectrum.

- Smith, Larry D., Raymond Anderson, and Tanmoy Roy. "Power plane SPICE models and simulated performance for materials and geometries." IEEE Transactions on Advanced Packaging 24, no. 3 (2001): 277-287.

These lumped element models don't exactly capture the true nature of wave propagation and essentially model the PDN as a big group of transmission lines in 3D. The whole point of this is to attempt to account for propagation and reflection, which would produce plane pair resonances at specific frequencies. If this system were simply prepared as a basic RLC circuit, the results would show a very high number of poles in the network's transfer function; SPICE results would actually show the network resonating at the pole frequencies.

For this reason, electromagnetic field simulations for the PDN are needed. You can do these simulations with your Altium Designer® PCB layout by exporting your design into an Ansys field solver format using the EDB Exporter extension. When you've finished your design, and you're ready to release files to your manufacturer, the Altium 365™ platform makes it easy to collaborate and share your projects.



Identifying Near-field EMI in a PCB's Power Distribution Network

Any electronic product that is intended for FCC or CE certification needs to pass radiated emissions and EMC testing. If your product doesn't pass testing, identifying sources of excessive radiated electromagnetic interference (EMI) can be difficult. PCB designers often resort to near-field probe measurements with an oscilloscope to identify offending components or board areas, as well as the frequency content of the radiated EMI. Designers then need to rely on their experience to link radiation at specific frequencies to various EMI sources.

All this takes time, effort, and specialized experience to identify EMI sources and propose solutions. The alternative is to use a field solver to simulate near-field EMI in a PCB directly, as well as evaluate potential solutions to EMI problems. By calculating the electromagnetic field emitted from different regions in a PCB, a field solver can be used to pinpoint an EMI problem to a specific area of the board before a prototyping run. Anytime you can identify and correct an EMI problem before manufacturing, you've cut down your development costs and time to market.

With the Ansys SIwave® package, you can access multiple integrated field solvers for signal integrity, power integrity, and EMI analyses. Altium Designer® also provides seamless integration with SIwave through the Ansys EDB Exporter extension, giving designers a simple way to perform these analyses directly from their layout data. To see how this works with an Altium PCB layout, we'll look at an example Altium Designer project and how excessive near-field EMI can be identified from a series of simulation results.

Near-Field EMI Analysis for a PDN

The Mini PC example project in Altium Designer will be used here for near-field EMI analysis with Ansys SIwave. This particular board contains multiple high-speed interfaces, and any of these could experience power integrity or signal integrity problem. After importing the board geometry and layout into SIwave, a full-wave solution in the frequency domain can be used to identify sources of near-field EMI in the Mini PC board.

The Mini PC contains multiple components and high-speed interfaces that should be investigated for signal integrity and power integrity problems.

- Intel Arria 10 FPGA
- 2 Onboard 8 GB DDR4 DRAM chips running at 1866 MHz
- 2 SODIMM expansion slots for DDR3/4 RAM modules
- USB 3.0, 10/100/1000Base Ethernet, PCIe

Any of these high-speed components and the interconnects between them can act as a source of near-field EMI if not laid out correctly. In order to identify any EMI sources in the board during operation, the EMI Scanner tool in SIwave can be used to automatically check a PCB layout against EMI design rules before running full-wave simulations. This allows problem areas to be identified so that they can be inspected further during a full-wave simulation.

Identifying Problem Areas

The Mini PC layout contains 16 layers with multiple plane-signal-plane layer arrangements for stripline routing. In an initial survey of the Mini PC layout in Altium Designer, we see two stripline DDR4 bus nets (Layer 7) are referenced to the PLL_1V8 power plane (Layer 6, provides 2.5 V to 1.8 V regulation for the FPGA) and to the VDD_DDR power plane without (Layer 8, provides power to the DDR4 modules). Other byte lanes sit on Layer 5, which also use Layers 4 and 6 as their GND reference. As return paths are being established in power planes as displacement currents, there needs to be a low-impedance return path back to the reference potential on the ground plane.

In the Mini PC layout, the only plane in the DDR4 section that doesn't have a sufficiently low-impedance return path back to ground is Layer 6, specifically the PLL_1V8 net. This low-impedance return path back to the nearest ground planes (Layers 4 and 9) could be provided through decoupling capacitors. One would reasonably expect a near-field EMI problem to arise somewhere in this region as there is low interplane capacitance between PLL_1V8 and the nearest GND nets on Layers 4 and 9.

The PLL_1V8 net in the Mini PC is shown in Figure 1. In this image, we see a region in the PCB layout where discontinuous return paths for the DDR4 nets were identified with the EMI Scanner tool in SIwave. The highlighted region in Figure 1 is the PLL_1V8 net.

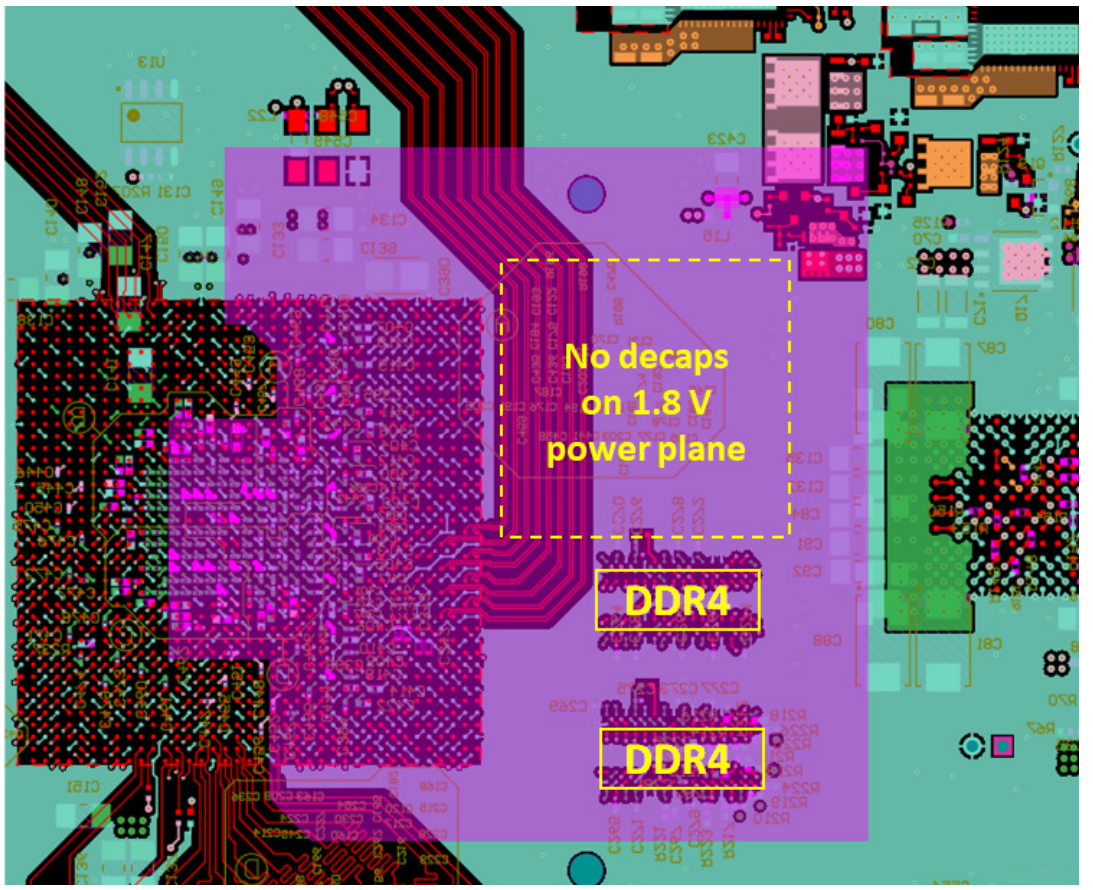


Figure 1: PLL_1V8 net flagged by missing decoupling capacitors.

Now that EMI Scanner has flagged this net for further inspection, more sophisticated techniques can be used to check whether this EMI design rule violation causes a significant problem in the design. To do this, we can use SIwave to:

1. Identify impedance anti-resonances in the PLL_1V8 portion of the power delivery network (PDN) as these could be excited by displacement currents, and
2. Simulate near-field radiated EMI before and after the return path problem is fixed.

Let's look at this in greater depth using the simulation tools in SIwave.

https://www.youtube.com/watch?v=QxdwziRjpTw

Matching Potential EMI Frequencies to PDN Anti-resonances

The hybrid solver in SIwave can be used to extract broadband Z-parameters for the PLL_1V8 net, which then allows any anti-resonances in the Z-parameter spectrum to be identified. In this case, PDN resonances can be excited if their frequency falls in the bandwidth of the displacement current, which would produce strong ringing on the PDN. This would then radiate a strong electric field in the near-field regime at the PDN anti-resonant frequency.

Figure 2 shows the extracted self-impedance for the PLL_1V8 net from 100 kHz to 4 GHz. Note that other Ansys electromagnetic solvers could also be used to extract other Z-parameters for a complex multiple-input multiple-output PDN, such as the transfer impedance between PLL_1V8 and any other power plane.

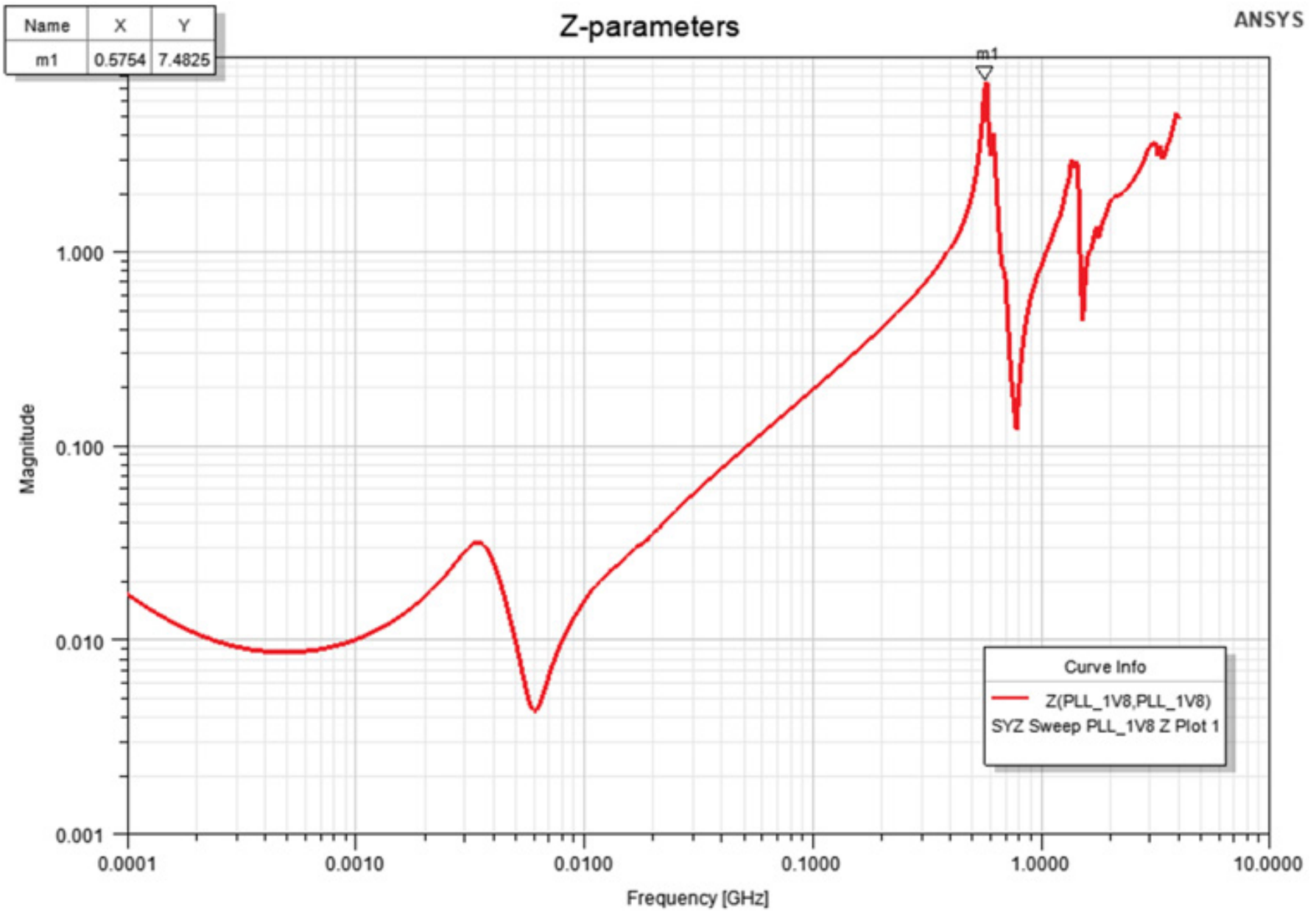


Figure 2: Self-impedance of the PLL-1V8 net extracted with SIWave.

The PLL_1V8 portion of the PDN has a strong anti-resonance at 580 MHz, so the next logical step is to investigate near-field radiated emission near that frequency. Rather than trying to model discontinuous return paths in the time domain, near-field radiated emissions throughout the PCB can be simulated directly in the frequency domain with the AC Solver option in SIwave.

Near-field EMI Simulation Results

Some initial near-field simulation results due to return currents induced in the PLL_1V8 net are shown in Figure 3. In this figure, we clearly see strong emission near Q4, which supplies power to the PLL_1V8 power plane net (upper-right portion of the region shown in Figure 3). The radiated electric field (magnitude) from this region is orders of magnitude larger than the background electric field in the rest of the board. We also see that this strong EMI is radiated at 580 MHz, corresponding exactly to the PDN anti-resonance.

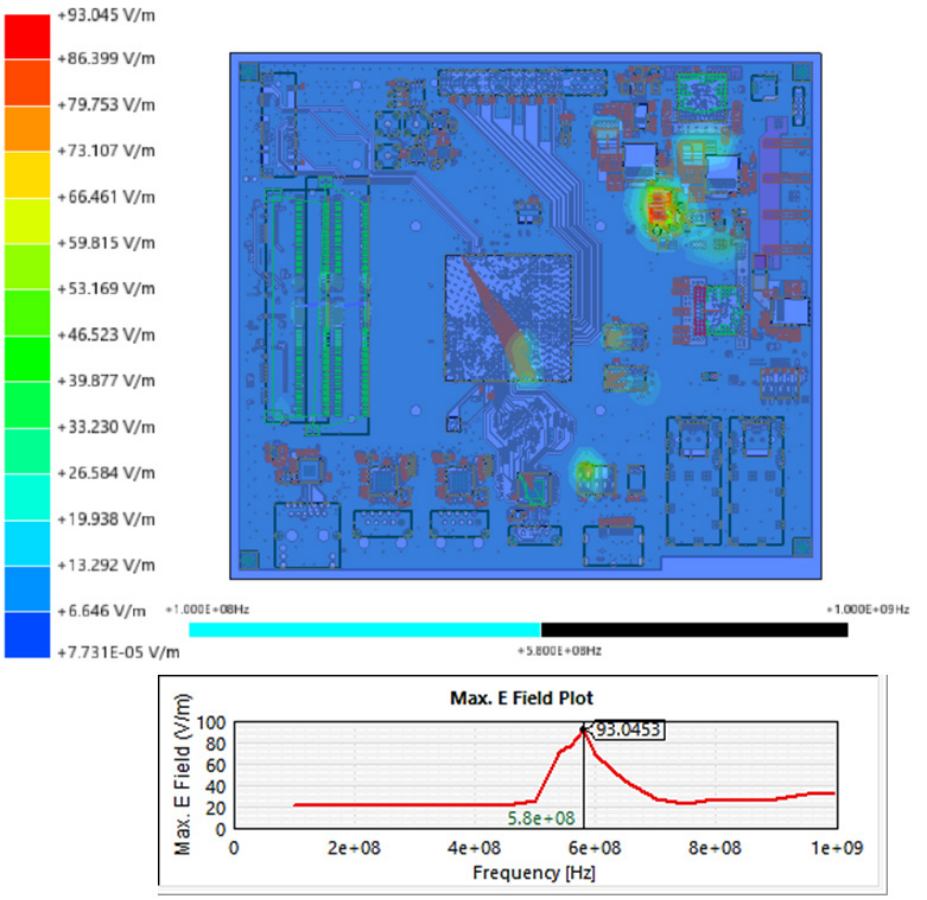


Figure 3: Simulated Near-field EMI distribution at the input to the PLL_1V8 net.

This motivates two possible solutions to reduce radiated EMI from the PLL_1V8 net:

1. Increase the lateral size of the power/ground plane pair to provide higher interplane capacitance.
2. Change the layer stackup so that the DDR nets do not reference the power plane.
3. Add decoupling capacitors with high self-resonant frequency to the surface layer to damp the anti-resonance in the PDN.

The third route is easiest as pursuing the first two routes in a finished layout could require extensive redesigns. After adding decoupling capacitors, the simulation can be run again and the results can be compared. Figure 4 shows a simulation of the Mini PC board after adding decoupling capacitors on the PLL_IV8 net in Altium Designer.

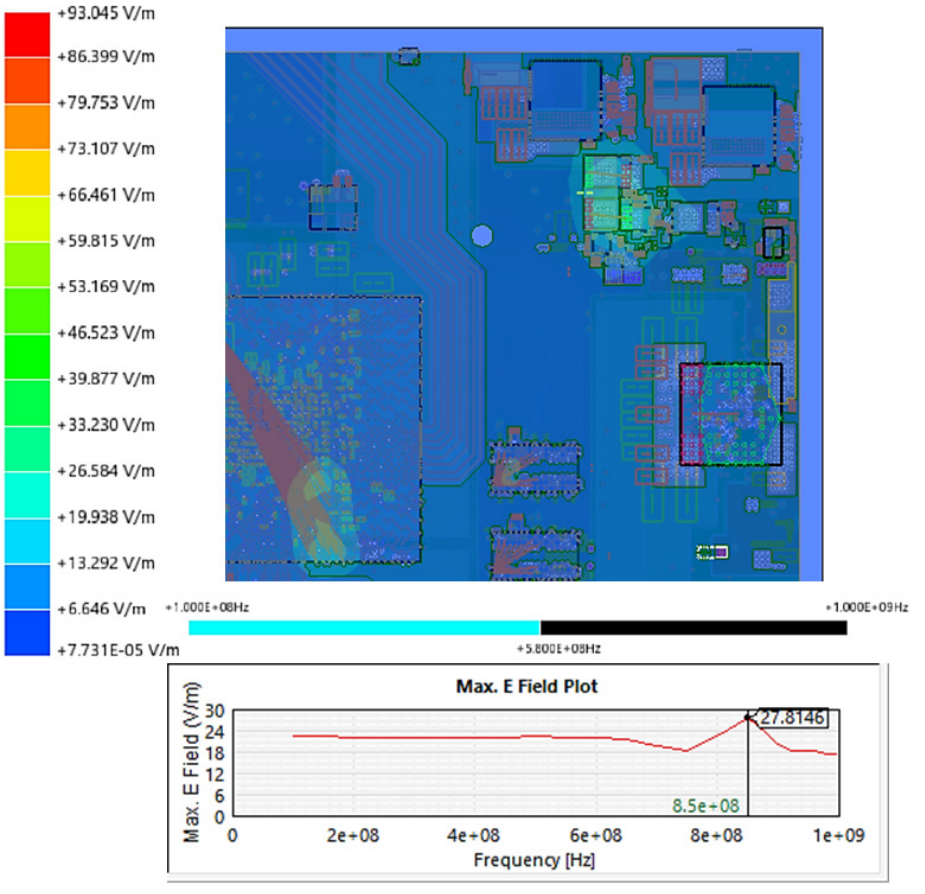


Figure 4: Simulated Near-field EMI distribution after adding decoupling capacitors.

This result shows that the radiated electric field at 580 MHz in the near-field regime is reduced by ~70% by merely adding decoupling capacitors to the PDN. Solving this PDN problem does more than address a near-field EMI issue; it also reduces phase noise/jitter coupled to other components connected to the PLL_1V8 net.

Summary

The Mini PC example project in Altium Designer was examined in Ansys SIWave to identify potential near-field EMI problems, and a severe problem with near-field radiated emission was located and resolved. By identifying PDN resonances in SIWave and adding some decoupling capacitors to the PDN in Altium Designer, the PDN impedance at the strongest anti-resonant frequency was reduced, thereby reducing the radiated electric field in the near-field regime by ~70%.

The integration provided by Ansys SIwave and Altium Designer makes this type of post-layout simulation workflow quick and easy thanks to Altium Designer's EDB Exporter extension. PCB designers can use this integration to create advanced PCBs and quickly run post-layout multiphysics simulations for their designs.

Register for the joint Altium and Ansys Webinar to learn more.

3D near-field EMI simulations with real PCBs can be complicated to prepare and implement without the right design and analysis tools. Altium Designer® can interface with Ansys SIwave® using the Ansys EDB Exporter extension, giving you a simple yet powerful way to run power integrity, signal integrity, and EMI analyses in the time domain or frequency domain with a variety of 3D field solvers.

ABOUT ALTIUM

Altium LLC (ASX: ALU) is a multinational software corporation headquartered in San Diego, California, that focuses on electronics design systems for 3D PCB design and embedded system development. Altium products are found everywhere from world leading electronic design teams to the grassroots electronic design community.

With a unique range of technologies Altium helps organisations and design communities to innovate, collaborate and create connected products while remaining on-time and on-budget. Products provided are Altium Designer®, Altium Vault®, CircuitStudio®, PCBWorks®, CircuitMaker®, Octopart®, Ciiva® and the TASKING® range of embedded software compilers.

Founded in 1985, Altium has offices worldwide, with US locations in San Diego, Boston and New York City, European locations in Karlsruhe, Amersfoort, Kiev and Zug and Asia-Pacific locations in Shanghai, Tokyo and Sydney. For more information, visit www.altium.com. You can also follow and engage with Altium via Facebook, Twitter and YouTube.