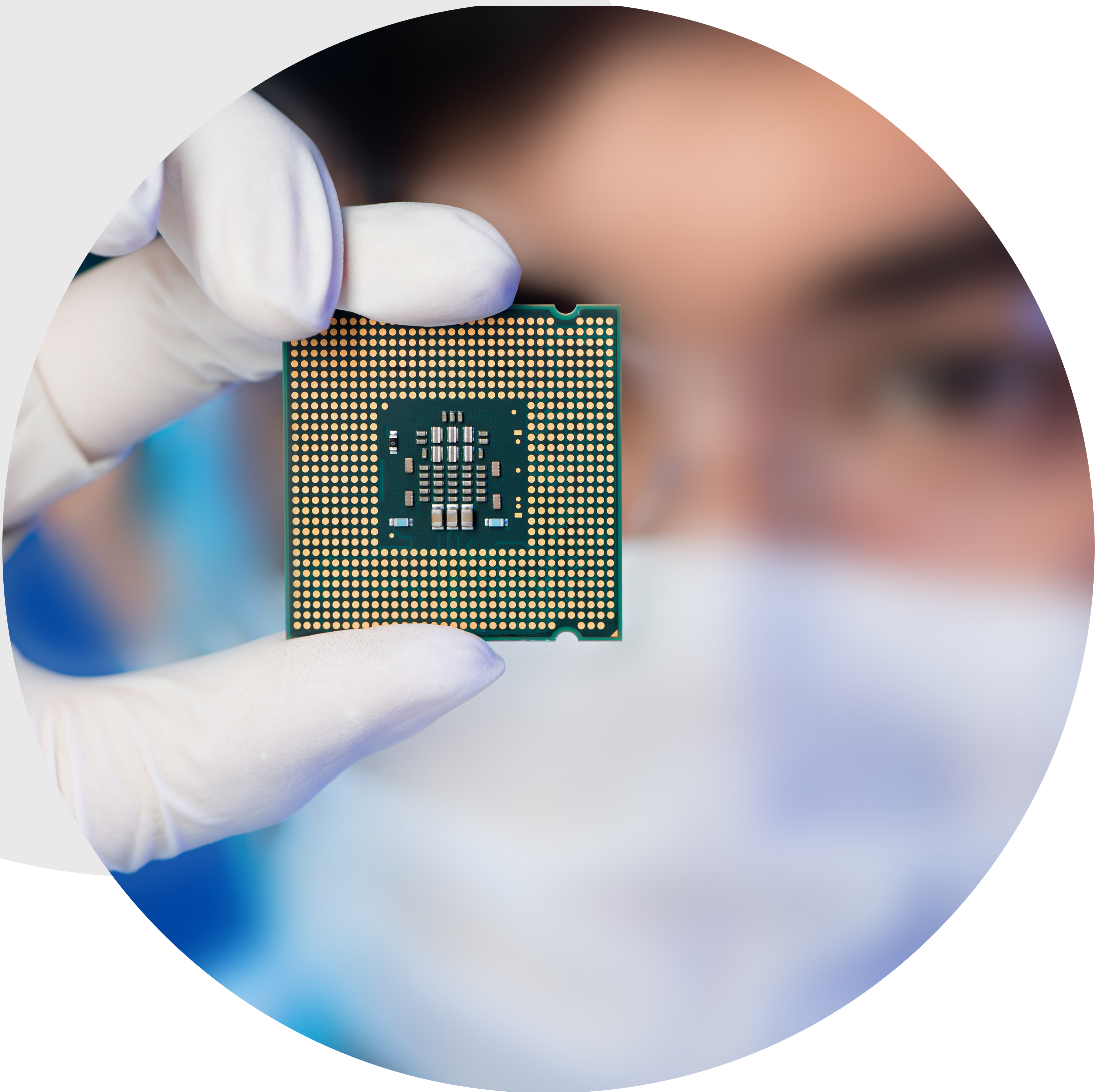

HDI PCB Design and Manufacturing Guide

An in-depth look at HDI PCB design

Altium®

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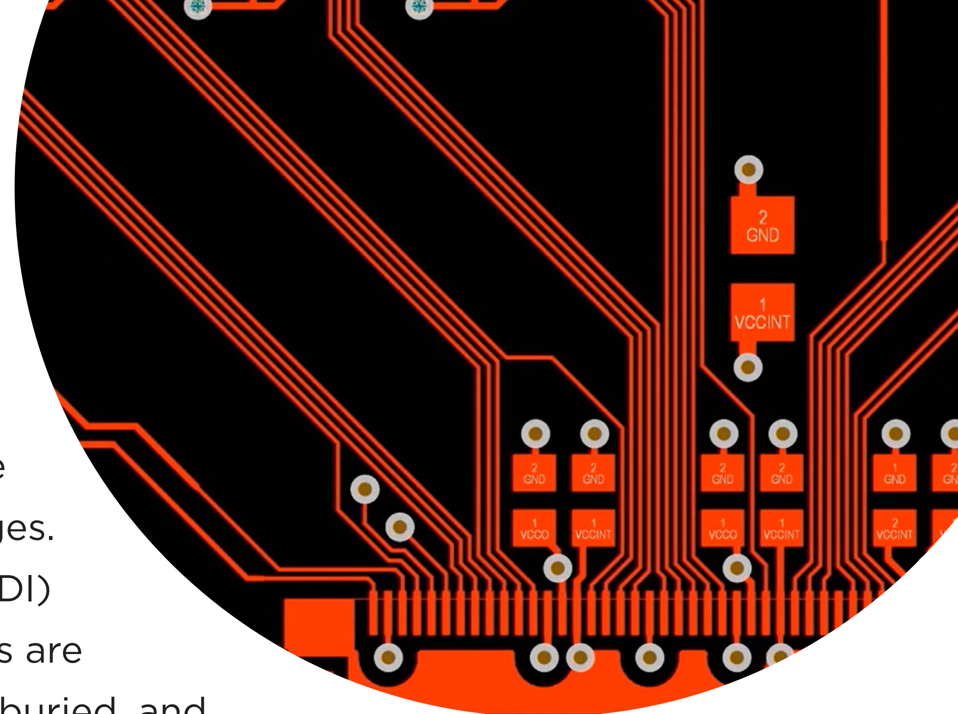
Design Basics for HDI and the HDI PCB Manufacturing Process



As the world of technology has evolved, so has the need to pack more capabilities into smaller packages. PCBs designed using high-density interconnect (HDI) techniques tend to be smaller as more components are packed in a smaller space. An HDI PCB uses blind, buried, and micro vias, vias in pads, and very thin traces to pack more components into a smaller area. We'll show you the design basics for HDI and how Altium Designer® can help you create a powerful HDI PCB.

High density interconnect (HDI) printed circuit design and fabrication started in 1980 when researchers started investigating ways to reduce the size of vias in PCBs. The first production build-up or sequential printed boards appeared in 1984. Ever since that time, designers and component manufacturers always look for ways to pack more functions on a single chip and a single board. Today, HDI design and fabrication are codified in the IPC-2315, IPC-2226, IPC-4104, and IPC-6016 standards.

When planning an HDI PCB design, there are some design and manufacturing challenges to overcome. Here is a short list of challenges you may run into when designing an HDI PCB:

- Limited board workspace area
- Smaller components and tighter spacing
- Larger number of components on both sides of PCB stackup
- Longer trace routes creating longer signal flight times
- More trace routes required to complete the board

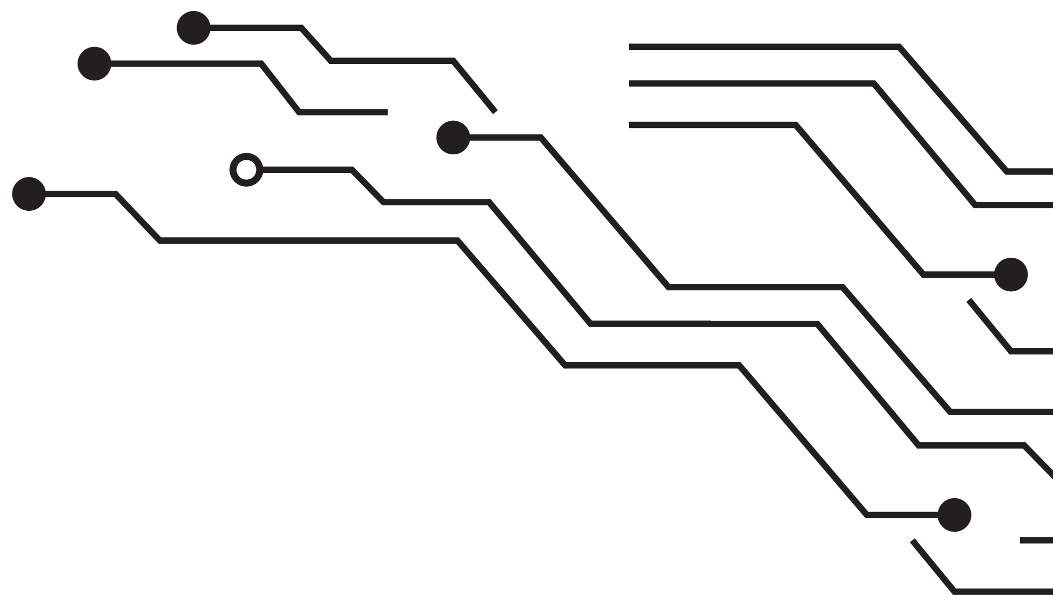
With the right set of layout and routing tools built on a rules-driven design engine, you can violate the normal rules in PCB design and create powerful PCBs with very high interconnect density. Working with high-density PCB routing and fine pitch components is easy when you use advanced PCB design software that is built for HDI PCB design. You can create your new HDI design and plan for the HDI manufacturing process with the world-class design features in Altium Designer.

What's Different About HDI PCB Design and Manufacturing?

The HDI manufacturing process differs from the traditional PCB manufacturing process in a few simple yet important ways. An important point here is that fabricator limitations will constrain design freedom and will set limits as to how the board can be routed. The use of thinner traces, smaller vias, more layers, and smaller components can still be accommodated in your design software, but accommodating design for manufacturing (DFM) requirements means taking advantage of automation in your design software. The exact DFM requirements depend on the manufacturing process and materials used to build the board. DFM requirements also become important when we consider reliability requirements.

Material selection needs to answer these questions:

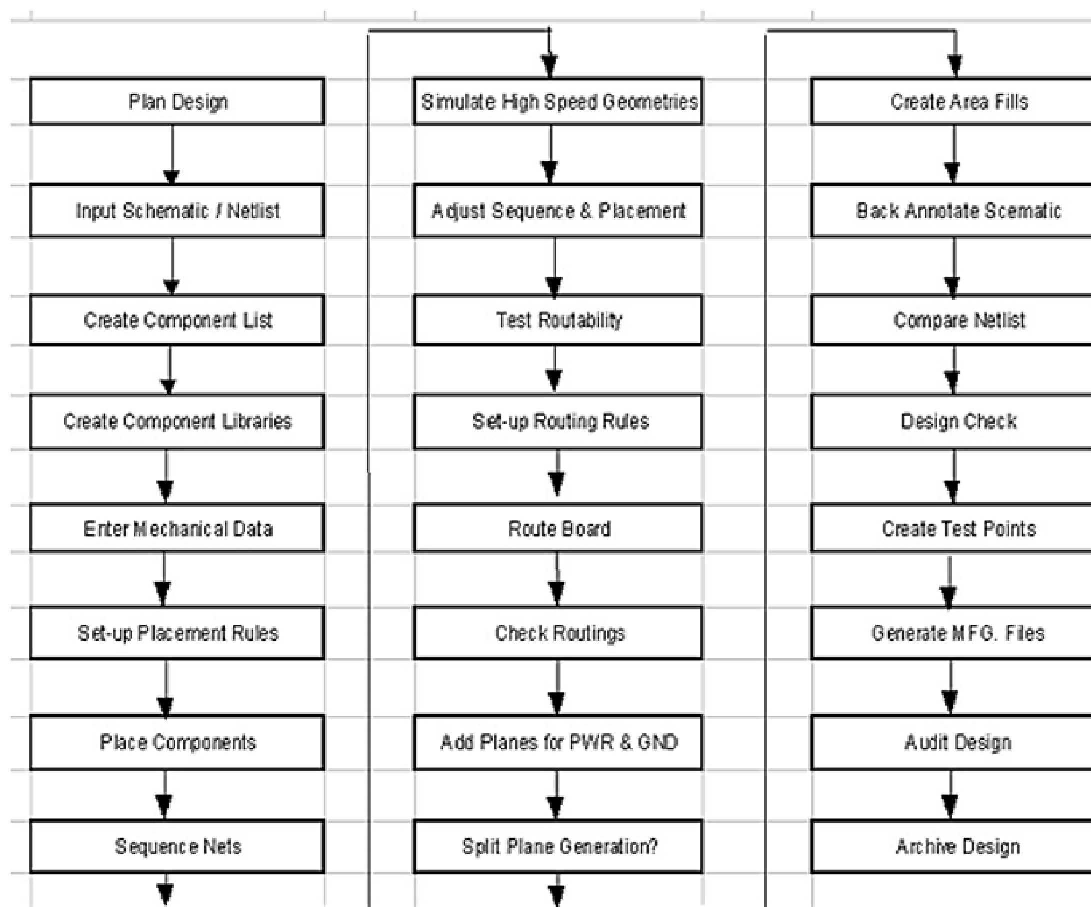
- Will the dielectric use chemistry compatible with current chemistry used by core substrate material?
- Will the dielectric have acceptable plated copper adhesion? (Many original equipment manufacturers [OEMs] want >6 lb./in. [1.08 kgm/cm] per 1 oz. [35.6 Qm] copper.)
- Will the dielectric provide adequate and reliable dielectric spacing between metal layers?
- Will it meet thermal needs?
- Will the dielectric provide a desirable "high" Tg for wire bonding and rework?
- Will it survive thermal shock with multiple SBU layers (i.e., solder floats, accelerated thermal cycles, multiple reflows)?
- Will it have plated, reliable microvias?



There are nine different general dielectric materials used in HDI substrates. IPC slash sheets like IPC-4101B and IPC-4104A cover many of these, but many are not yet specified by IPC standards. The materials are:

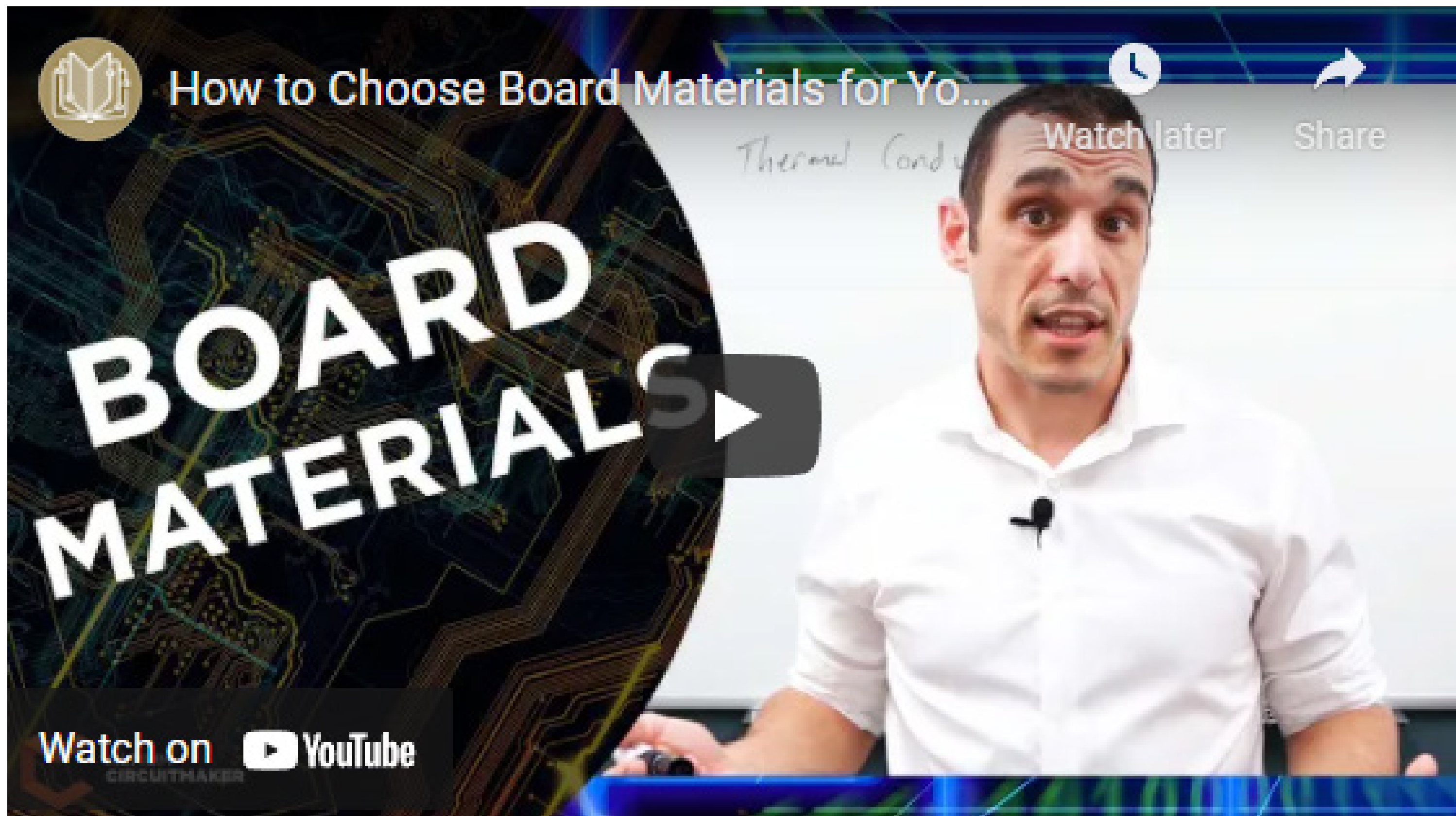
- Photosensitive liquid dielectrics
- Photosensitive dry film dielectrics
- Polyimide flexible film
- Thermally cured dry films
- Thermally cured liquid dielectric
- Resin-coated copper (RCC) foil, dual-layer and reinforced
- Conventional FR-4 cores and prepregs
- New ‘spread-glass’ laser-drillable (LD) prepregs
- Thermoplastics

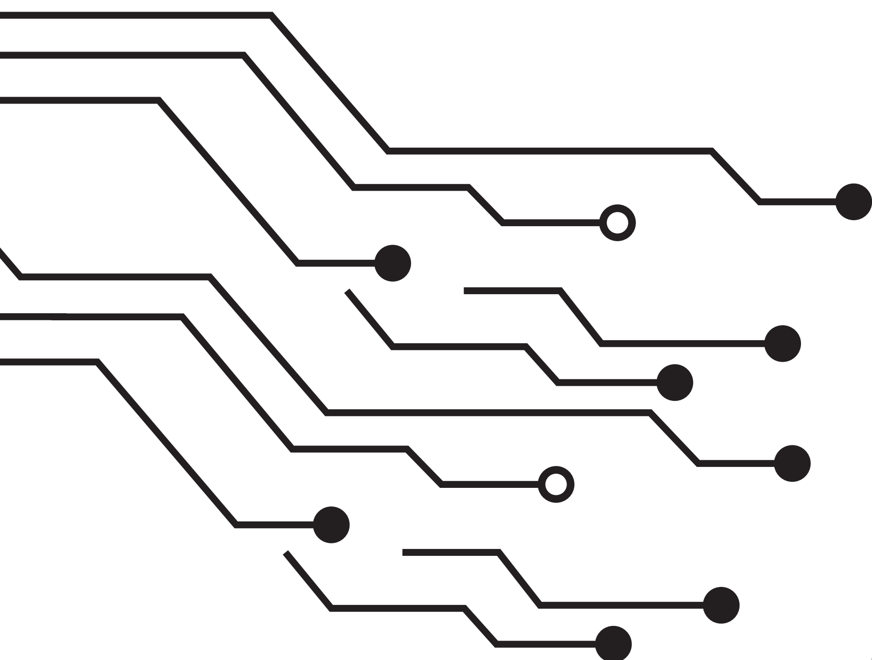
The HDI PCB design process is shown below. Routing efficiencies for HDI are dependent on stackup, via architecture, parts placement, BGA fanout, and design rules. The most important parts of planning your HDI layout are to consider your trace width, via size, and placement/ escape routing for BGA components.



General overview of the HDI PCB design and layout process.

Always check with your board house to determine their fabrication methods for HDI PCB manufacturing. You'll need to determine the limits of their fabrication methods as this will influence the feature sizes you can place in your layout. The ball pitch on BGA components will determine the via size you need to use, which then determines the HDI manufacturing process required to create the board. A central feature of your HDI PCB is microvias, which need to be precisely designed to accommodate routing between layers.





Overview of HDI PCB Design and Manufacturing Processes

There are a number of steps involved in the typical PCB manufacturing process, but HDI PCB manufacturing uses some particular steps that may not used in other boards. The HDI design process starts like many other processes, where the

1. Determine the layer count required to route all signals, either by using the largest BGA component on the board or by using the interface + direction count from the largest IC on the board.
2. Contact your fabrication house to select materials and obtain dielectric data to create your PCB stackup.
3. Based on layer count and thickness, determine the via style that will be used to route signals through inner layers.
4. Perform a reliability assessment if relevant, to verify that the materials will not stress interconnects to fracture during assembly processing and operation.
5. Determine design rules based on fabricator capabilities and reliability requirements (need for tear drops, trace widths, clearances, etc.) to ensure reliable manufacturing and assembly.

Stackup creation and determination of design rules are the critical points as they will determine ability to route the board and reliability of the end product. Once these points are completed, a designer can implement their fabricators DFM requirements and reliability requirements as design rules in their ECAD software. Doing this on the front-end is very important and it will help ensure the design is reliable, routable, and manufacturable.

Design Your Feature Size to Satisfy HDI DFM Requirements

Although DFM requirements relating to clearances in an HDI PCB are quite stringent, these can be accommodated by taking advantage of your design rules in your PCB design software. Some of the important DFM requirements to gather before layout and routing include:

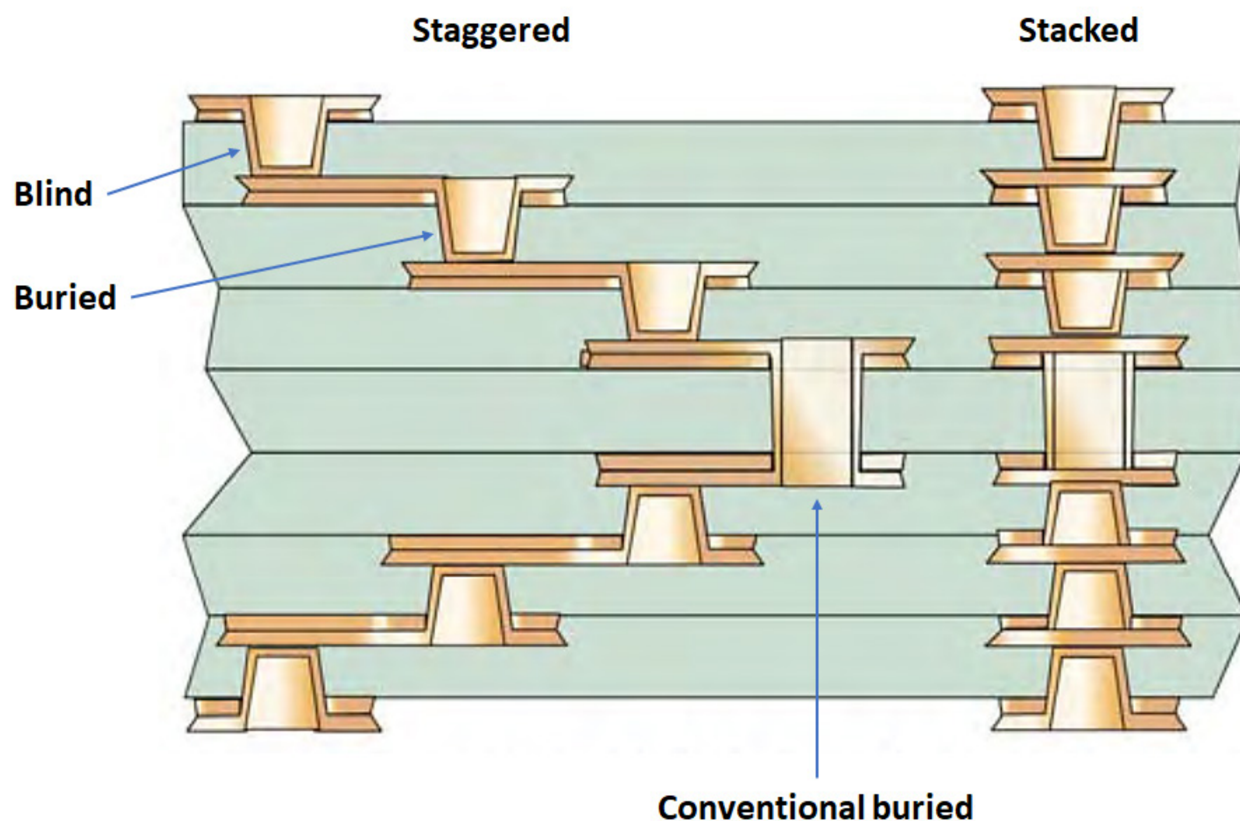
- Trace width and spacing limits
- Annular ring and aspect ratio limits, especially for high reliability designs
- Material system used in the board to ensure controlled impedance in the required stackup
- Impedance profiles for the desired stackup or layer pairs if available

Your design tools are critical for designing your HDI circuit board to satisfy these DFM requirements. Routing impedance controlled traces in your HDI PCB is quite easy with the right set of design tools. You simply create an impedance profile and define your desired trace width while keeping your manufacturer's DFM guidelines in mind. The online DRC engine in your routing software will check your routing as you create your HDI layout. Make sure you get a complete set of specifications for your fabricator's process to ensure you've taken into account all the relevant HDI DFM rules.

Types of Vias in HDI PCB Routing

The image below shows the typical via styles that are used in HDI PCB layout and routing. These via styles have low aspect ratio of)(ideally) less than 1, although some manufacturers may provide reliability claims up to aspect ratios of 2, including for stacked microvias. In the center of the PCB stackup is a conventional buried via to provide a connection through the thicker core layer; this inner layer buried via can have a larger aspect ratio as will be mechanically drilled with somewhat . Once the layer count and dielectric thicknesses are determined, the designer can design vias against the aspect ratio limits listed above. Obeying these aspect ratio limits on microvias is an important part of reliability, particularly as these boards pass through reflow, or when deployed in an environment with repeated thermal/ mechanical shocks and cycling.

Learn more about using microvias and their reliability in HDI PCBs



Sequential Buildup

The sequential lamination process is predominantly used to build an HDI stackup construction in a layer-by-layer manner. In general, this technique can be used for any multilayer PCB, but it is particularly important for HDI. This is because the high density, very thin dielectrics are formed in individual layers around a thick core, so lamination will happen in multiple steps to build the stackup. The sequential lamination process. This consists of the following steps:

- **Photoresist deposition and exposure:** This is used to define areas to be etched, which will leave behind a pattern of conductors on the laminate.
- **Etching and cleaning:** The current industry standard etchant is a ferric chloride solution. After etching, the leftover photoresist can be reclaimed and the resulting conductor pattern is cleaned.
- **Via formation and drilling:** Vias need to be defined using mechanical or laser drilling. For high via density, the via holes can be removed chemically.
- **Via metallization:** Once vias are defined, they are metallized to form a continuous conductive interconnect.
- **Buildup:** Layers are stacked in multiple lamination cycles to build the stackup before outer layer processing.

A flow chart showing the buildup process can be found in the Metalization section below.

Via Formation in HDI

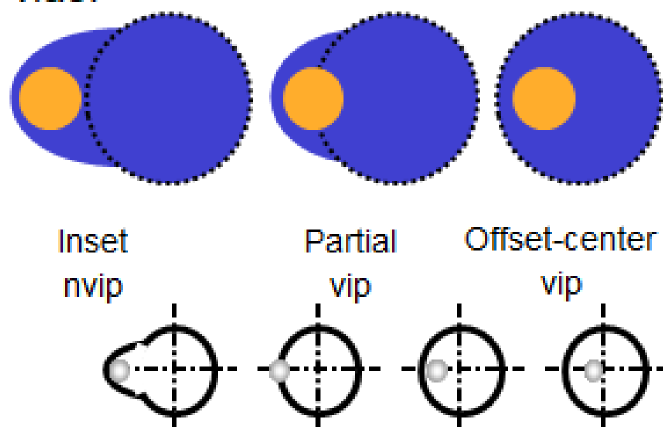
HDI PCBs will require interconnects that typically hit the lower limit of the via size that can be placed in a PCB with mechanical drilling. Once via holes get smaller than 6 mils, an alternative via formation process is needed to place microvias between layers. As filled plated microvias are a standard feature on HDI PCBs, they can be used in a via-in-pad design approach to help increase density. Using via-in-pad is an easy way to pack more components into a design as they provide a direct connection from a component lead into an internal layer.

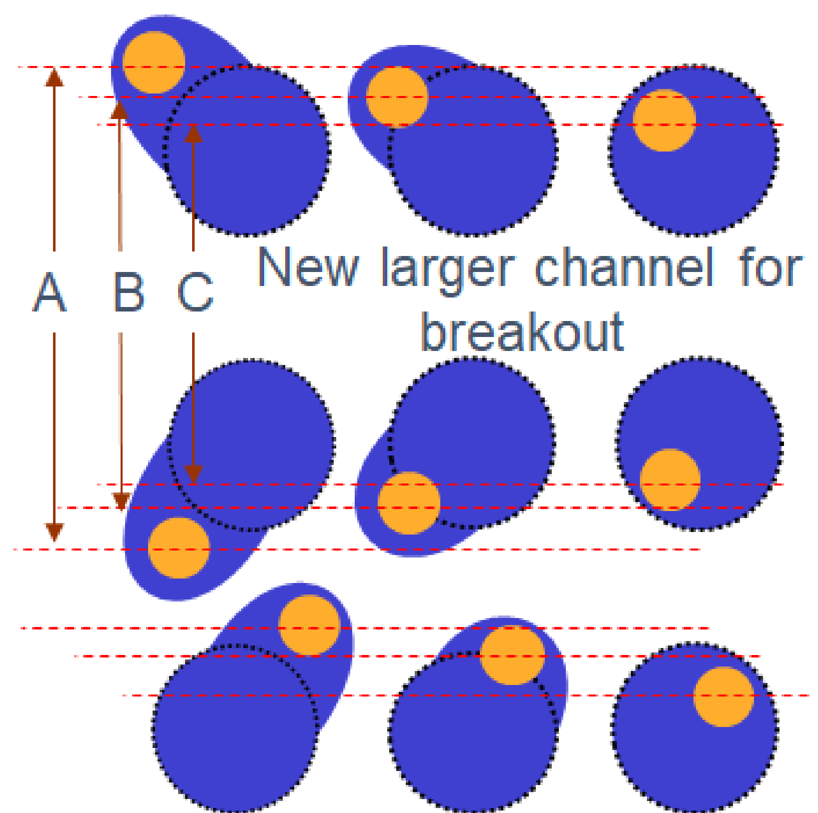
Whenever there are reliability concerns regarding microvias, a near-pad technique can also be used, where a very small trace section comes off from a pad and touches the microvia. This completes the connection to an internal layer and provides a larger breakout channel should drill wander create some deviation from the desired drill hit location.

Learn more about laser-drilled via-in-pad technology

(Near) Via in pad techniques

μvias many times should have multiple angles, in order to maximize the routing channels on the layer below and how it might be connected to buried vias.





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Via-in-pad design styles for HDI PCBs.

Metalization

During the sequential lamination process, each layer in an HDI PCB will go a via metalization, fill, and plating process. The resulting vias must be void-free in the internal body with sufficient wrap plating around the neck so that cracking can be avoided during reflow cycles and during operation. There are four via metallization processes that are used in HDI manufacturing. These methods are:

- Conventional electroless and electroplating copper
- Conventional conductive graphite or other polymers
- Fully and semi-additive electroless copper
- Conductive pastes or inks

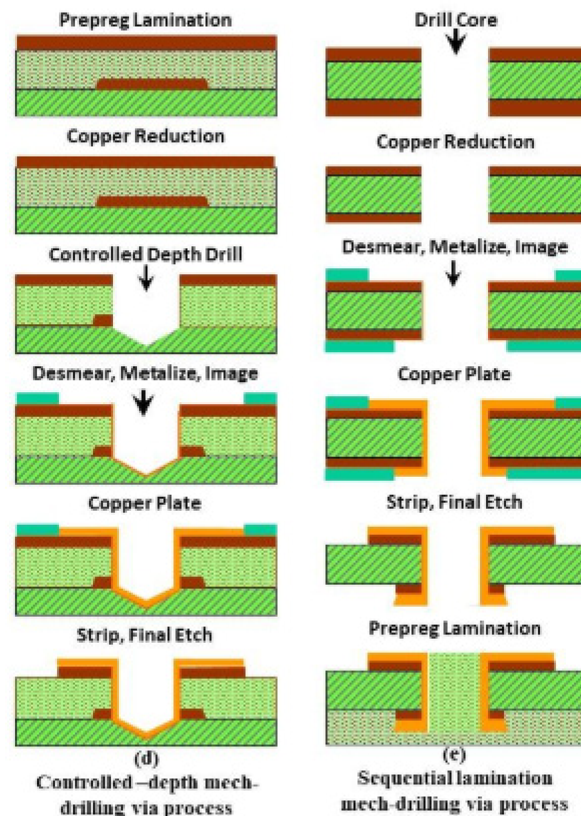
Larger vias can be drilled, but the costs eventually exceed laser drilling costs with lower throughput as a slower drilling speed is required. Laser drilling is by far the most popular microvia hole formation process, but it is not the fastest via formation process. The chemical etching of small vias is the fastest, with an estimated rate of 8,000 to 12,000 vias per second. This is also true of plasma via formation and photovia formation.

In laser drilling, a high fluence beam is used to place a hole in a PCB laminate. Lasers are capable of ablating dielectric material and stopping when intercepting the copper circuitry, so they are ideally suited for creation of depth-controlled blind vias. The wavelengths for laser energy are in the infrared and ultraviolet region. A beam spot size as small as approximately 20 microns

Learn more about microvia manufacturing techniques in the HDI manufacturing process

If the vias in the board are wide enough to drill, a controlled drilling step may be used to place vias. This requires an intermediate sequential lamination step to bond two layers of the board, followed by drilling and plating to define the via barrel, connection to the inner layer, and landing pad on the upper layer. These vias might also be filled before the next sequential lamination step (if they are on the inner layers), or they could be left un-filled if kept on the outer layers.The overall drilling and sequential process is shown below.

Learn more about HDI manufacturing processes on standard materials



Microvia drilling and metalization processes in an HDI manufacturing process.

Getting Your Board into the HDI Manufacturing Process

HDI PCB processes are more advanced than traditional rigid PCB processing steps, but they still use the same set of fabrication data you use for a typical rigid PCB. Once you've finished your HDI PCB layout and it's passed a DFM review, it's time to prepare deliverables for your fabricator and assembler. The unified design environment in Altium Designer takes all your design data and uses it to create Gerbers/ODB++/IPC-2581 fabrication files, drill tables, a bill of materials, and assembly drawings for your new HDI PCB.

When you're looking for the best software package for HDI PCB design, layout, and manufacturing, use the complete set of design tools in Altium Designer®. The integrated design rules engine and Layer Stack Manager give you everything you need to create your bare HDI circuit board, calculate impedance values, and account for copper roughness in your PCB material system. When you've finished your design, and you want to release files to your manufacturer, the Altium 365™ platform makes it easy to collaborate and share your projects.

What's Different in HDI?

Defining Interconnect Density

When planning an HDI design, there are measures of performance or metrics for the HDI process. Like the triangle in Figure 1, these three vital chains of the HDI Process are elements of interconnection density.

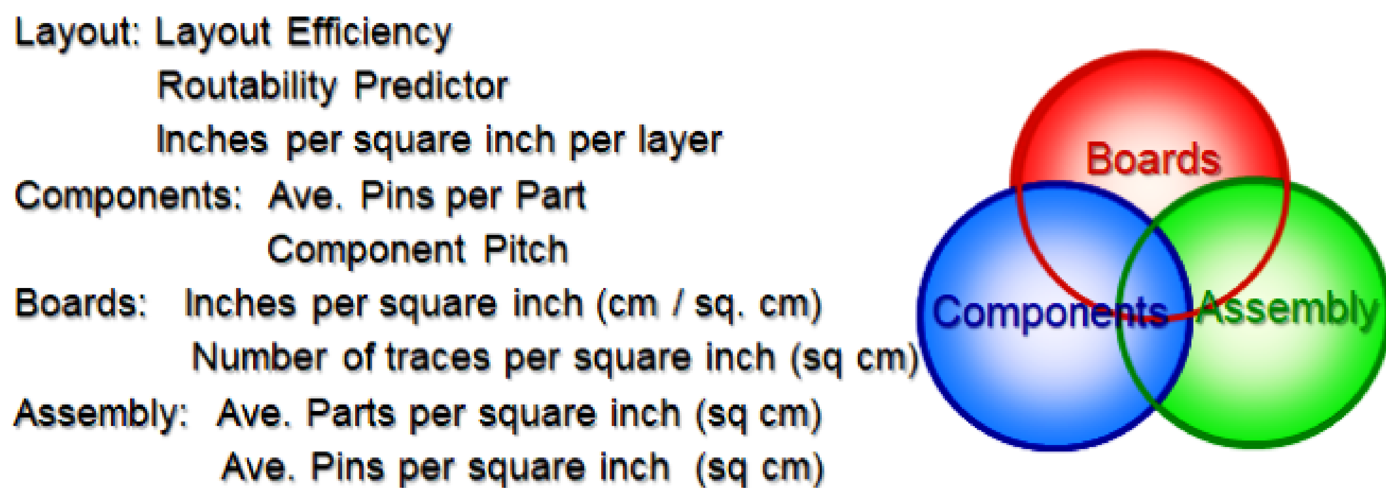


FIGURE 1. HDI Design Metrics

Assembly Complexity

Two measures of the difficulty to assemble surface mounted components, Component Density (Cd), measured in parts per square inch (or per square centimeter.) and Assembly Density, (Ad), in leads per square inch or per square centimeter.

Component Packaging

The degree of sophistication of components, Component Complexity, (Cc), measured by its average leads (I/Os) per part. A second metric is component lead pitch.

Printed Wiring Board Density

The amount of density (or complexity) of a printed circuit, Wd, as measured by the average length of traces per square inch of that board, including all signal layers. The metric is inches per square inch. or cm per square centimeter. A second is the number of traces per linear inch or per linear cm. The PWB density was derived by assuming an average of three electrical nodes per net and that the component lead was a node of a net. The result was an equation that says the PWB density is times the square root of the parts per square inch times the average leads per part. ? is 2.5 for the high analog/discrete region, 3.0 for the analog/digital region and 3.5 for the digital/ASIC region:

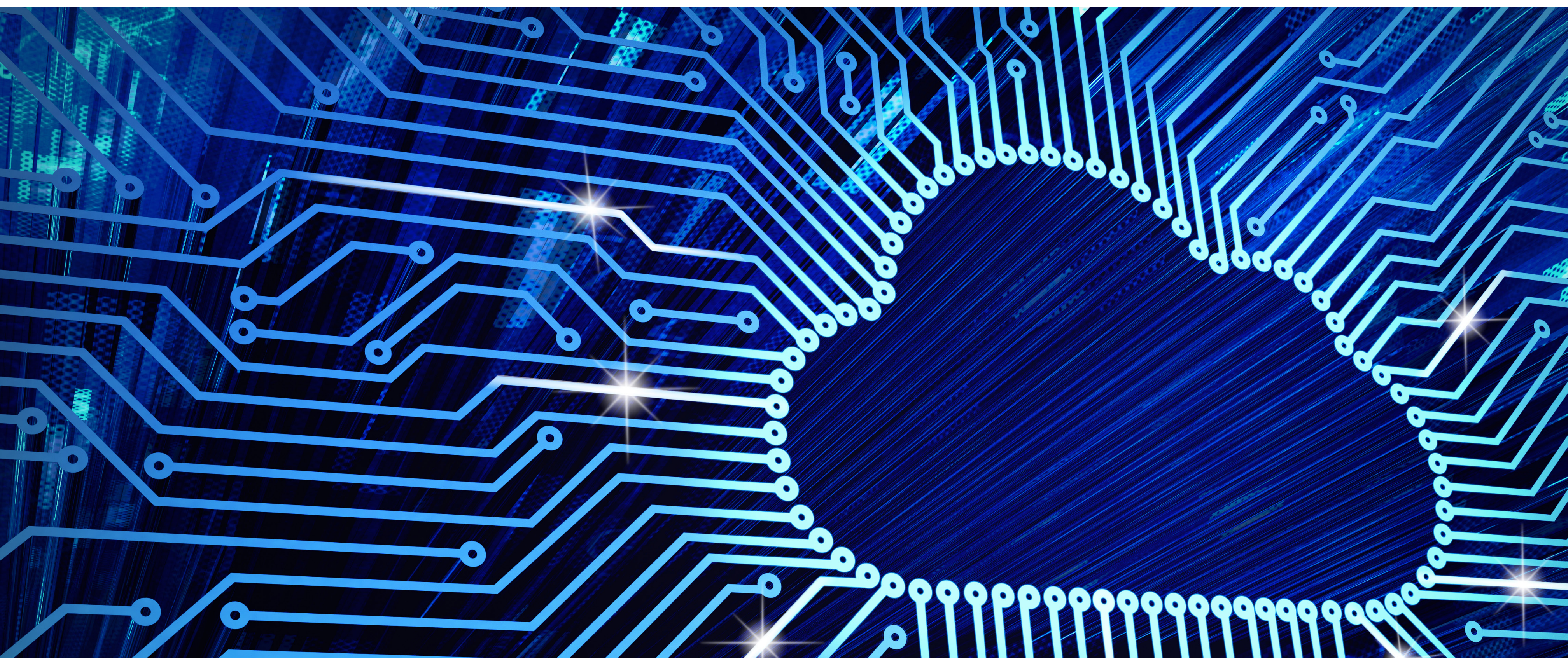
PWB Density (Wd) = ? ffl [Cd] x [Cc]

= ? ffl [parts per sq. in.] x [ave.leads per part]

Where: p = Number of components (parts)

l = Number of leads for all the components

a = Area of the top surface of the board (square inches)



Packaging Technology Map

Figure 2 is what I call a Packaging Technology Map. The Packaging Technology Map was first displayed by Toshiba in January of 1991. [1].

A second valuable feature of the map is the area of upper-right. This is the "Region of Advanced Interconnections". This is where it is necessary to have an HDI Structure. The dashed lines indicate the barrier or wall of HDI! Cross this and it now becomes cost effective to use HDI. Move too far and it becomes a necessity.

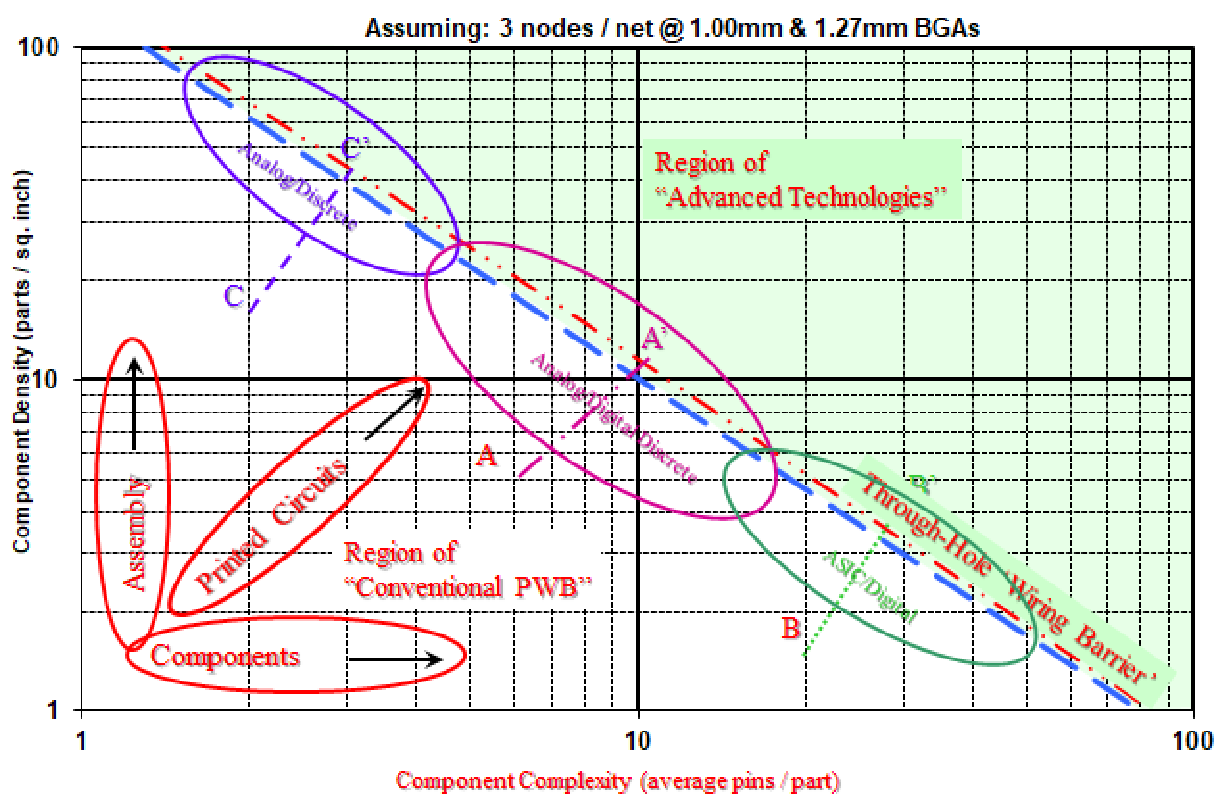


FIGURE 2. The through-hole (TH) wiring barrier as a function of a typical assembly

The packaging map is created by measuring an assembly size, number of components and the leads those components have. The components include both sides of an assembly as well as edge fingers or contacts. By the simple division of leads by parts and parts by area of the assembly, the X and Y-axis are known. Plotting the components per square inch (or components per square centimeter) against average leads per component on a log-log graph the PWB wiring density in inches per square inch (or centimeters per square centimeters) and Assembly Complexity (in leads per square inch or leads per square centimeter) can be calculated. The Assembly density is just the X-axis times the Y-axis.

Through-Hole Wiring Barrier

When the chart (Fig. 2) is used to analyze surface mount assemblies, three major zones show up on the packaging chart, which is why I call it a Map. The first is products with a high content of analog devices and discrete components. Typical products are camcorders, pagers and cellular telephones (C-C'). They have the highest assembly complexity. Up to 300 to 400 leads per square inch (47 leads per square centimeter). The second group is products with a high degree of digital components and some mixed discretes. Notebook computers, desk tops, instruments, medical equipment and telecom routers are examples (A-A'). The last group has a highly integrated use of ICs. PCMCIA, flash memory, SiPs and other modules are typical of this group (B-B'). This group has the highest PWB wiring density of over 160 inches per square inch (25 centimeters per square centimeters). The Figure loosely shows the three regions.

When you look at the Figure, the Assembly Complexity lines cross the Wiring Density lines. At high discreet levels, less wiring is required for the amount of assembly density. At high ASIC (and low discreet) levels, much more wiring is required to connect the components. This makes assembly metrics like leads per square inch a good indicator, but not adequate to substitute for the PWB wiring density.

The General Process of PCB Design

The process of PCB design utilizing HDI technology is shown in Figure 3. When designing with HDI technologies, the first step – [Plan Design] is the most important. Routing efficiencies for HDI is dependent on stackup, via architecture, parts placement, BGA fanout and design rules, as seen in Figure 4. But the entire HDI Value Delivery Chain must be taken into consideration, including fabrication yields, assembly considerations and in-circuit test. Working with your PWB fabricator and assembler is essential for a successful design.

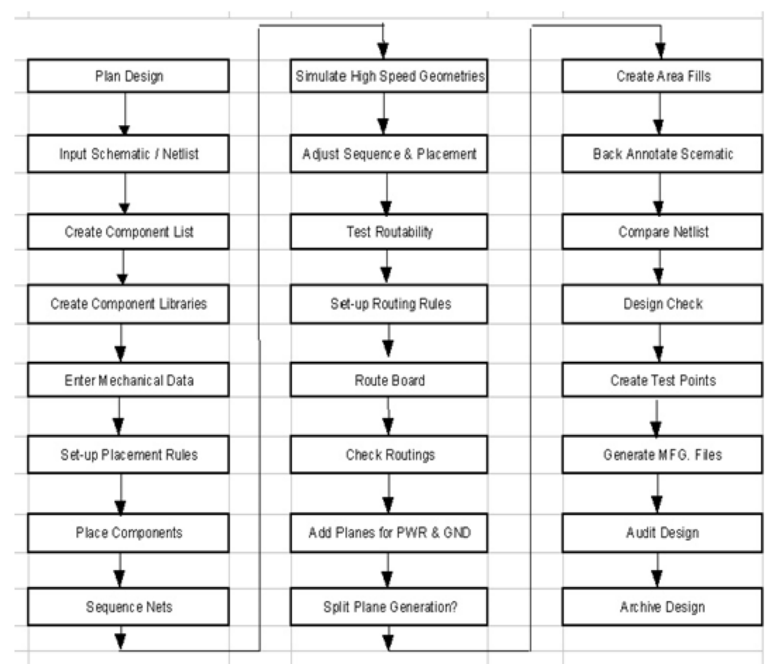


FIGURE 3. A general overview of the PCB design and layout process

HDI Standards, Guidelines, Specifications and References

When approaching HDI design, the place to start is with the IPC Guidelines and Standards. Four apply specifically to HDI design, as seen in Figure 5.

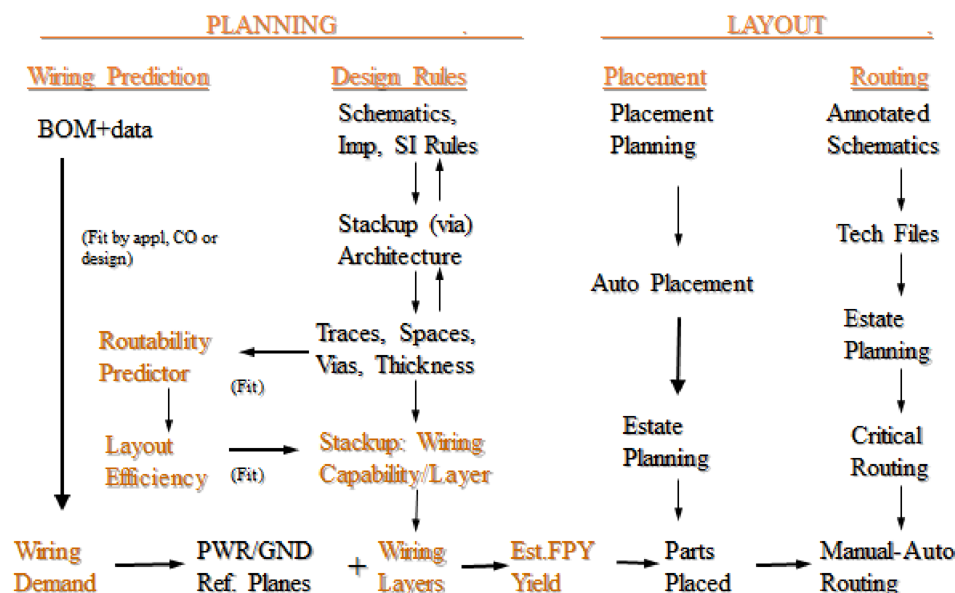


FIGURE 4. A recommended HDI planning process to add the general PCB design process

- IPC/JPCA-2315: This is an overview of HDI and provides models for estimation design density.
- IPC-2226: This specification educates users in microvia formation, selection of wiring density, selection of design rules, interconnecting structures, and material characterization. It is intended to provide standards for use in the design of printed circuit boards utilizing microvia technologies. [2]
- IPC-4104: This standard identifies materials used for high-density interconnection structures. The IPC-4104 HDI Materials Specifications contain the slash sheets that define many of the thin materials used for HDI. The slash sheets of materials characteristics are divided into three main materials types: Dielectric Insulators (IN); Conductors (CD) and Conductor and Insulators (CI).
- IPC6016: This document covers the performance and qualification for high-density structures.

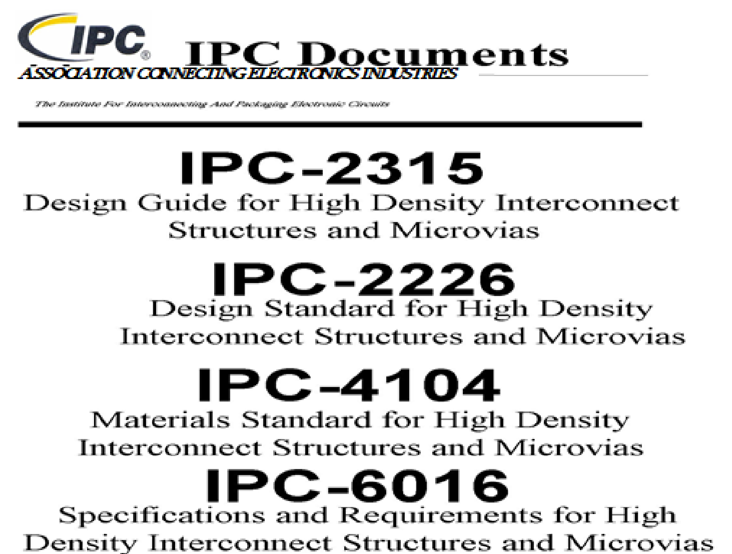


FIGURE 5. IPC standards and guidelines

What's Different in HDI Design

Three (3) New Principles

There are three (3) new principles for HDI-microvia design that don't exist in TH design:

Microvias must replace TH vias, not just used '"in addition to" TH vias.

- Consider new layer stackups that allow the elimination of TH vias.
- Place microvias in such a way that they create channels and boulevards for improved routing. (see Table 1)

Microvias Replacing Through Holes (TH)

The main idea is that microvias replace or allow the removal of TH vias, thus allowing the routing density on inner layers to improve by 2X or 3X, using the space the TH vias used to occupy. This will allow fewer signal layers and fewer reference layers for those signal layers.

This principal is more profound than it first appears. This is because there are three dimensions on how the microvias are placed, see Figure 6):

- **Use of Microvias in Place of Through-Holes**
- **Layer Stackup Changes to Eliminate Drilled Holes**
- **Using the Blind Vias to Form Channels**
- **Placing the Blind Vias to Open Up Boulevards**

TABLE 1. New principles for HDI design not used for TH multilayers

- The blind-vias can be "shifted or swung" in the X-Y or theta () angle to create more routing space
- The blind-vias can be placed on inner layer (3D) to further create more breakout spaces
- The center-to-center distance can be altered on inner layers to provide additional space for traces.
- If all of this is happening on or near the Primary Side, then there will be space created under the BGA on the Secondary Side for traces or more important, for discretes like decoupling capacitors.

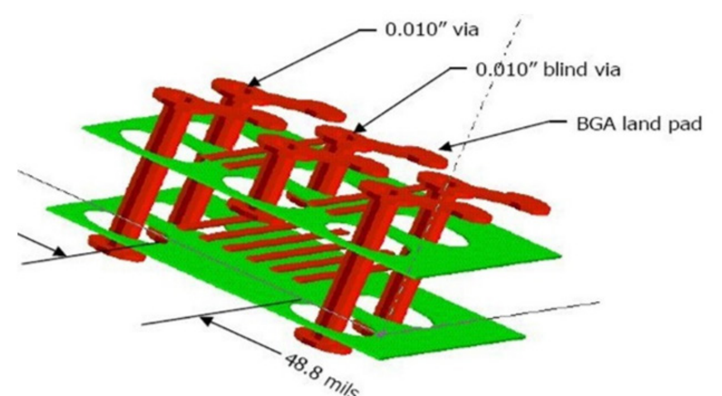


FIGURE 6. Illustration of the benefits for routing by using blind vias

Layer Stackup Alternatives

If you study the first Principle and ask yourself, “What jobs do my vias do?”. The answer is that the most common via on a PWB are the vias to GND. “The second most common via?”, the answer is obvious, it’s the vias to PWR. Thus, moving the GND plane that usually is Layer-2 up to the surface provides the opportunity to eliminate all those vias to GND. In the same vein, moving the most used PWR plane up to Layer-2 will replace those THs with blind vias. These provide four (4) advantages over the conventional ‘microstrip’ stackup, as seen in Figure 7:

- There are no fine-lines to plate or etch on the surface.
- The surface can be an unbroken GND pour to reduce EMI and RFI (faraday cage)
- The closer Layer-2 (PWR) is to Layer-1 (GND) the more planar capacitance is available and the lower is the PDN planar inductance.
- The energy stored in the planar capacitance can be delivered to components with the lowest series inductance available, providing for the elimination of most of the decoupling capacitors.

Figure 7. shows some of the most common HDI stackups to reduce the number of TH vias. The three common HDI stackups are shown with the IPC-Type structures (I, II & III).

The possible dielectrics available between Layer-1 and Layer-2 can be conventional prepregs, laser-drillable prepregs, RCCs, reinforced RCCs or BC cores. These materials are described in Chapter 2 -HDI Materials. If the dielectric is thin, then it is practical to also utilize a ‘skip-via’ from Layer-1 to Layer-3, thus saving the cost of not having to utilize a IPC-Type III structure. Even if a thin dielectric is not employed, any dielectric thickness less than 0.005 inch (<0.125mm) will couple GND to PWR and provide a lower power supply (PS) impedance, as well as reducing PS resonances and noise.

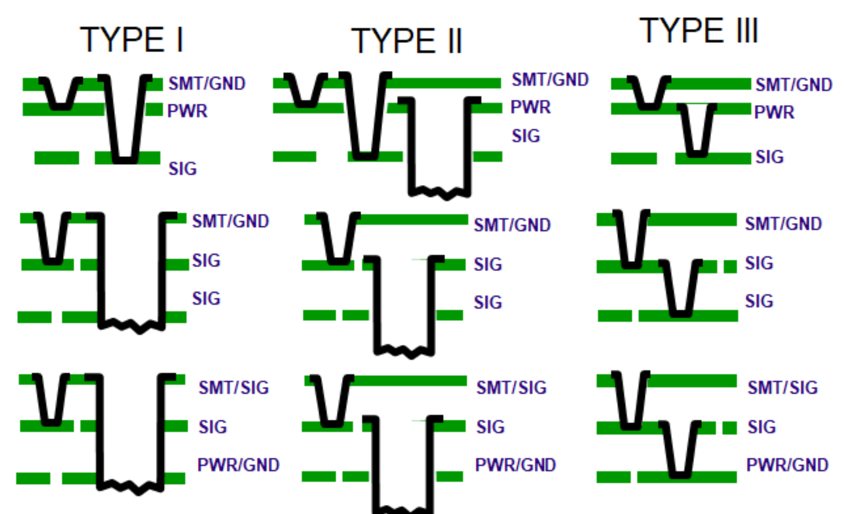


FIGURE 7. Three alternative surface layer stackups compared to IPC-Type I, II & III structures

Placing blind vias to open larger boulevards

One useful HDI design technique is to use blind vias to open up more routing space on the inner layer. By using blind vias between the through-vias, the routing space effectively doubles on the inner layers,

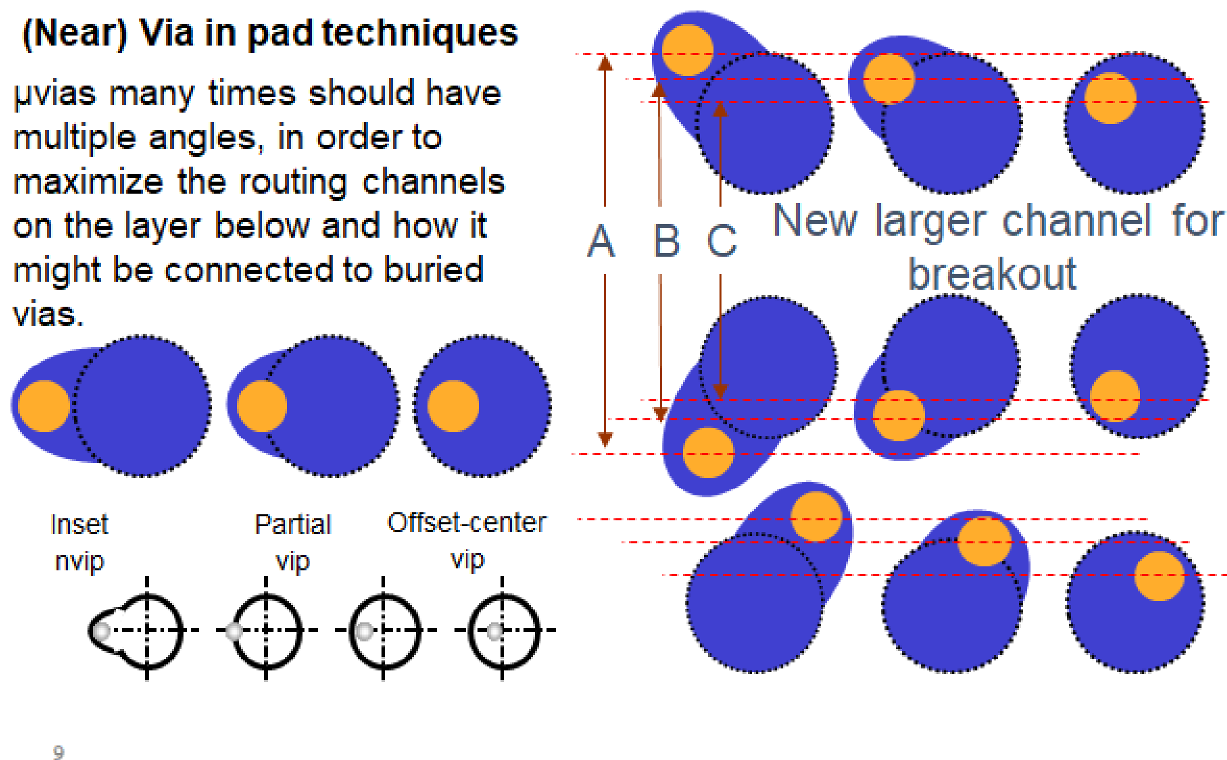


FIGURE 8. Near-via-in-Pad definition and swinging the ViP to create channels for routing

allowing for more traces to connect pins on the inner rows of a BGA. As seen in Figure 6, for this 1.0 mm BGA, only two traces can escape between vias on the surface. But beneath the blind vias, now six traces can escape, increasing the routing by 30%. With this technique, one fourth the number of signal layers is required to connect a complex, high-I/O BGA. Blind vias are arranged to form boulevards either in a cross, L-shaped or diagonal formation. Which formation to use is driven by the power and ground pin assignment. This is why, for a FPGA, reprogramming the placement of power and ground pins can be so productive.

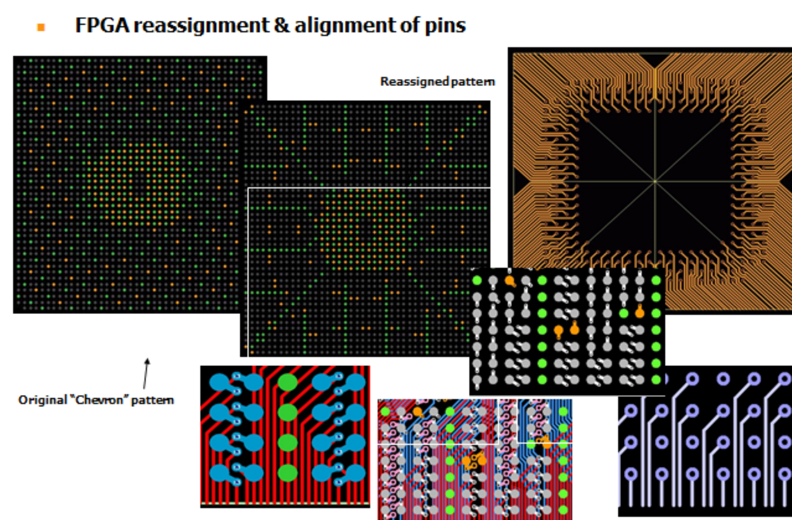


FIGURE 9. Blind vias can be used to form boulevards in inner layers allowing 30% more routing out of the BGA

The microvia used for BGA fanout was shown in Figure 9. The microvia can be placed outside the BGA land (inset), partially in/out of the land (partial vip) or completely in 'the pad' (vip)-see Figure 10.. If placing the via-in-pad, then the via should always be 'off-center' and not placed in the direct center of the land. This is to minimize any trapped air 'voids' during soldering. If the via is placed in the center of the BGA land, and it is not-filled, when the solder paste is applied on the land, and the BGA placed on the paste-land, during reflow, as the solder melts, the BGA ball drops and traps any air that may be there, much like a 'cork in a bottle'. By placing the via 'off-center', the air has a chance to escape as the solder melts and flows into the microvia.

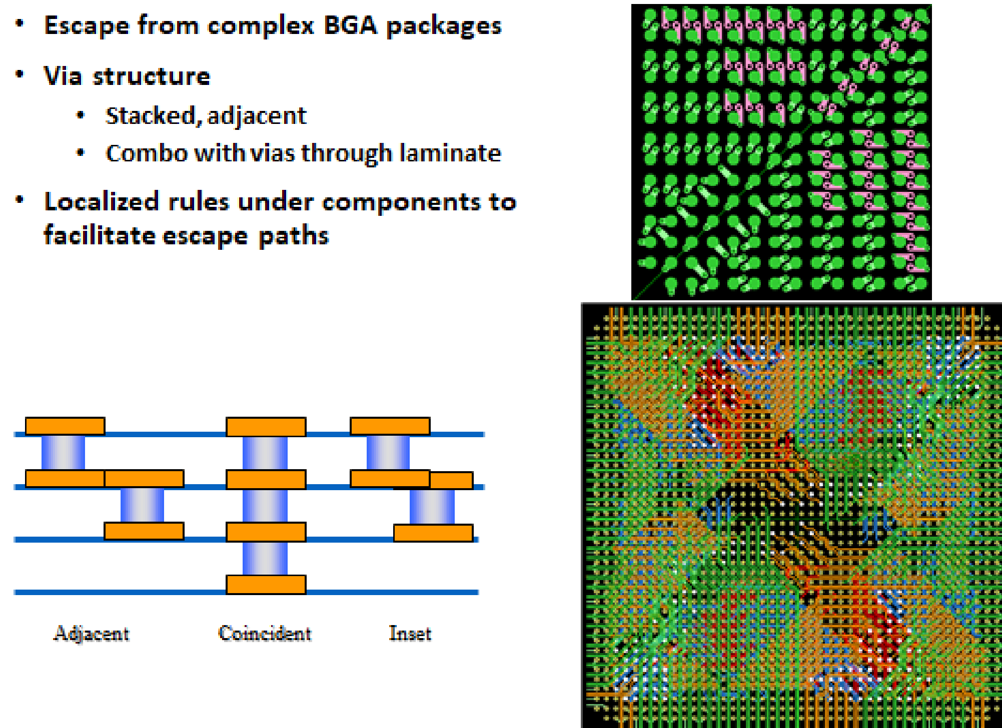


FIGURE 10. blind-via alternatives

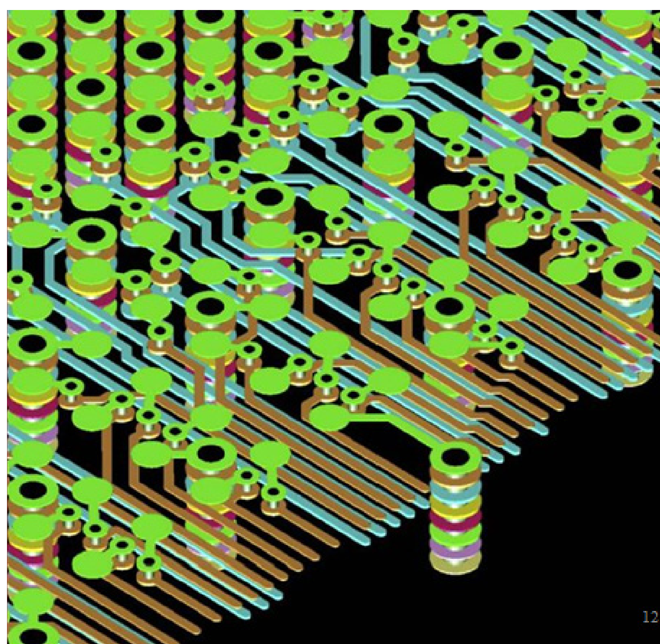


FIGURE 11. Fancy 3D view of 'swing-vias' connecting to buried-vias and through-holes

Introduction to High Density Interconnects

This article outlines the advanced design approaches and manufacturing processes needed to design the most complex of these PWBs, the high-density interconnects (HDI).

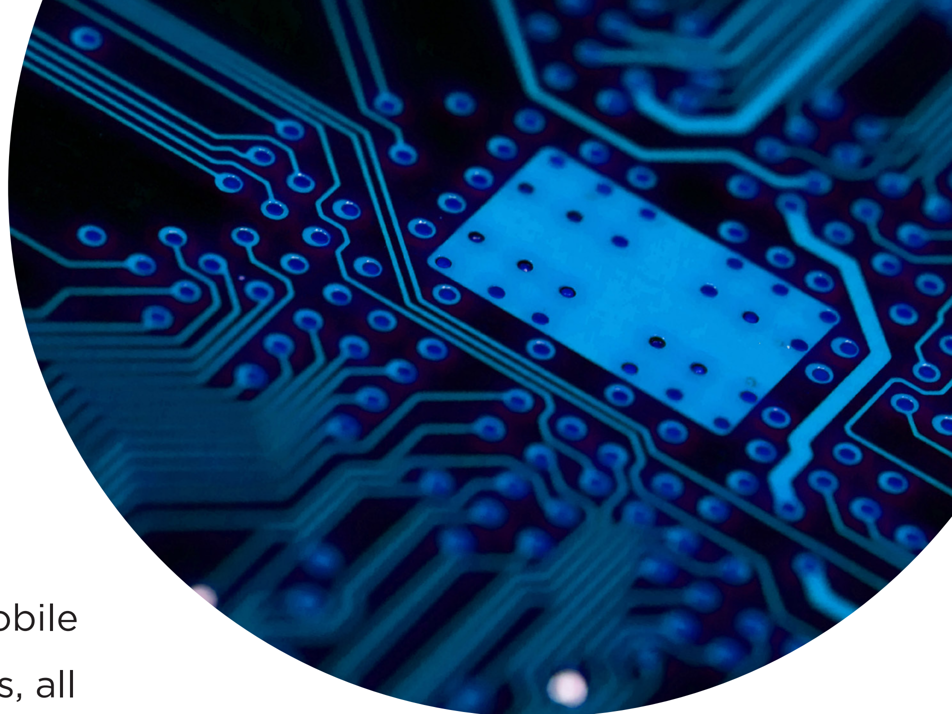
The Evolution of Electronics

Electronics is a relatively new industry since it has been only 65 years since the transistor was invented. The radio tube was developed nearly 100 years ago but blossomed in WWII, with communications, radar, ammunition fusing (especially the radar-altimeter electronic fusing for the first atom bomb) and has evolved into the world's largest industry. All electronic components must be interconnected and assembled to form a functioning unit. Electronics packaging is the technology where we integrate the design and manufacturing of these interconnections. Since the early 1940s, the basic building platform of electronic packaging is the printed circuit board (PCB). This Guidebook outlines the advanced design approaches and manufacturing processes needed to design the most complex of these PWBs, the high-density interconnects (HDI), as illustrated in Figure 1.

This chapter introduces the basic considerations, the main advantages, and the potential obstacles that must be accounted for in the selection of the high-density interconnection methods. Its main emphasis is on the interconnections and wiring of components. The focus is on density and the potential effects that the selection of various HDI board types and design alternatives could have on the cost and performance of the complete electronic assembly.

As printed circuits became more commonplace since the early 50s, the density and complexity of interconnects have increased quickly, but not as much as the last ten years. Conventional printed circuit technology is capable of meeting most of today's requirements. Yet, there is a growing group of products referred to as "High Density Interconnects" (HDI for short) that are used to create still denser interconnect, and it is these that are the subject of this Guidebook.

Interconnect Trends



Drivers for higher-density interconnection come under three headings; platforms, performance, and parts:

Platforms

With fast-growing markets for products such as mobile phones, digital appliances, and wearable computers, all of which represent new opportunities. HDI makes possible electronics becoming smaller and lighter.

Performance

With decreased semiconductor rise-times, and more RF and microwave communications, at frequencies up to 80 GHz in some telecom's areas.

Parts

The evolving silicon technology of smaller transistors and its faster rise-times leads to the challenge to provide more leads in a smaller footprint, which equates to more connections per unit area.

All these trends create a demand for denser interconnects, with smaller trace and gap dimensions, smaller vias, and more buried vias. While this is not necessarily accompanied by a change in board design practices, conventional constructions can reach their limits and the design of HDI constructions require rethinking of design strategies.

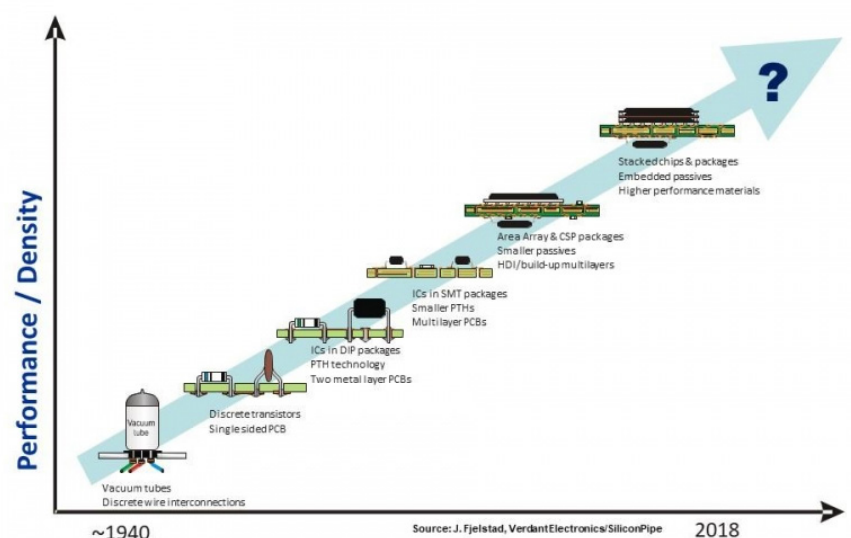


FIGURE 1. Electronics have evolved in density from the 1940s to the current state of high-density interconnects that include 3D stacking and embedded components.

HDI Multilayer Platforms

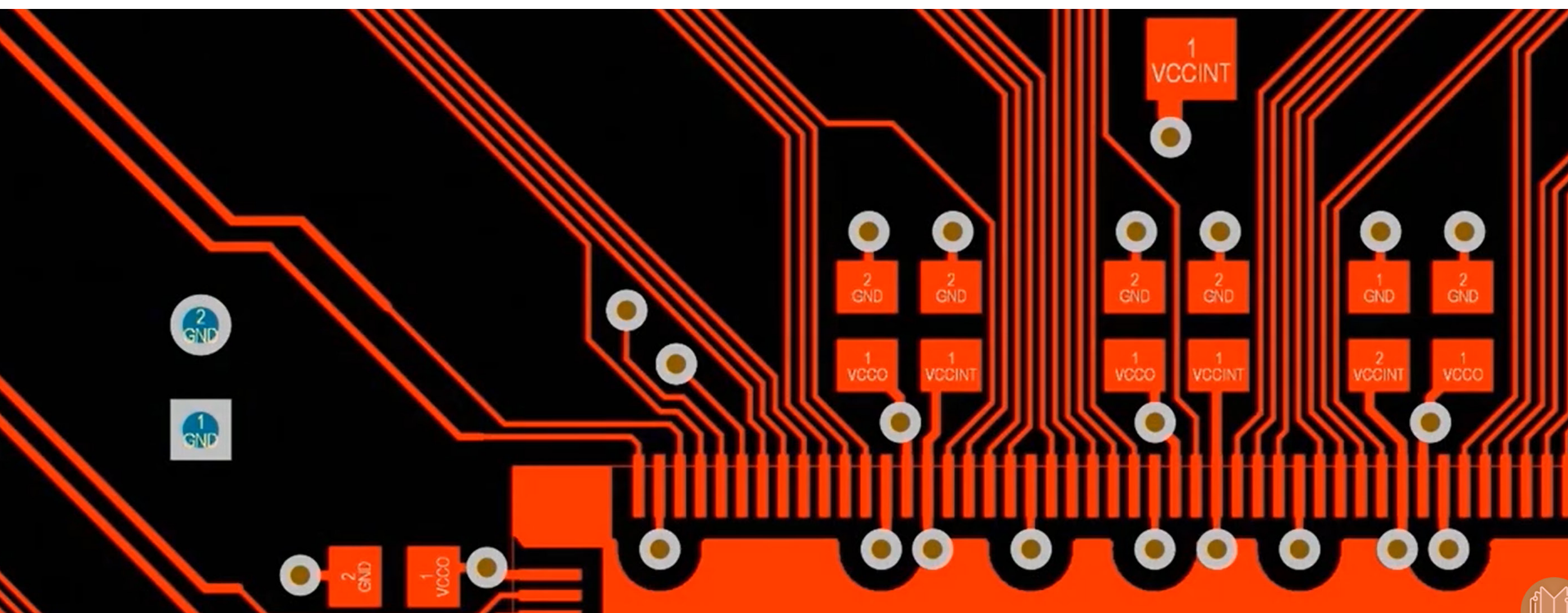
HDI is such a large and growing PWB application market, that there are at least three (3) different HDI Platforms that make it up. These four platforms are 1. Substrates & Interposers modules; 2. Portables; and 3. High performance.

Substrates & Interposers Modules

This technology is used for flip chip or wire bondable substrates. Microvias allow the increased density needed to escape from the high-density flip chips. The dielectric materials are the newer engineered films. A typical example is seen in Figure 2. The modules are small substrates that may have their ICs wire bonded, flip-chipped or TAB mounted or may use fine-pitch CSPs. The discrete components are typically very small, like 0201 or 01005s, and may even be embedded. The design rules are usually coarser than the single IC substrate, since the module may be larger than a single IC package.

Portables

Portables and miniaturized consumer products are the leading edge in HDI Technology. The dense designs offer small form factors and very dense features including micro-BGA and flip chip footprints. The largest application is currently mobile phones. A typical mobile phone product (Motorola MicroTack and the Apple iPhoneX) is seen in Figures 3.



High performance

This technology is used for high layer count boards with high I/O or small pitch components. A buried via board is not always necessary. The microvias are used to form the escape area of dense components (high I/O, micro BGA). Dielectric is reinforces-resin coated foil, reinforced prepregs and cores and high-performance laminates. A typical example is seen in Figure 4. A possible 4th platform to be developed is 'embedded components' seen in Figure 5.

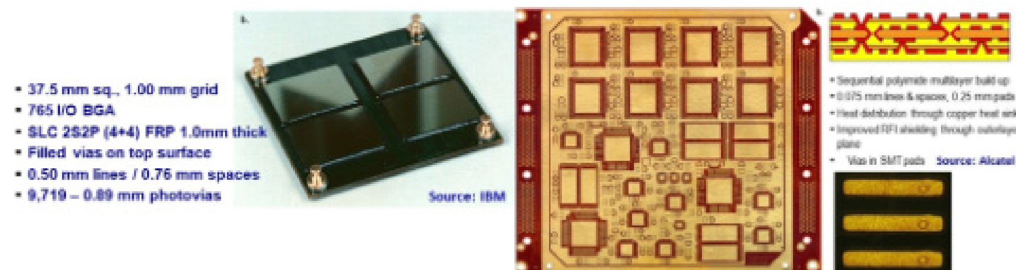


FIGURE 2. High-density modules for a. Flip chip substrates and b. Telecom

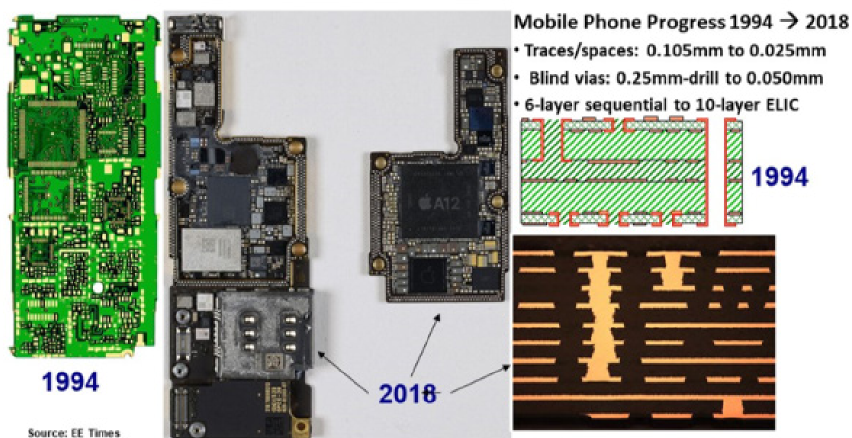


FIGURE 3. Ever increasing complexity and density characterize the HDI boards used in mobile phones from 1994 through the present day.

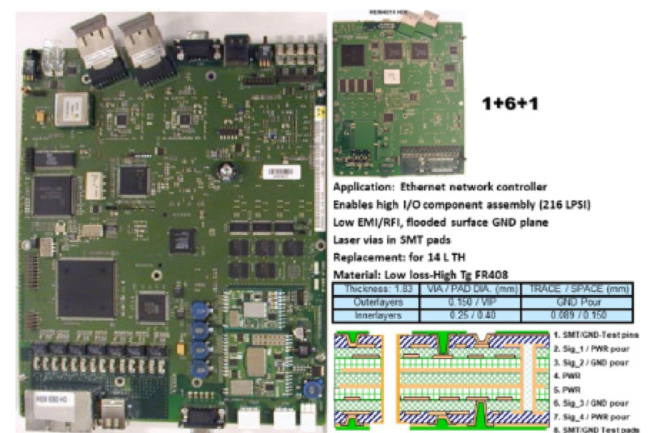


FIGURE 4. A high reliability telecom board for a triple OC-192 (10 Gb/s) optical network controller. Construction is of low-loss laminates and uses a 1+6+1 HDI structure.

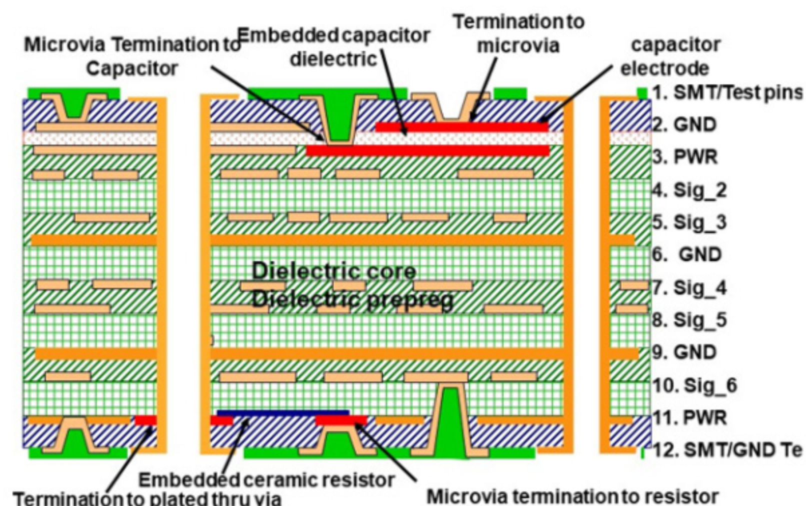


FIGURE 5. The typical usage of microvias to connect various embedded capacitors and Resistors

Performance Improvements

When performance improvements are required for PWBs, HDI is the leading contributor. In addition to making the PWB smaller, lighter, and thinner, it will have superior electrical performance. Some of these improvements are:

- Order of magnitude lower via electrical parasitic
- Minimal stubs
- Stable voltage rail
- Removal of decoupling capacitors
- Lower crosstalk and noise
- Much lower RFI / EMI
- Closer ground planes
- Opportunities for distributed capacitance (PWR/GND)
- Surface ground planes w/via-in-pads cut emissions and radiation

As semiconductor fabs reduce the size of their devices, the physics allows faster rise / fall times. This manifests itself in higher-frequency performance. But with smaller devices comes many more on a chip and higher heat dissipation. With a reduction in power supply voltage to minimize the power dissipation, what results is to increase the sensitivity of circuits to various forms of noise and loss of signal strength. High-performance laminates have always been one of the requirements. Additionally, improved processes for microvias fabrication also improve high-frequency performance.

Microvias have nearly 1/10 the parasitics of THs. Test Vehicle structures can validate the lower inductance in microvias, and when combined with low-inductance decoupling capacitors, and via-in-pads, show the merits of noise reduction, especially for high-speed logic.

Access to Advanced Components (parts)

The semiconductor industry is the primary driver for electronics. Smaller gate geometries and greater total gates allow more functions to be performed – and faster. With larger wafers, the prices continue to tumble.

IC packaging, say a 0.80- and 0.65-mm. pitch device, benefit from PCB technologies like HDI, but the use of 0.8 mm pitch and smaller devices is where HDI really begins to provide advantages. The blind vias save room on inner layers and have reduced via lands, as well as making possible via-in-pads. Typical of these devices is the 953 pins, 0.65mm pitch, Digital Signal Processor (DSP) seen in Figure 6a or the 498 pins DSP shown in Figure 6b. The other new components becoming more widespread are ones with very high pin counts of around 600 to 2500 pins, even at 1.00- and 0.8-mm pitches. Although some of these are telecom digital switches (Figure 6c), the vast majority are the new field programmable gate arrays (FPGAs). Current products from Actel, Infineon, Xilinx and Altera have packages with 456, 564, 692, 804, 860, 996, 1020, 1164, 1296, 1303, 1417, 1508, 1696 and 1764 pins. FPGAs of greater than 2000 pins are being designed!

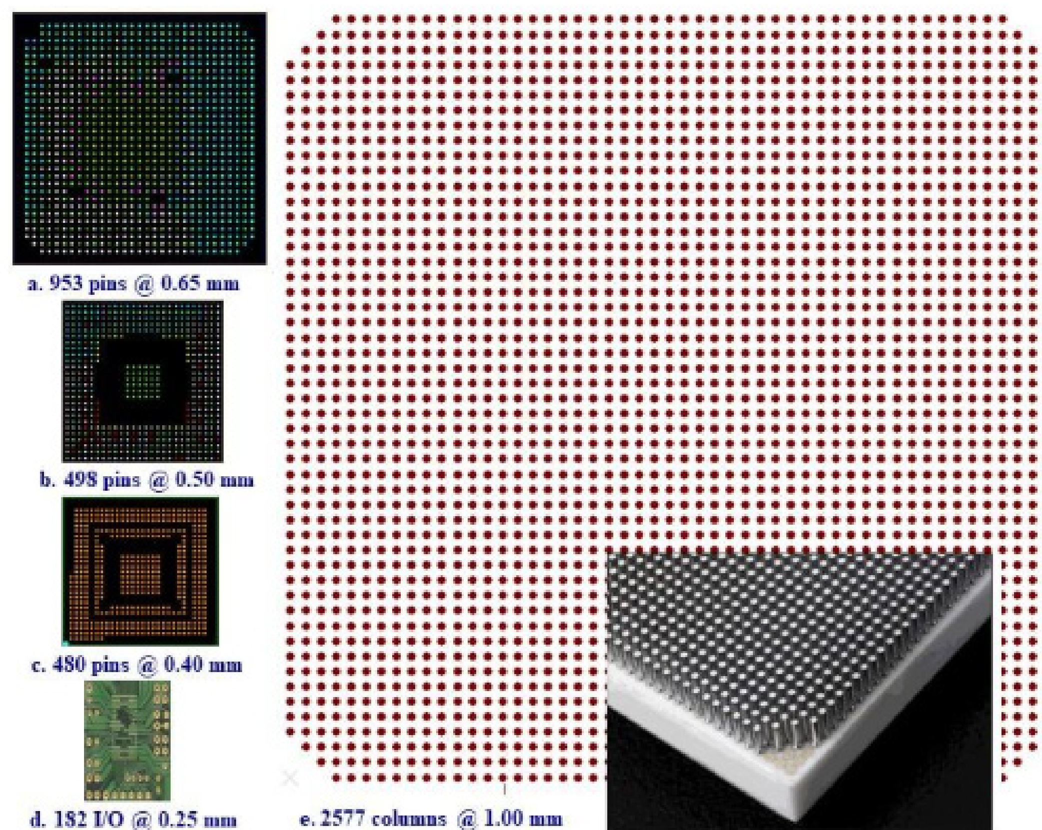


FIGURE 6. a. Fine-pitch devices such as these 953 pins - 0.65 mm pitch microprocessor, b. the 498 pin 0.5mm DSP device or c. the 480 pin @ 0.4 mm controller, even the d. 182 pins @ 0.25 mm require microvias. e. The 2577 pin - 1.0 mm pitch digital switch now require microvias in order to connect them on a printed circuit.

The HDI Opportunities

Other benefits of using HDI technologies can come from the ease of design resulting in Faster Time-to-Market and its Improved Reliability.

Faster Time-to-Market

The faster time-to-market comes about because of easier placement of components using blind vias or via-in-pads. Other design efficiencies come about because of smaller spacing, improved BGA breakouts, boulevards routing (see Chapter 4), and ease of auto-routing using blind/buried vias over through-hole vias. The overall system design times can be reduced because of the improved electrical performance of blind vias instead of TH vias, fewer respins will be required because of signal integrity and noise reduction.

Improved Reliability

Extensive reliability testing was performed by the IPC-ITRI in the late 1990s about the reliability of microvias. [1] Other groups (like HDPUG & NASA-JPL) have also produced reports on the superior reliability of small-blind vias over TH vias. [2] Understanding 'WHY' is quite simple! The via aspect ratio (AR-depth to diameter ratio) is less than (6:1 (+) that go as high as 20:1. This is a result of the thin materials and low Z-Axis TCE materials used in HDI (see Chapter 2). HDI materials are numerous and exceed multilayer laminate in variety, thus they are covered by the IPC Standard IPC-4104A and not IPC-4101B. If the blind vias are properly drilled and plated, then they will perform with many times the thermal cycle like typical THs (see Chapter 6)

The thin HDI materials are thus well suited for thermal heat transfer and this is also covered in the IPC HDI Design Standards, IPC-2226.

Lower Cost

Chapters 4 and 5 will discuss in detail, the improved design process for HDI PWBs. Properly planned and executed, an HDI multilayer can be less expensive than the TH board alternative. As illustrated in Figure 4, the Benchmark of a high-speed, controlled impedance 14-layer TH multilayer to an 8-layer HDI multilayer. By fully utilizing the Secondary Side of the PWB, 40% less area was required to connect all the components, in addition to 6 fewer layers.

Predictability or "What Will It Cost?" and the Need For Design Models

Predictability

Customers need to know the HDI stackup, design rules, and PRICE, BEFORE starting the project or board design.

Fabricators can quote the design AFTER it is designed, but without the numbers up front - no one can afford the time to run down a blind alley. The concept that "Microvias cost more!" is one of not knowing how to properly design an HDI board.

One of the benefits of Benchmarking HDI for the last 37 years, was the TH versus HDI Trade-Off chart seen in Figure 7. The Price / Density Comparison. The two key variables are RCI, a comparison currency, normalized to the actual price of an 8-layer multilayer and DEN, the average number of pins on a board divided by the length and width of the board.

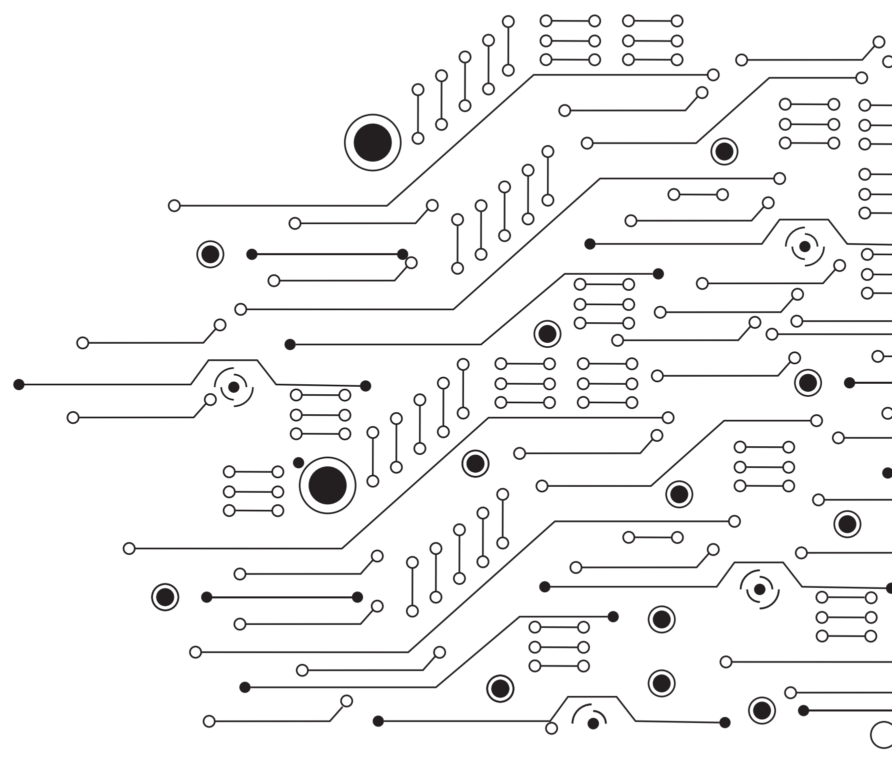
N Layers	A		B		C		D		E		F		G	
	THRU-HOLE		HDI BLIND		HDI BL/BU		1BU BLIND		2BU BLIND		2BU BL.BU		2BU BL.BU	
	N		1+N+1		1+bN+1		1+N+1		2+N+2		2+bN+2		2+bN+2	
	blind via*		L1-L2		L1-L2		skip via L1-L3		staggered L1-L2, L2-L		skip via L1-L3		staggered L1-L2, L2-L	
	buried via		none		L2-L(N-1)		L2-L(N-1)		none		L2-L(N-1)		L3-L(N-2)	
	RCI	DEN	RCI	DEN	RCI	DEN	RCI	DEN	RCI	DEN	RCI	DEN	RCI	DEN
4L	0.62	20	0.83	40	1.05	80	1.26	135	1.38	135	- -	- -	- -	- -
6L	0.78	20	0.99	60	1.24	160	1.46	200	1.60	200	1.74	260	1.91	280
8L	1.00	30	1.21	120	1.49	180	1.74	240	1.90	240	2.06	300	2.25	320
10L	1.30	40	1.51	200	1.83	210	2.11	260	2.30	260	2.50	400	2.73	440
12L	1.70	60	1.92	210	2.31	230	2.62	300	2.85	300	3.10	600	3.37	650
14L	2.24	70	2.48	220	2.95	250	3.32	360	3.61	360	3.91	800	4.25	860
16L	2.97	80	3.22	260	3.81	300	4.25	420	4.61	420	5.00	1000	5.43	1100
18L	3.92	100	4.21	300	4.95	400	5.47	480	5.93	480	6.42	1250	6.96	1350
20L	5.14	105	5.48	360	6.41	500	7.04		7.62		8.23		8.90	
22L	6.67	110	7.08	400	8.23	600	8.99		9.70		10.45		11.27	
24L	8.53	125	9.03	460	10.41	700	11.32		12.17		13.07		14.04	
26L	10.68	130	11.30	500	12.92		13.96		14.96		16.00		17.11	
28L	13.09	135	13.83	540	15.65		16.82		17.93		19.09		20.32	
30L	15.63	140	16.50	580	18.47		19.73		20.94		22.18		23.48	
32L	18.17	145	19.17	620	21.21		22.53		23.79					
34L	20.59	150	21.69	660	23.73		25.09							
36L	22.79	160	23.96	700	25.94									
38L	24.68	180	25.91	740										
40L	26.26	200												

FIGURE 7. TH versus HDI Price / Density Comparison. The Relative Cost Index (RCI) and DENsity predictor (pins/sq. inch) provides a quick comparison of TH layers (column A) to equivalent HDI structures (columns B – G).

The RCIs in the matrix is the 'Basis' numbers (or minimums) for costs. But the 'Ceiling' number for a range is out of our ability to calculate or set up at this time. It all depends on the various factors in the design. Yields are very sensitive to min. diameter, annular rings, min. trace and spacing, material thicknesses, total number of holes and their density. Other cost factors such as final finish, hole filling, and tolerances will affect the price. I have added a column for "Density" (DEN). This is the Maximum Number of Electrical Connections (called 'pins') per square inch of surface (for both sides). The dashed lines are "Equivalent" PCBs. So, as an example, an 18-Layer TH (through-hole-column A) board with an average of 100 'pins' per sq. in could have been designed as a 10-layer HDI board (1+8+1-column C) because it can handle 210 'pins' per sq. in (p/si). Or, it could have been designed as a 6-layer HDI board with 2+2+2 (column E, also 200 p/si).

The RCI does not show the "Absolute" cost savings in this example. The "Relative" cost saving is 28.1% for the 10-layer and 20.5% for the 6-layer HDI 'equivalents'. But a smaller board could result in more boards per panel and the 'PRICE" would be even lower than the above numbers. In the range of 8L to 18L, the HDI boards, especially the 2+N+2 are NOT the equivalent of 8L to 18L TH boards, they represent boards with 12X- 20X the density of TH boards.

This Matrix is based on FR-4. This has two important implications. The TH RCI scale (from 4L – 16L) represents competitive pricing set by China. This scale is depressed compared to the HDI pricing. So the HDI pricing, if equal or lower, is very competitive. If the material of construction is NOT FR-4, but a more expensive, low Dk or low Dj material, then the savings from HDI will be MUCH LARGER as you reduce layers!



11 HDI Materials You Need to Know

In this article we will discuss the materials used to manufacture HDI circuits. Several good resources exist on the subject of materials for PCBs (such as the Printed Circuit Handbook edited by Holden & Coombs) so we will concentrate on those materials that are specific to HDI.

Materials for HDI

The current HDI materials market worldwide was estimated by BPA Consulting Ltd. to be 83 million square meters. The breakdown by BPA Consulting of the eleven (11) HDI materials used, in order of usage:

- Laser-Drillable Prepregs-40.4%
- RCC-28.3%
- Conventional Prepregs-17.2%
- ABFilm-5.0%
- Epoxy-3.3%
- Other-3.2%
- BT-1.8%
- Aramid-0.4%
- Polyimide-0.3%
- Photo Dry film-0.1%
- Photo Liquid--~0.0%

The major material components of PCBs are the polymer resin (dielectric) with or without fillers, reinforcement, and metal foil. A typical construction is shown in Figure 1. To form a PCB, alternate layers of dielectric, with or without reinforcement, are stacked in between the metal foil layers.

The majority of the materials are epoxy, but some are BT, PPE, cyanate ester, and modified acrylates. The newest materials are the growing number of laser-drillable prepregs.

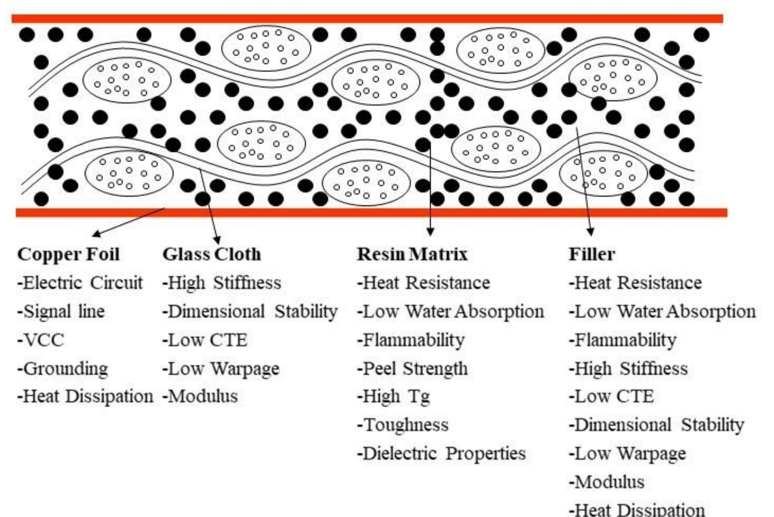


FIGURE 1. Construction of a PWB laminate [Source: PC Handbook,7th Ed]

Dielectrics and Insulators

The backbone resin of the industry has been the epoxy resin. Epoxy has been a staple due to its relatively low cost, excellent adhesion (both to the metal foils and to itself), and good thermal, mechanical, and electrical properties. As demands for better electrical performance, ability to withstand lead-free solder temperatures (see Table 1), and environmental compliance have entered the picture, the basic epoxy chemistry has been dramatically changed over the years.

Epoxies are thermosetting resins and use hardeners and catalysts to facilitate the cross-linking reactions that lead to the final cured product. Epoxies are also inherently flammable, so flame retardants are incorporated into the resin to greatly reduce the flammability. Traditionally, the main curing agent was Dicy, but now various phenolic compounds are used. The traditional bromine compounds (i.e., TBBA) used as flame retardants are being substituted with other compounds such as those containing phosphorous because of concerns about bromine getting into the environment when the PCBs are disposed of. Many companies have gone to a "Halogen-Free" requirement in anticipation of an eventual ban or for the appearance of being "green."

- **Tg – Glass Transition Temperature**
- **Td - Thermal Decomposition Temperature**
- **"Time to Delamination", T-260°C and T-288°C**
- **CTE - Coefficient Thermal Expansion Z Axis**
- **STII – Solder Temperature Impact Index**

TABLE 1. The four important thermal characteristics of a 'lead-Free' laminate and STII.

STII-Values for Some Laminate Materials

Vendor	Grade	T_g(TMA)	T_d (5%)	TE (50-260°C)	STII
ELITE	EM-827	175°C	355°C	2.6%	238
ISOLA	IS400	135°C	330°C	3.0%	202
ISOLA	FR250HR	140°C	350°C	3.4%	211
TUC	TU-662	145°C	340°C	3.4%	211
NELCO	N4000-7	150 °C	340°C	3.4%	203
TUC	TU-752	170°C	350°C	2.7%	233
NELCO	N4000-11	170°C	345°C	3.2%	225
ISOLA	IS410	170°C	350°C	3.5%	225
TUC	TU-722	172°C	330°C	3.0%	260
NANYA	NPC-175F	175 °C	361°C	3.1%	233
ISOLA	IS500	170°C	400°C	2.8%	257
TUC	TU-842	170°C	390°C	2.1%	259
NANYA	NPC-180	180°C	370°C	3.6%	240
ISOLA	370HR	170°C	350°C	2.7%	233
NELCO	N4000-12	180°C	370°C	3.6%	239
NELCO	N4000-13	200°C	365°C	3.5%	247

STII =(T_g+ T_d)/2 - [% thermal expansion 50 to 260°C] x10
Soldering Temperature Impact Index (STII ≥ 215)

FIGURE 2. Some STII values of common laminates.

Other resins that are in common use are typically selected to address specific shortcomings of epoxy-resin systems. BT-Epoxy is common for organic chip packages due to its thermal stability, while polyimide and cyanate ester resins are used for better electrical properties (lower Dk and Df) as well as improved thermal stability. Sometimes they will be blended with epoxy to keep costs down and improve mechanical properties. An important thermal property for lead-free assembly is the STII and some laminates values are seen in Figure 2.

Besides thermosetting resins, thermoplastic resins are utilized including polyimide and polytetrafluoroethylene (PTFE). Unlike the thermoplastic version of polyimide which is relatively brittle, the thermosetting version is flexible and is supplied in film form. It is typically used to make flexible circuits as well as the combination circuits called rigid-flex. It is also more expensive than epoxy and is only used as needed.

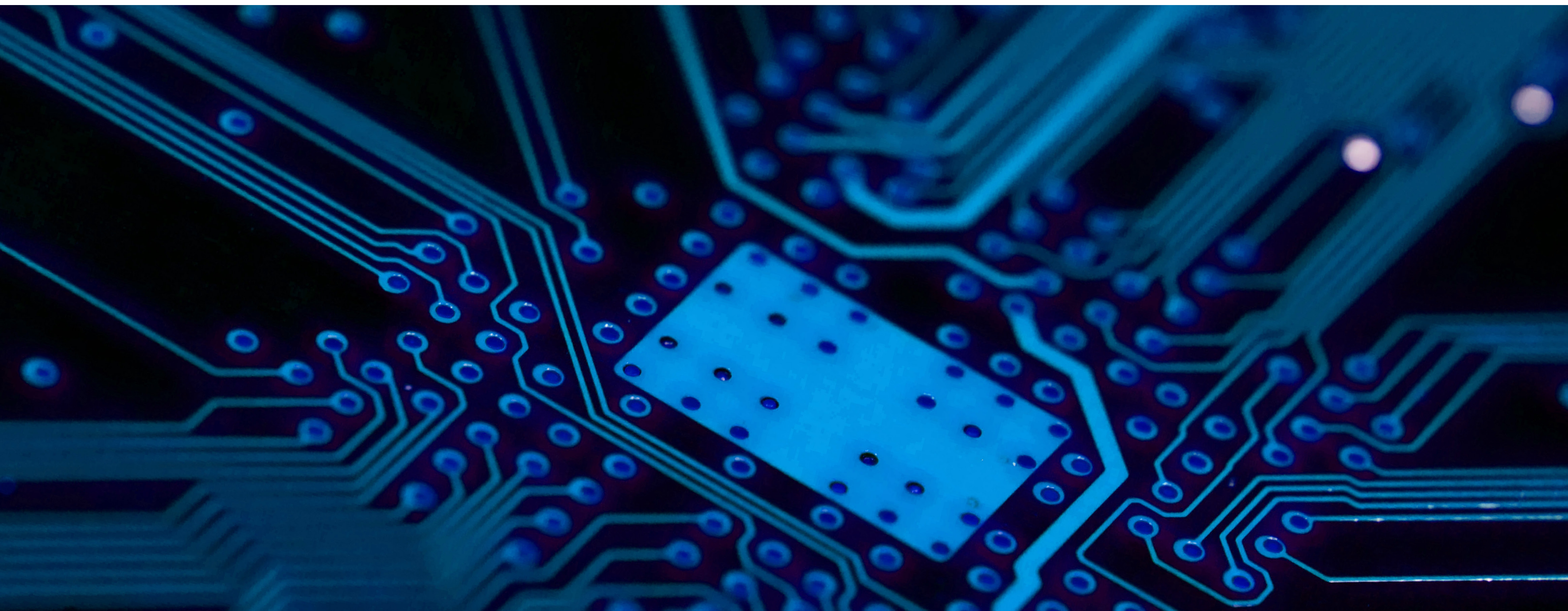
LAMINATE SUBSTITUTION CHART rev.3 (2-14-07)

TRADITIONAL LAMINATE

Tg °C		130 Epoxy	140 Epoxy	150 Epoxy	150 Phenolic-Epoxy	170 Epoxy	175 Phenolic-Epoxy	180 (CTE) Thermount	185 Phenolic-Epoxy	200 BT/ Blends	210+ Polyimide Cyante Ester PTFE	170 (lowDj) PPO-Epoxy PPE-Epoxy	155 RCC Epoxy
ISOLA	N. America/Europe	CM310TM:130	FR402:140 ED130OU:135 IS400:135 IS402:140	FR404:150 Duraver® 155		FR406:170	IS420:170	Duramid:180	IS410:180 IS415:190	G200:185 GI-180	IS620:215 P95: 260 P96:260	FR 408:180	ECOFoil:150 ISOFoil160:160
NELCO			N4000-2:130		N4000-7:155	N4000-6:175		N4000-13T:210 Thermount:180	N4000-11:175 N4000-12:190	N5000:185 N5000-32:205	N7000-1:260 N8000-13:230 N9000:315	N4000-13:185 N6000:200	
POLYCLAD			PCL-FR-226:140 PCL-FR-240:140	PCL-FR-254:150 PCL-FR-250:150 PCL-HP-541:145		PCL-370 TURBO:175	PCL-HF-571:165 PCL-400:170		PCL-FR370:175 PCL-FR-370HR: 180	PCL-GI-180:200 PCL-PCC:200	PCL-GI-785:260 PCL-GI-787:260 PCL-GI-789:260 PCI-GI-702LF:230	PCL-LD-621:210 GETEK HR:175	PCL-400:170 PCL-RCC:200
ARLON								Thermount 180					
GORE											Speedboard C:220	G620:155	
MITSUBISHI	Japan									HL832/830:180			
PANASONIC			R1766:140		R-1755C_R-1650C	R-1766:170 R-1767	R-1755S_R-1650S		R-1755_R-1650 R-1755T_R-1650T	Megtran 3:200 Megtran 3-ES:200	R4775:220	Megtron6:190 Megtron +:195	R-0880:170 R-1661E
HITACHI		MCL-E-67:125			EM-280	MCF-6000G:170			E-679:183	MCF-6000E:190 E679:170	MCL-LX67F:215	MCL-E-65:155 MCL-LX-67:185	MCF-6000E:190 MCF-9000E:135
NANYA CCL	Taiwan	FR4-86	NP-140 NP-140M	NP-150	**NP-155F**	**NP-170**	**NP-175** **NP-175F**		NP-180(F)	NP-200		NPLD-II	NP-RCC
TUC			TU-622	TU-622-5	TU-722-7				TU-742	TU-822		TU-732	
LEADER		LS-4Y											
ITEQ			IT140	IT150				IT1556	IT180				
ELITE MAT'L			EM-220	EM-220(5) EM-826(5)	EM-320(5) EM-826(5)	**EM-320**	**EM-827**					EM-340	
KINGBOARD	China	KB-6150 KB-6160	KB-6164			KB-6167							
GRACE						GA170							
HOLLEY HILAND			FR4-74 FR4-TC										
ShingYi		S1130	S1141		S1000	S1170	S1000-2		S1180		S1860	S1139:145	S6018
LG	Korea	LG-E-451:130				LG-E-451H:175		LG-E-451HT:180		LG-E-410L:195		LG-E-200LL:195	
DOOSAN		DS-7405:130	DS-7408:140			DS-7409:170						DS-7409D	DSF-400:140 DSF-500:170

FIGURE 3. Laminate substitution chart for many PWB laminates

To aid in your selection of the proper laminate for HDI, Figure 3 shows a selection of laminates from around the world and their equivalency.



Reinforced Materials
Laser-Drillable and Conventional Fiberglass

Most of the dielectric materials that are used to make printed circuit boards incorporate reinforcement into the resin system. Reinforcement usually takes the form of woven fiberglass. Woven fiberglass is just like any other cloth, made up of individual filaments that are woven together on a loom. By using different diameter filaments and different weave patterns, different styles of glass cloth are created.

Fiberglass adds both mechanical and thermal durability to the dielectric, but it does present some problems when used in HDI constructions. Figure 5 shows that glass fabric is woven, and the table shows the styles, yarns, and thicknesses of those yarns. When lasers are used to create the vias, the difference in ablation rates between the fiberglass and the surrounding resin can cause poor hole quality. Also, since the fiberglass cloth is not uniform due to having areas with no glass, areas with one strand, and the intersections of strands (also known as knuckles), it is difficult to set up drilling parameters for all these regions. Usually the drilling is set up for the hardest to drill region which is the knuckle area.

The fiberglass manufacturers have created so-called laser-drillable dielectrics by spreading the yarns in both directions and making the fabric more uniform which minimizes the areas with no fiberglass as well as the knuckle area. Figure 4 shows the 12 currently available LDPs and their properties. It still takes more energy to penetrate the fiberglass than the resin, but now the drilling parameters can be optimized to get consistent results throughout the panel.

Cloth Style	Warp x Fill	Glass Cloth Thickness (mm)		Air Permeability (M3/M2min)		Warp & Fill Yarn Width (mm)			
						Standard		LDP	
		Standard	LDP	Standard	LDP	Warp	Fill	Warp	Fill
1015	75 X 75	- -	0.020	- -	23-45	- -	- -	0.163	0.270
1027	75 X 75	- -	0.020	- -	22-42	- -	- -	0.163	0.270
1037	71 X 74	- -	0.025	- -	20-40	- -	- -	0.210	0.270
106	56 x 56	0.037	0.028	120-140	20-40	0.138	0.254	0.163	0.385
1067	70 x 70	- -	0.033	- -	9-14	- -	- -	0.215	0.351
1078	54 x 54	- -	0.044	- -	9-14	- -	- -	0.255	0.419
1080	60 x 48	0.055	0.045	85-105	20-40	0.213	0.296	0.283	0.413
1086	60 x 61	- -	0.047	- -	6-10	- -	- -	0.285	0.398
2112	40 x 40	0.071	0.069	60-75	5-20	0.318	0.439	0.356	0.537
2113	60 x 56	0.070	0.065	32-50	4-12	0.302	0.319	0.329	0.452
2313	60 x 64	0.072	0.067	17-30	3-8	0.308	0.311	0.313	0.403
2116	60 x 58	0.092	0.088	8-18	5-10	0.360	0.365	0.365	0.395

FIGURE 4. Table of cloth specifications for laser-drillable fiberglass.

RCCs
Resin Coated Copper (RCC) Foil

The limitations of fiberglass-reinforced dielectrics prompted companies to look at alternative dielectric solutions. In addition to the problems with laser drilling (poor hole quality and long drilling times), the thickness of woven fiberglass limited how thin the PCBs could be. To overcome these issues the copper foil was utilized as a carrier for the dielectric so it could then be incorporated into the PCB. These materials are called “Resin Coated Copper’ or RCC. RCC foil is manufactured using a roll to roll process.

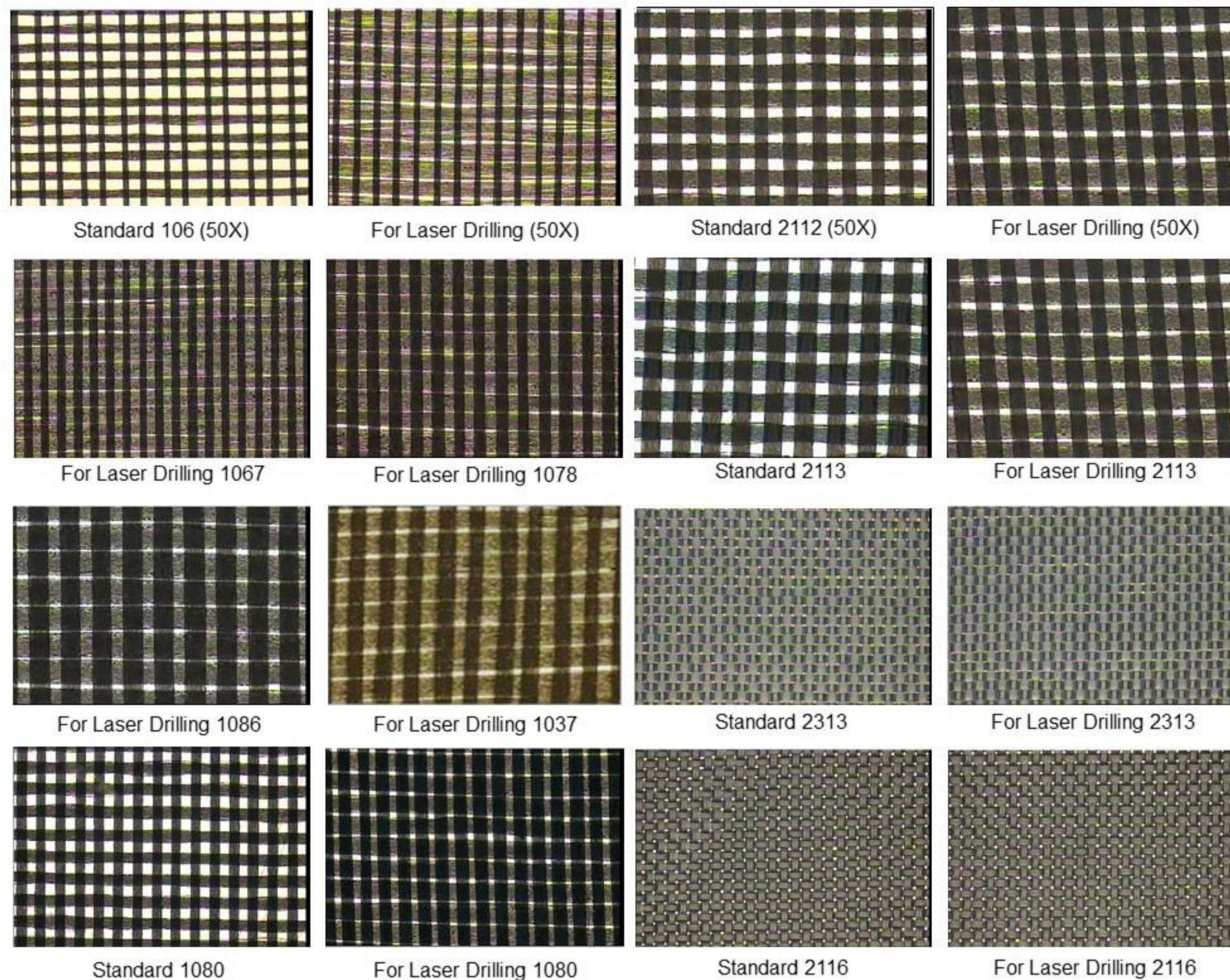


FIGURE 5. Photos of standard and laser-drillable fiberglass cloths.

The copper goes through a coating head and the resin is deposited on the treated side of the copper. It then goes through drying ovens and is partially cured or “B” staged which will allow it to flow and fill in the areas around the internal circuitry and bond to the core. The resin systems are usually modified with a flow restrictor to prevent excessive squeeze-out during the lamination process.

Most of the RCC foil is manufactured this way, but additional types exist. One of these types is a two-stage product (Figure 6). After the first resin layer is coated, it is put through the coater again to add a second layer. During the second coating the first layer is fully cured, while the second layer is "B" staged. The benefit of this process is that the first stage acts like a hard stop and guarantees a minimum thickness between layers. The disadvantage is that the product is more expensive than the single coated version.

For all the benefits of RCC foil, there are concerns over the lack of reinforcement in terms of dimensional stability and thickness control. A new material was developed to address these concerns. MHCG from Mitsui Mining and Smelting incorporates an ultra-thin fiberglass (either 1015 or 1027) during the resin-coating process. The fiberglass is so thin that it cannot be made into a prepreg since it cannot go through a treater tower like traditional fiberglass. There is also a polyimide / epoxy RCC available.

The fiberglass does not impact laser drilling significantly, yet it provides dimensional stability equal to or better than standard prepreg. Dielectric layers as thin as 25 microns are now available allowing for very thin multilayer products.

Cost is another aspect of RCC foil that is of concern. RCC foils almost always cost more than the equivalent prepreg/copper foil combination. However, the RCC foil can actually result in a less expensive product when laser-drilling time is taken into consideration. As the number of holes and size of the area increase, the improved throughput of the laser drills more than offsets the increased cost of the RCC foil.

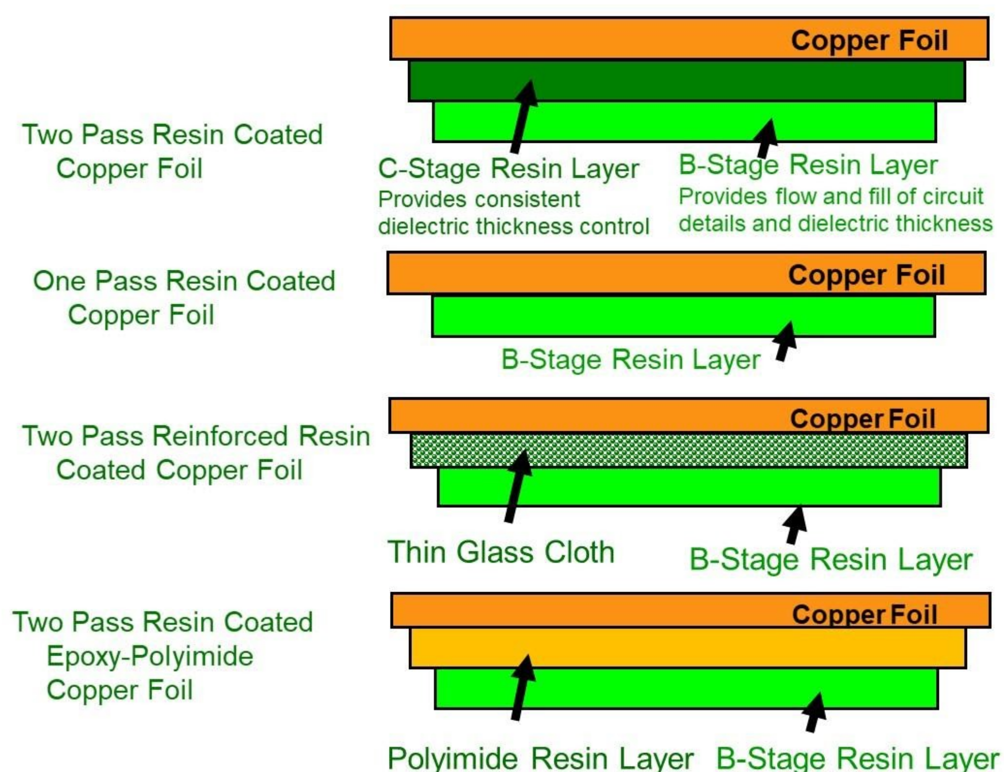


FIGURE 6. Four available styles of resin coated copper (foil).

Other Dielectrics

Optimized liquid epoxy can provide the lowest cost of any of the dielectrics for HDI. It is also the easiest to apply in thin layers for fine-line wiring. It can be coated by screen printing, vertical or horizontal roller-coating, meniscus coating, or curtain-coating. The Taiyo Ink brand is the most used but Tamura, Tokyo Ohka Kogyo, and Asahi Denka Kogyo also have products.

Polyphenyl Ethers/Polyphenylene Oxide: M.P > 288° C are thermoplastics of Polyphenyl Ethers (PPE) or Polyphenylene Oxide (PPO) with melting points well over 288°-316° C. PPO/Epoxy blends have a Tg >180° C with higher decomposition temperatures. Their popularity is their excellent electrical performance due to having lower dielectric constants and loss tangents than many of the thermosets like epoxy and BT with low water absorption. Their high melting points and chemical resistance make desmearing a critical process.

Electrical Properties

Figure 7 displays the dielectric constants (Dk) and dissipation factors (Dj) of popular dielectrics, including those suitable for very high-speed logic. Table 2 lists other electrical characteristics related to high-speed performance for HDI design.

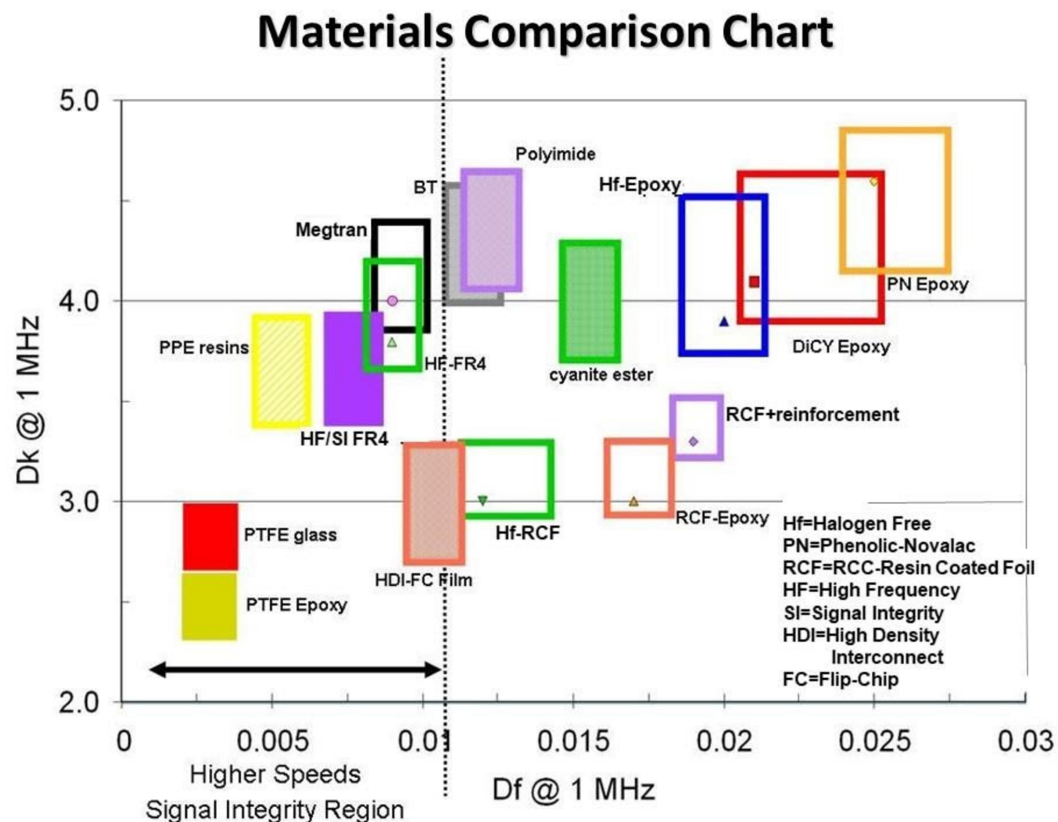


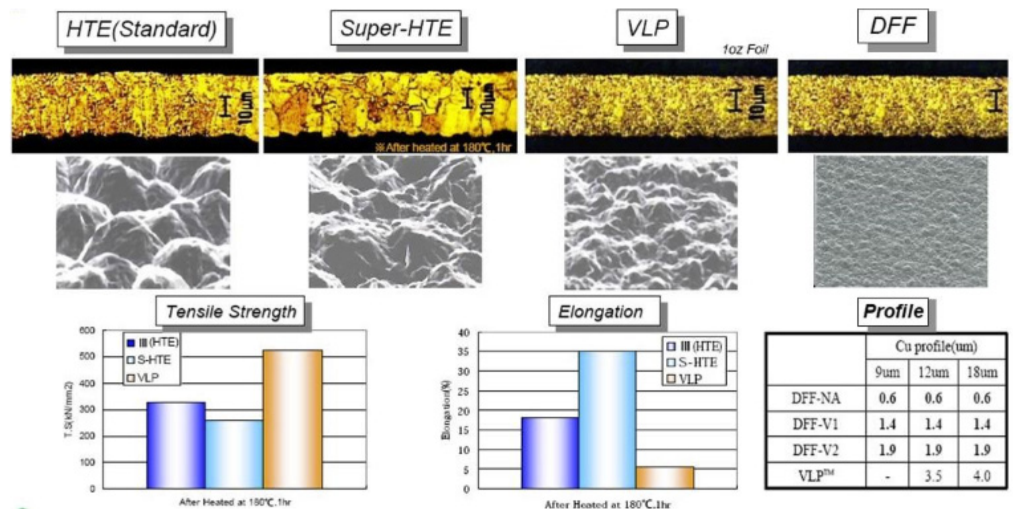
FIGURE 7. The electrical characteristics of various laminates by their dielectric constant and dissipation factor.

- **Signal Attenuation-losses**
- **Propagation velocity - delay**
- **Controlled Impedance Structures**
- **Capacitance & Inductance Loading**
- **Crosstalk**
- **Spatial distortions**
- **PWB Power Distribution-Stackups**

TABLE 2. Other important electrical performance considerations when designing high-speed circuits.

Enabling Fine Traces and Spaces

For very high-speed logic, the signals travel on the surface of the conductor (the Skin Effect). Smooth copper foils enable the fabrication of very fine traces and spaces with less copper losses. (See Figure 8) in Figure 9, ultra-fine traces are capable with the 5 micron and 3 micron copper foils, or with a mSAP process.



	Cu profile(um)		
	9um	12um	18um
DFF-NA	0.6	0.6	0.6
DFF-V1	1.4	1.4	1.4
DFF-V2	1.9	1.9	1.9
VLP™	-	3.5	4.0

FIGURE 8. Foil treatment for adhesion comes in four profiles and is important for copper losses (skin effect).

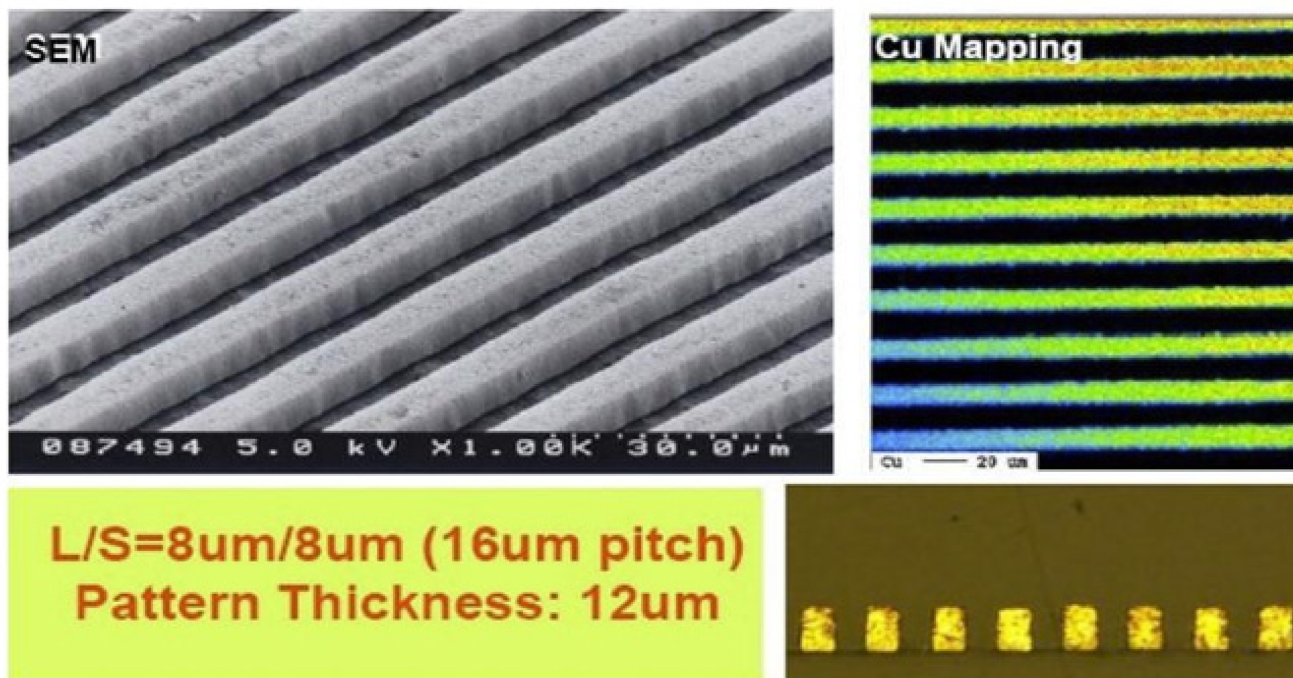


FIGURE 9. Very thin and smooth copper foil can permit very fine traces and spaces (8um/8um).

Materials for High Density Interconnects is a serious subject for PCB designers and Electrical Engineers. Several good resources exist on the subject of materials for PCBs and the focus here has been HDI Materials to help the engineer design printed circuit boards.

HDI Quality and Acceptability Requirements

The very nature of microvias' small size makes the acceptability criteria difficult to define. Most HDI Quality and Acceptability requirements are still OEM defined. The IPC has IPC-6016 as part of the IPC-6012, the generic QUALIFICATION AND PERFORMANCE SPECIFICATIONS (6010 SERIES). These specifications only cover the build-up HDI layers and not the core, which is covered by their own IPC specifications.

IPC-6016 Qualification and Performance Specification for High Density Interconnect (HDI) Structures

IPC-6016: This document contains the general specifications for high-density substrates not already covered by other IPC documents, like IPC-6011, the generic PWB qualification and performance specifications. The acceptance criteria of HDI layers are organized into slash sheet categories of:

A. Chip Carrier

B. Hand Held

C. High Performance

D. Harsh Environment

E. Portable

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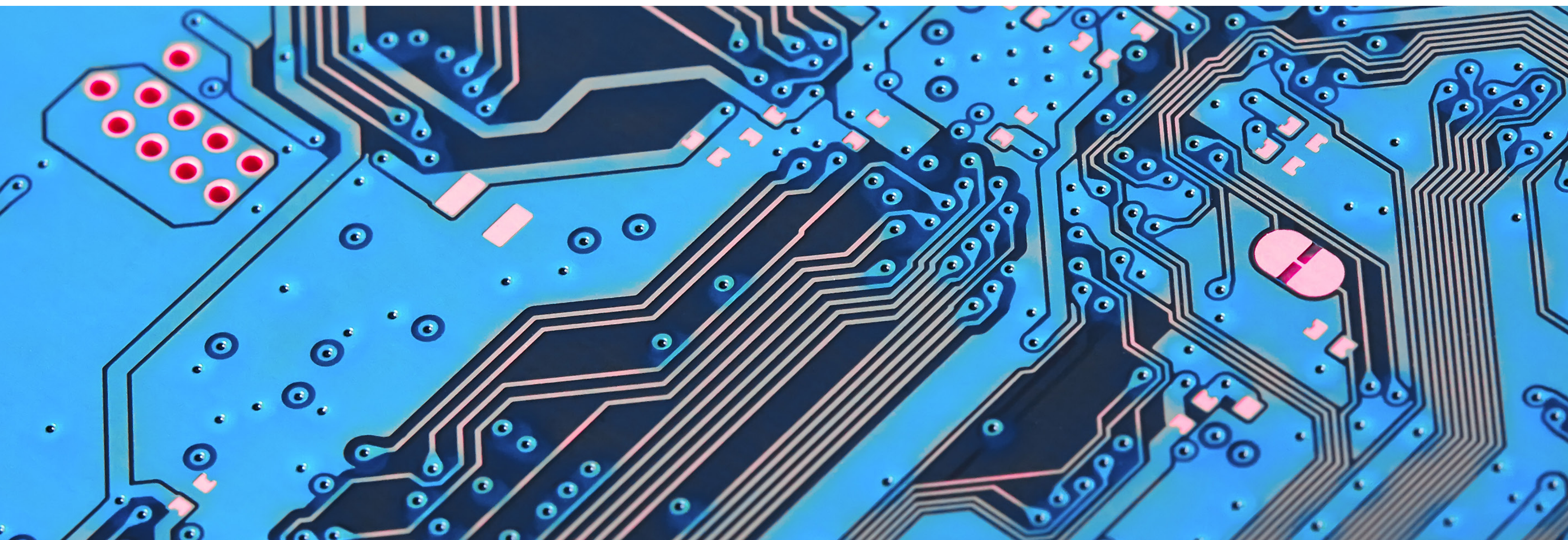
The acceptability requirements are broken down into these 12 specific specifications:

- Section 3.1: General
- Section 3.2: Materials
- Section 3.3: Visual Examination
- Section 3.4: Dimensional Requirements
- Section 3.5: Conductor Definition
- Section 3.6: Structural Integrity
- Section 3.7: Other Tests
- Section 3.8: Solder Mask
- Section 3.9: Electrical Properties
- Section 3.10: Environmental Requirements
- Section 3.11: Special Requirements
- Section 3.12: Repair



Quality- Control

Microvias are nearly impossible to inspect visually and extremely difficult to cross-section. This necessitates a more indirect approach to verification of proper fabrication. Proper microvias, as seen in Figure 1 a-d, can be distinguished from defective microvias, as seen in Figure 2a-d. It is easiest to cross-section these vias when they are employed in a "test coupon" such as the IPC's PCQRR program. These coupons are the same as used in IPC-9151 and correlate to a statistically measured via-chain resistance and accelerated thermal-cycling tests (HATS). [1] The criteria for quality microvia production are no more than 50 defective microvias per million microvias and a covariance of the standard deviations of the daisy chain Kelvin resistances coupons of 5%.

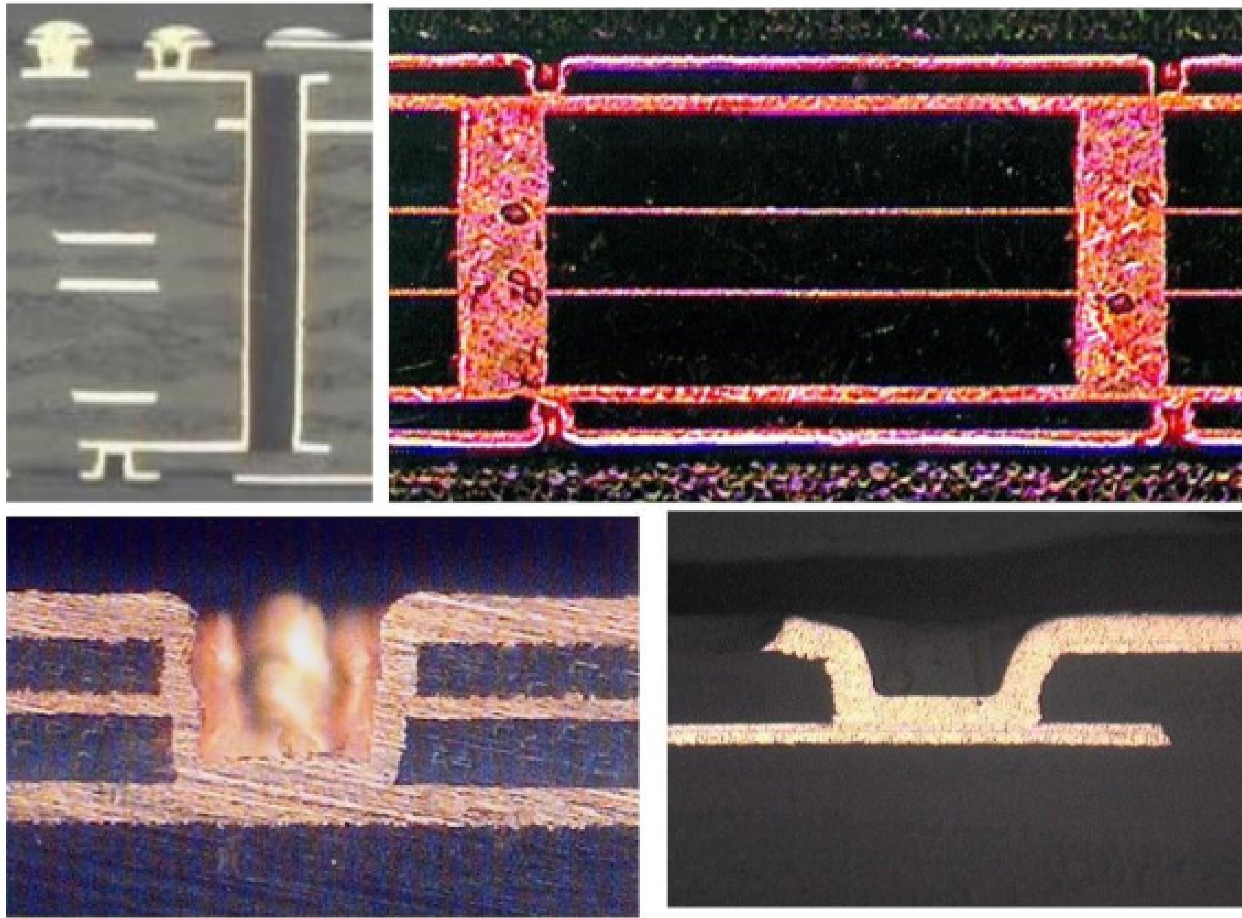


FIGURE 1. Example of well fabricated blind and buried vias; a. 8-Layer blind-buried vias; b. 6-Layer blind-buried vias; c. Skip blind via from L-1 to L-2 & L-3; d. Proper blind via filled with solder-mask.

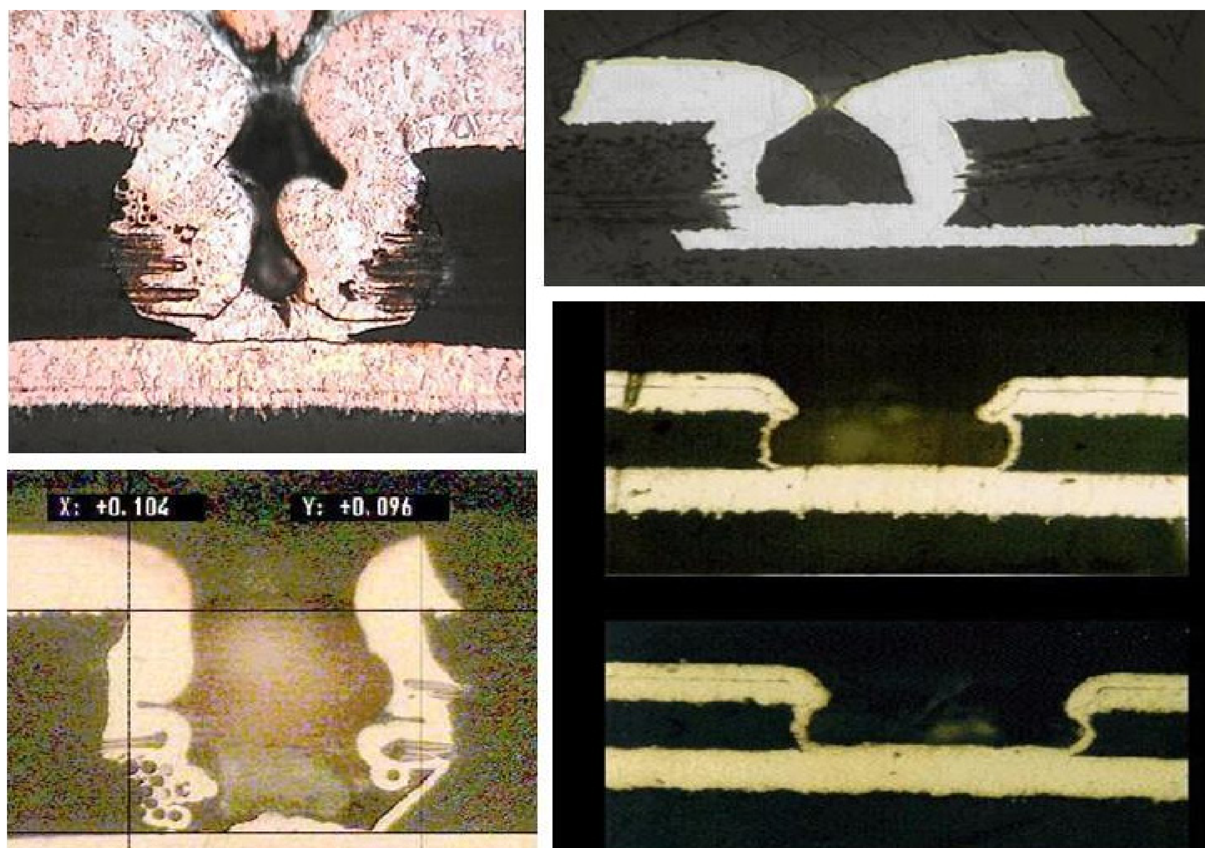


FIGURE 2. Improperly formed blind vias that should be rejected.

Laser Drilling Quality

The quality of laser drilling of microvias illustrates the nature of the failure modes in microvias. Figure 3 shows the seven main quality criteria for laser microvias, along with the quality criteria spec, measurement methods, sample size and control limit.

Item	Spec	Measurement	Sample Size	Control limit
1. Overhead	Class A: a / b ≥ 0.95 Class B: a / b ≥0.90,a/b<0.95 Class C: a / b <0.90	Cross section inspected by microscope	1. first piece of Per Part 2. one of per 10 lots.	a / b = 0 a / b ≤ 0.9
2. Roughness	Class A: R < 0.1 mil Class B: R ≥ 0.1, P ≤ 0.5 mil Class C: R > 0.5 mil	Cross section inspected by microscope	1. first piece of Per Part 2. one of per 10 lots.	R = 0 R ≤ 0.5 mil
3. Taper angle	Class A: 5° Class B: 10° Class C: 15°	1. Cross section inspected by microscope 2. Z-check	1. first piece of Per Part 2. one of per 10 lots.	θ = 0° θ ≤ 20°
4. Voids	Class A: No Voids Class B: Voids	Cross section inspected by microscope	1. first piece of Per Part 2. one of per 10 lots.	No Voids
5. Wicking	Class A: L ≥0, L ≤0.1 mil Class B: L > 0.1, L ≤0.5 mil Class C: L > 0.5 mil	Cross section inspected by microscope	1. first piece of Per Part 2. one of per 10 lots.	L = 0 L ≤ 0.5 mil
6. Resin remains	Class A: t ≥0, τ ≤0.2 mil Class B: > 0.2, t ≤0.5 mil Class C: t > 0.5 mil	Cross section inspected by microscope	1. first piece of Per Part 2. one of per 10 lots.	t = 0 t ≤ 0.5 mil
7. Cracks	Class A: No Cracks Class B: Cracks	Cross section inspected by microscope	1. first piece of Per Part 2. one of per 10 lots.	No Cracks

FIGURE 3. The seven main quality criteria for laser drilled microvias

Vendor Qualification

Selecting an HDI fabricator can be very challenging. One way to discover the HDI capabilities of PCB fabricators is the new IPC-9151 Capabilities Benchmarking Panel. This standardized multilayer panel can be seen in Figure 4. It is provided in 2, 4, 6, 10, 12, 18, 24 and 36 layer structures with high and low density design rules, 5 thicknesses (for PCB and backplanes), and in a large panel size of 18” x 24” with various traces and spaces and via structures of blind and buried. The IPC Committee is planning other new Benchmarking Panels for substrates.

The blind vias are optional, but provide significant data on the fabricator’s HDI capabilities. Details, artwork, and a sample report are available on the IPC 9151 Website.

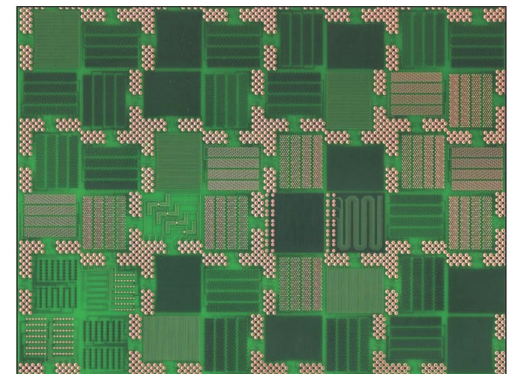


FIGURE 4. A typical PCQR2 panel from the IPC Program

Other options include fabricating production boards and having them tested. Although this method is convenient, most times this results in statistically non-significant results, that is; too few samples are evaluated to provide for statistical significance interpretation. The performance measured could be the result of hand-selecting the samples and not being statistically accurate in covering a range of capabilities.

Test Vehicles many times are used for qualification and this can be very accurate. This is also the way reliability can be established. Later sections will discuss test vehicles and reliability testing results

Qualification Coupons

The best tools I know for doing this are the many parametric analysis and characterization coupons available to you. These are part of the quality assessment process. These processes cover reliability evaluations, end-product evaluation, work-in-process product evaluations, and process parameter evaluations. Here are five coupon systems, four seen in Figure 5:

- IPC-2221 Appendix A, D-Coupon
- Conductor Analysis Technology (CAT™)
- Printed Circuit Quality and Relative Reliability (PCQR2) (Figure 4)
- Highly Accelerated Thermal shock (HATS™)
- Interconnect Stress Test IST™)

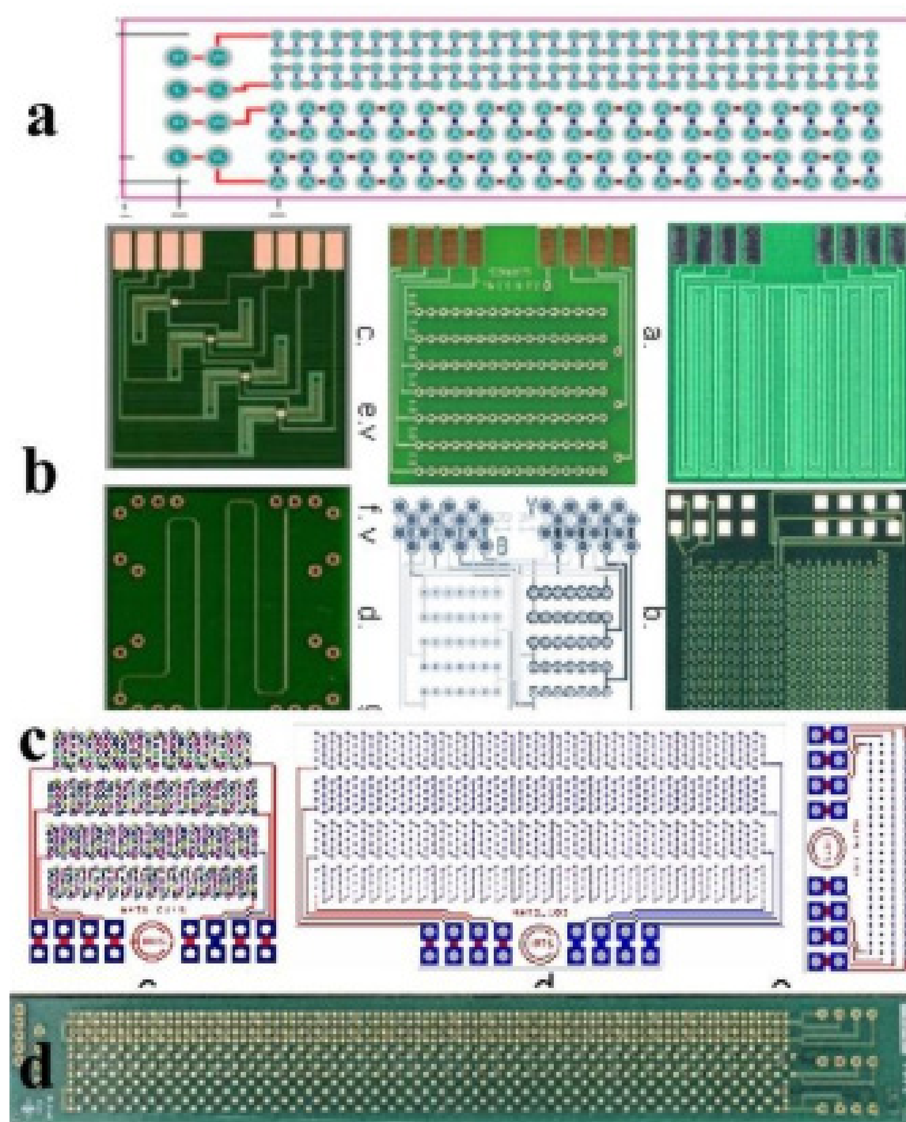


FIGURE 5. Four of the five qualification test coupons systems; a. IPC D-Coupon; b. CAT's coupons for panels; c. CAT's various HATS test coupons; d. Interconnect Stress Test (IST) coupon.

Accelerated Reliability Test Coupons

Three coupon methods are typically used in reliability test vehicles:

- Accelerated Thermal Cycling (ATC)
- Highly Accelerated Thermal Shock (HATS)
- Interconnect Stress Test (IST)

Thermal Cycling Testing

Accelerated reliability testing using test coupons is about as old as PCBs are. The principle is to crowd a large number of holes into a small space and connect them in a chain, hence the name ‘daisy-chain’. The test board pictured in Figure 6 is typical of an HDI daisy-chain test vehicle. This board contains a number of different test structures for various test criteria. Most of the space is taken up by the HDI blind-via daisy-chains (BLOCK A, B, C, E, and F) and the TH daisy-chain (BLOCK D). The Table 1 shows a summary of the test blocks and their criteria for qualification. Figure 7 is typical for the qualification of higher volume technology-intensive products like notebook computers and networking cards.

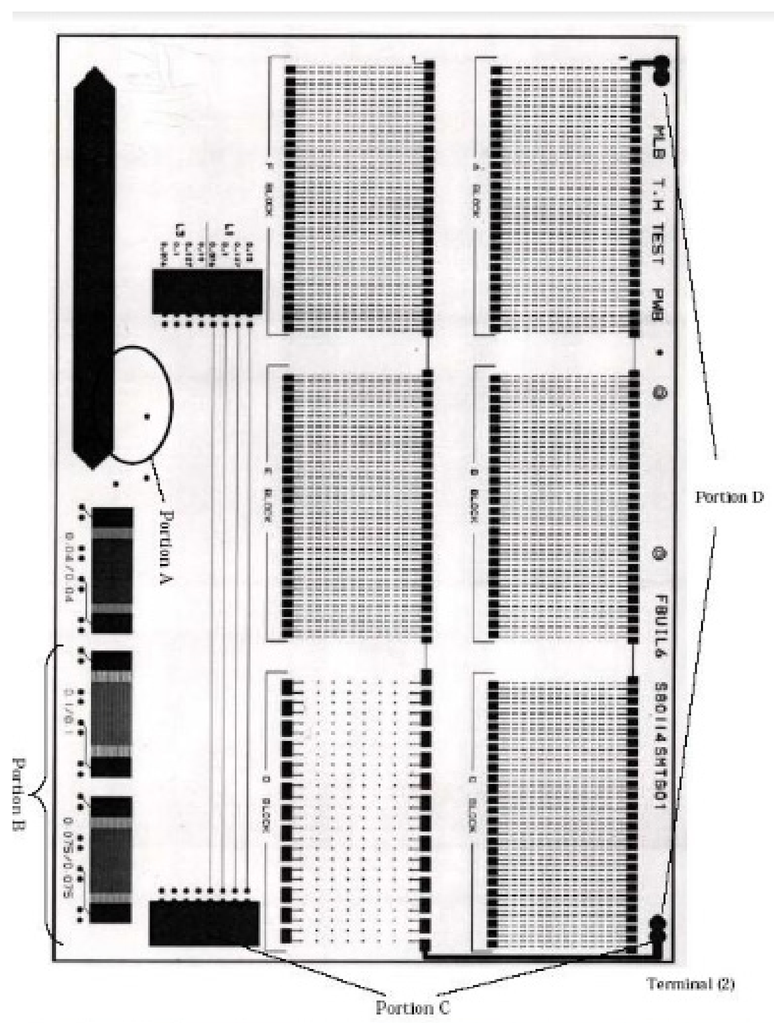


FIGURE 6. Typical HDI Qualification/Reliability test vehicle.

Many coupon systems are used for reliability testing. These are incorporated into test vehicles that are then fabricated and subjected to various conditioning and stresses, and then evaluated for performance. The IPC has provided a new generation of test coupons, the “D-Coupons” from Appendix A in the IPC-2221 standard. The testing criteria for the 4-wire Kelvin resistance test is provided in IPC-TM-650, Method 2.6.27A. The thermal shock is per IPC-TM-650, Method 2.6.7.2.

These test are carried after the coupons are passed through a SMT convection reflow assembly oven for a minimum of 6 times using one of two different reflow profiles (230OC or 260OC) without any measured high resistances or opens detected.

Conditions	***Industry Requirement***	***Laser Drilling***
1. Liquid-Liquid Shock: - 55^{0}C to 125^{0}C, cycle time of 5 min., ***2000 cycles***, Change of resistance <10 %	Motorola: 500 cycles	no failures
2. High Temperature: 125^{0}C, for 1000 hrs,	Bellcore: 500 hrs	Passed
3. Adhesion Test - Copper Peel Strength	IPC: 5 lbs/inch	Passed Min. 5.5 lbs Max: 12.2 lbs
4. Dielectric Withstanding Voltage (0 to 5000 VDC applied, rate of 100volts/sec	IPC:500V/mil Bellcore: 1000 volts for 1 min	Passed >1500 V/mil
5. Min. Copper Thickness in Micro Via (mils)	Bellcore: Min. 0.7 mil	Passed 0.95
6. Dielectric Thickness (Micro via) mils	Bellcore: ≥ 2.00 mil	≥ 1.8
7. Temp./Humidity: 85^{0}C, 85%RH, 100 V Bias, 1000 hrs	Bellcore: 500 hrs	Passed

TABLE 1. Test criteria for HDI test vehicle.

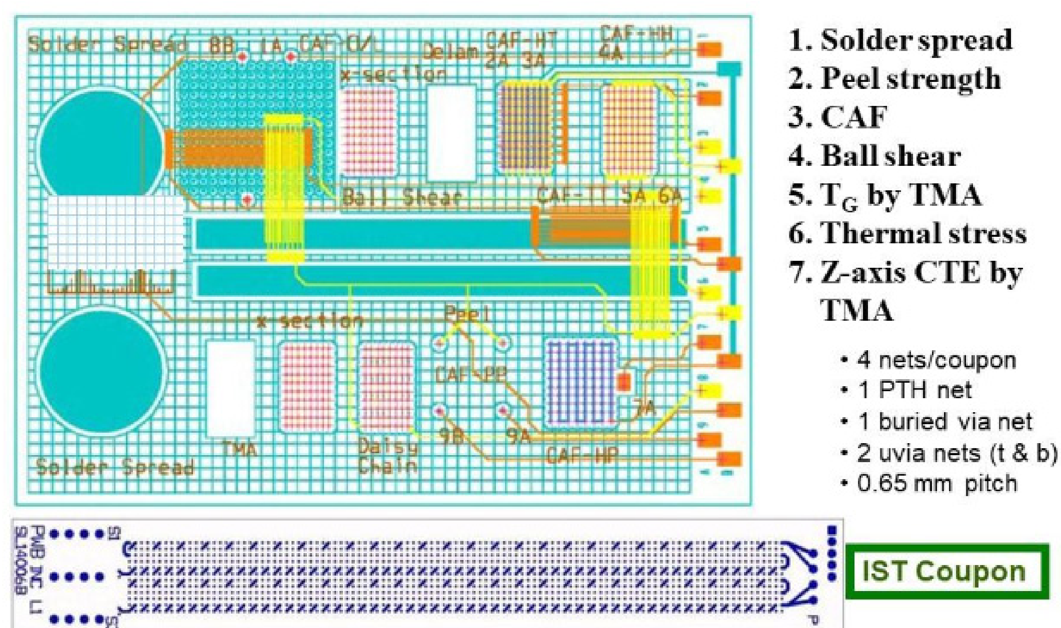


FIGURE 7. Typical industry test vehicle for higher reliability computer and telecom products.

ABOUT ALTIUM

Altium LLC (ASX: ALU) is a multinational software corporation headquartered in San Diego, California, that focuses on electronics design systems for 3D PCB design and embedded system development. Altium products are found everywhere from world leading electronic design teams to the grassroots electronic design community.

With a unique range of technologies Altium helps organisations and design communities to innovate, collaborate and create connected products while remaining on-time and on-budget. Products provided are Altium Designer®, Altium Vault®, CircuitStudio®, PCBWorks®, CircuitMaker®, Octopart®, Ciiva® and the TASKING® range of embedded software compilers.

Founded in 1985, Altium has offices worldwide, with US locations in San Diego, Boston and New York City, European locations in Karlsruhe, Amersfoort, Kiev and Zug and Asia-Pacific locations in Shanghai, Tokyo and Sydney. For more information, visit www.altium.com. You can also follow and engage with Altium via Facebook, Twitter and YouTube.