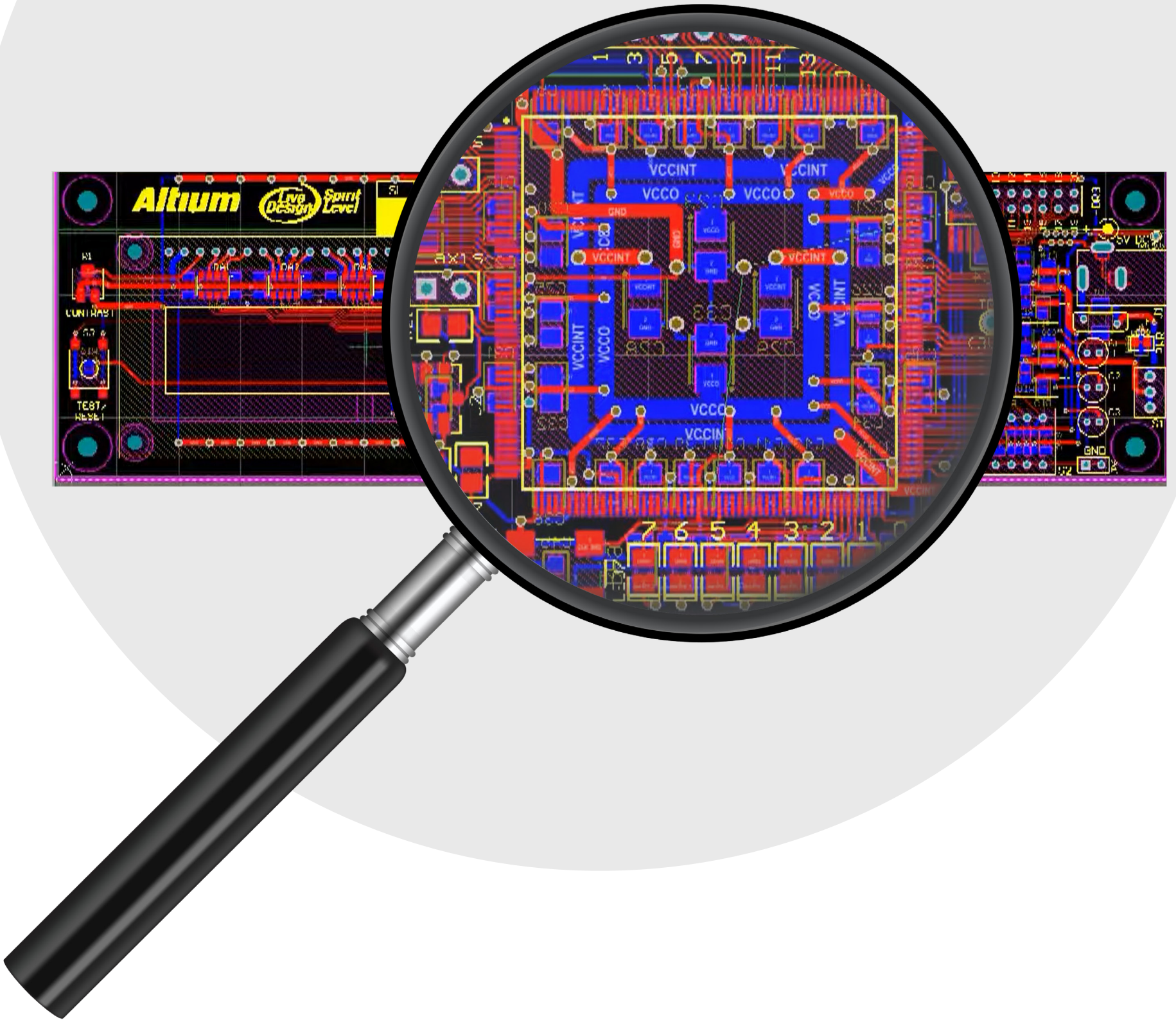


Routing High-Density Interconnects with Reliable Microvias

Reliability in an HDI PCB Layout

Altium®

Table of Contents

Altium®

The IPC Warning About Microvia Reliability for High Performance Products

Hopefully, by now, you have read the full Press Release from the IPC on March 6, 2019, about the warning of field and latent failures of high-profile HDI boards. IF not, the complete press release is available on I-Connect 007. [1]

What you may have seen is the warning statement which the IPC will be including in the upcoming IPC-6012E, ***Qualification and Performance Specification for Rigid Printed Boards:***

"There have been many examples of post-fabrication microvia failures over the last several years. Typically, these failures occur during reflow, however, they are often undetectable (latent) at room temperature. The further along the assembly process that the failures manifest themselves the more expensive they become. If they remain undetected until after the product is placed into service, they become a much greater cost risk, and more importantly, may pose a safety risk."

DON'T PANIC! Let me explain the background of this warning.

For the last few years, a few OEMs have experienced a latent defect in their sophisticated HDI multilayers even though screened with our best available incoming inspection and test methodologies. This defect caused failures observed in:

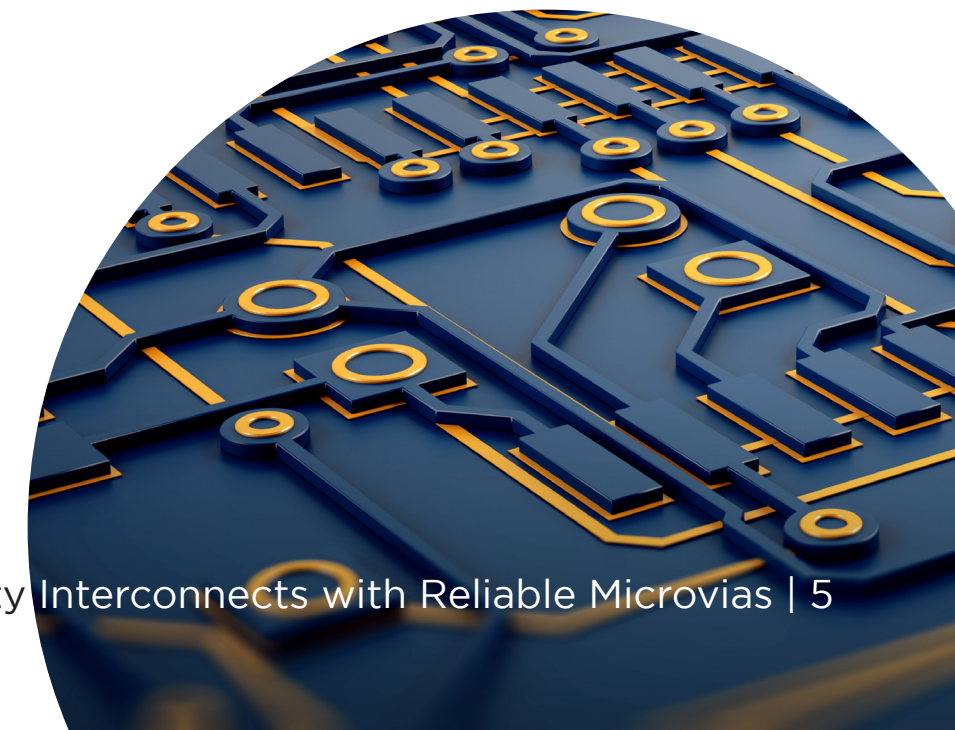
- Post-Reflow In-Circuit Test
- During the "Box Level" Assembly Environment Stress Screening (ESS)
- When removed from storage
- In-Service (End-Customer Fielded Product)

After much work and investigations by these OEMs, and with coordination with the D-32 Thermal Stress Test Methodology Subcommittee, the IPC issues a new test method for thermal stress, (IPC-TM-650, Method 2.6.27A) and thermal shock (IPC-TM-650, Method 2.6.7.2). The Method 2.6.27 calls for the test vehicle or coupon to be subjected to a normal solder paste reflow profile to reach a peak temperature of 230 degree C or 260 Degree C while under connection to a 4-wire resistance measuring unit for six (6) full reflow profiles without the increase of resistance of 5%. The daisy chain in the test coupon needs to be composed of features used in the actual circuits.

This has allowed these OEMs to detect the latent microvia failures and protect themselves from possible defect escapes. But finding the Root Cause of this latent HDI failure has been elusive. So, in early 2018, the IPC organized a select group of industry experts, under the supervision of Michael Carano, to investigate this situation. Later in 2018, this group was named the IPC V-TSL-MVIA *Weak Interface Microvia Failure Technology Solutions Subcommittee*. I am a founding member of this group. But let me emphasize,

During the past year, we have met and gone over test data, microsections and experimental results. Here is what we KNOW:

- The defect manifests itself as a fracture at the metallurgical interface of a microvia to the copper layer below it or to another microvia below it. (see Figure 1)
- First occurrence of the product-level failure detected (stacked microvias) 2010.
- Complex stacked microvias can exhibit this latent defect (>2 stacks) but not staggered microvias.
- Data thus far implies stacked microvia structures, especially stack-heights of 3 or greater, are much more likely to suffer this failure mode, and it is still a minority (but growing) percentage of high-reliability designs.
- Severity of end-use application environment (which we attempt to address by severity of test condition) appears to have some impact on the likelihood of occurrence.
- Several OEMs allow stacked FILLED vias if the design is no more than 2. Three is the tricky one.
- This has been observed in complex HDI structures such as the 3-8-3 Qualification Coupon Design seen in Figure 2 below.
- Product-level failures are unpredictable (in-process, storage or filed)
- Historical industry-standard test methods were insufficient in detecting this failure but seem sufficient for normal HDI constructions.
- Preconditioning and thermal cycling may induce this defect but when it returns to room temperature, the defect is not detectable by 4-wire resistance measurements. Only when the PCB is brought up to reflow temperatures is it apparent.
- IPC TM-650 2.6.27A technique that duplicates assembly reflow will reliably detect this latent problem. (see Figure 3 below).
- Although the committee developed an FMEA for microvia defects, only this one WMI is our focus.
- Additional work by the committee or industry is needed to identify the root cause(s) and implement corrective actions. Volunteer's for this committee are accepted provided they come to work. (contact Chris Jorgensen at IPC or Michael Carano at rbpchemical.net)
- Any industry data pertaining to this problem can be contributed to the IPC and will be used 'anonymously'.



To further read about the WMI Committee and our findings, there is a report available from our APEX 2019 WMI OPEN FORUM [2] and a White Paper was published by the committee, IPC WP-023 “Via Chain Continuity Reflow Test: The Hidden Reliability Threat- Weak Microvia Interface.” Available from the IPC Bookstore.

Further discussions will be undertaken at the upcoming IPC Annual High-Reliability Forum to be held in Baltimore on May 14~16 [3]

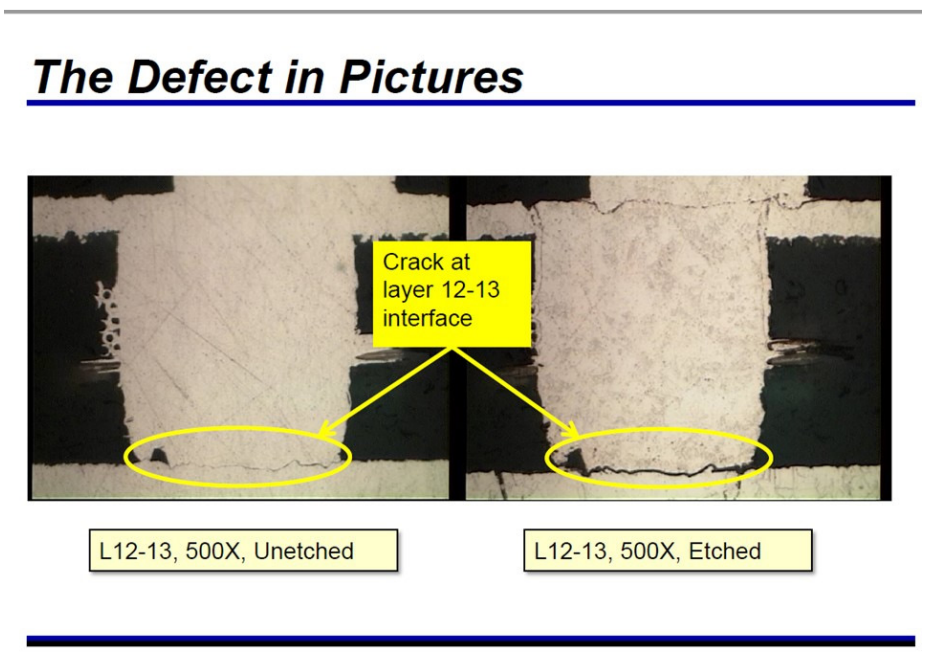


FIGURE 1. The WMI latent defect observed after six reflows of 230 OC. [used with permission][4]

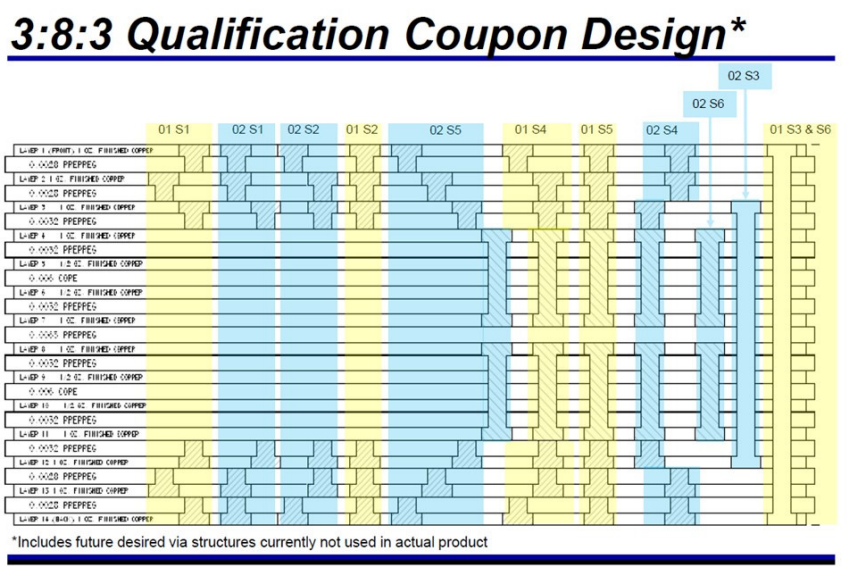


FIGURE 2. A complex HDI qualification coupon (3-8-3) with both stacked and staggered microvia structures. [used with permission] [4]

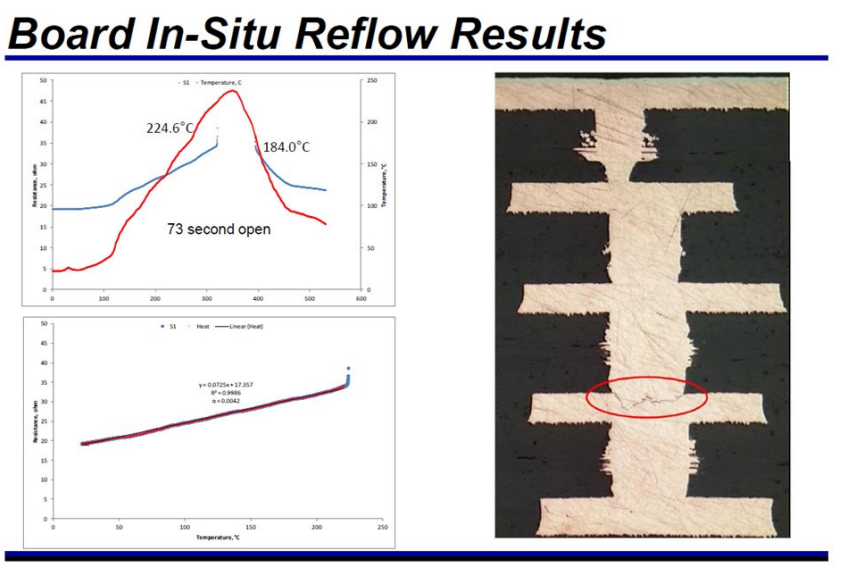
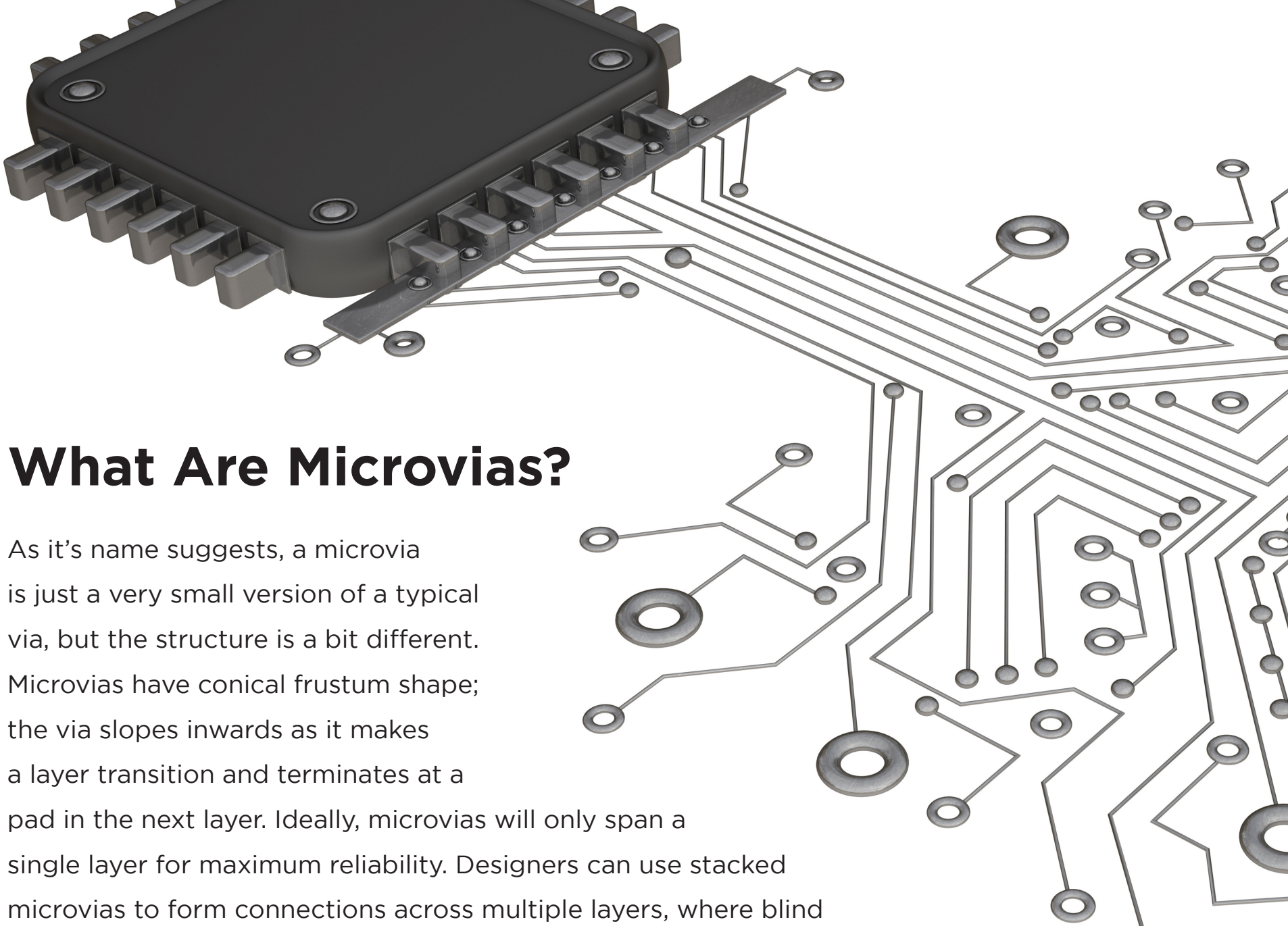


FIGURE 3. Reflow profile and 4-wire resistance of a 4+N+4 stacked microvia structure opening at only 224.6C and closing at 184C on cooling down. Subsequent room temperature testing and thermal cycling testing indicated no defect. [used with permission] [4]

Why Conduct PDN Impedance Analysis?

Have you ever wondered how designers pack so much functionality into such a small space? You can thank HDI design techniques and microvias in printed circuit design. These small structures let traces reach inner layers of a PCB with high interconnect density and high layer count. These structures have been around for years, but they are becoming more common in a variety of systems that require multiple functions on a single circuit board. If you've done a size study and you've determined you'll need 6 mil or smaller traces to fit all your components in your printed circuit board, your design is likely dense enough that microvias are needed to support routing between layers. Here's how these structures are formed and what you need to know about PCB microvias.



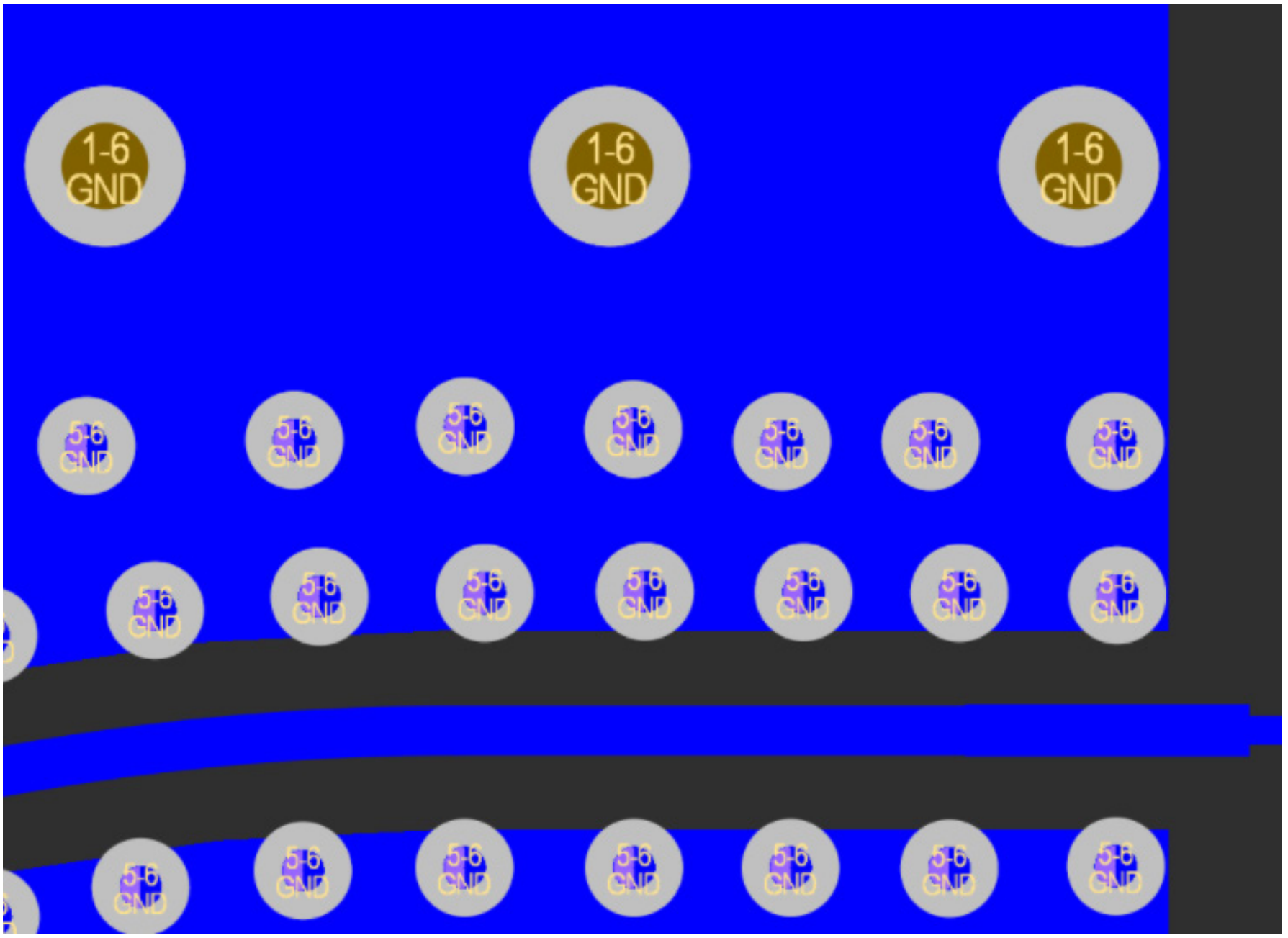
What Are Microvias?

As it's name suggests, a microvia is just a very small version of a typical via, but the structure is a bit different. Microvias have conical frustum shape; the via slopes inwards as it makes a layer transition and terminates at a pad in the next layer. Ideally, microvias will only span a single layer for maximum reliability. Designers can use stacked microvias to form connections across multiple layers, where blind and buried microvias are built up into a stack to reach across multiple layers. These designers are known to have reliability problems, so staggered versions are often preferred. There has been some debate about this point, which I'll outline below.

Microvias in Your CAD Software

Defining microvias starts in the PCB stackup editor, where layer pairs are defined and materials are selected. Note that you need to choose an appropriate laminate that can support the fabrication process you want to use. After building a proposed stackup, I always advise sending it to your fabricator for a review and getting their input as to manufacturability with microvias.

Once you're in the PCB editor, pay attention to the layer pair designation on the pad in the PCB layout. An example from an mmWave RF board with 6 mil vias is shown below. Three through-hole vias are shown in this image for comparison. The 6 mil number is important as this is right at the upper limit of what the IPC considers microvias.



These 6 mil vias (0.67:1 aspect ratio) are being used as a via fence between layers 5 and 6 for a grounded coplanar waveguide. This value for via diameter is right at the upper limit of what would be considered a microvia.

Taking the dielectric layer thickness and the hole diameter together gives the aspect ratio of microvias placed in the PCB layout. Care should be taken when sizing these structures as the aspect ratio is also related to reliability.

Fabrication

Exactly how small are microvias? If you ask most designers, they might tell you that they would consider a microvia to be a via with a diameter less than about 150 Qm (6 mils). Depending on the size of the vias, they can be mechanically drilled and plated (followed by stacking and pressing each layer), or they can be formed with a high-power laser. The latter process is constantly being improved and is preferred in high volume PCB manufacturing thanks to its high throughput. New advances in laser drilling techniques are pushing microvia sizes down to as small as 15 Qm.

After drilling and cleaning, the via hole is plated, either with a sputtering process, electrolytic deposition, or electroless copper plating process. The goal in the plating process is to prevent the formation of voids, dimples, bumps, or any other structural defect in the filled via. Voids are also a reliability concern as stress can concentrate around the edge of the void where copper is thinner if stress is applied to the via structure.

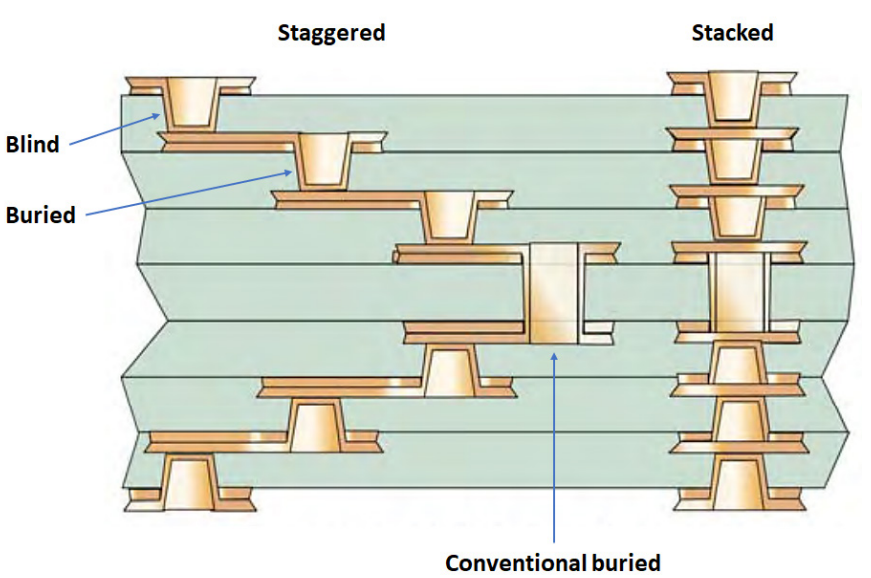
During fabrication, laser-drilled microvias have a lower potential for manufacturing defects than normal vias. Mechanically-drilled microvias can have defects due to drill vibration as the drill wears out, and mechanical microvia drilling is only useful down to 6 to 8 mil diameters, depending on the fabricator's tooling investments. However, microvias are known to be prone to failure during plating, filling, and assembly, prompting the IPC to issue a warning about these reliability concerns in early 2019. To learn more about microvia fabrication, I encourage readers to look at this article on HDI manufacturing by Happy Holden.

Types of Microvias

There are a few different types of microvias. All microvias have two common characteristics:

- **Low aspect ratio:** Contrary to through-hole vias in typical PCBs, microvias have small aspect ratio. The aspect ratio of these vias is preferably 0.75:1. Larger aspect ratios of 1:1, or even as high as 2:1, can be fabricated, but they bring reliability concerns. Because of this, they typically only span between a single layer. Note that a microvia aspect ratio that is greater than 1 does not meet the IPC definition of a microvia.
- **Susceptible to fracture at the neck:** High aspect ratio through-hole vias (~10:1) tend to be most susceptible to fracture near the middle of the via barrel. Due to the plating method used in microvias, copper curves inward to the barrel region and stress tends to concentrate there. As a result, microvias are most susceptible to fracture in the neck region under repeated thermal cycling, strong vibration, or mechanical shock.

Aside from these qualities, the differences between microvias are simply their typical diameter and where they appear in a circuit board. Microvia-in-pad configuration is common with fine-pitch BGA components, where the small distance between solder balls will not allow a dog bone fanout. Microvias on the surface layer can also be placed in a pad, filled with a conductive epoxy or electrodeposited copper, and plated over with copper (this is the microvia analogue of via-in-pad plated over, or VIPPO, for standard via sizes). The in-pad configuration has advantages in that the pad is now solderable, but the internal fill and the copper wrap plating on the via are now the main reliability concerns.



This illustration should the general uses and types of microvias that can be placed in an HDI PCB. Note that you can have a traditional buried via structure or through-hole structures in the same layer as microvias (see the PCB layout image above).

With these points in mind, here are the different types of microvias:

Blind Microvias

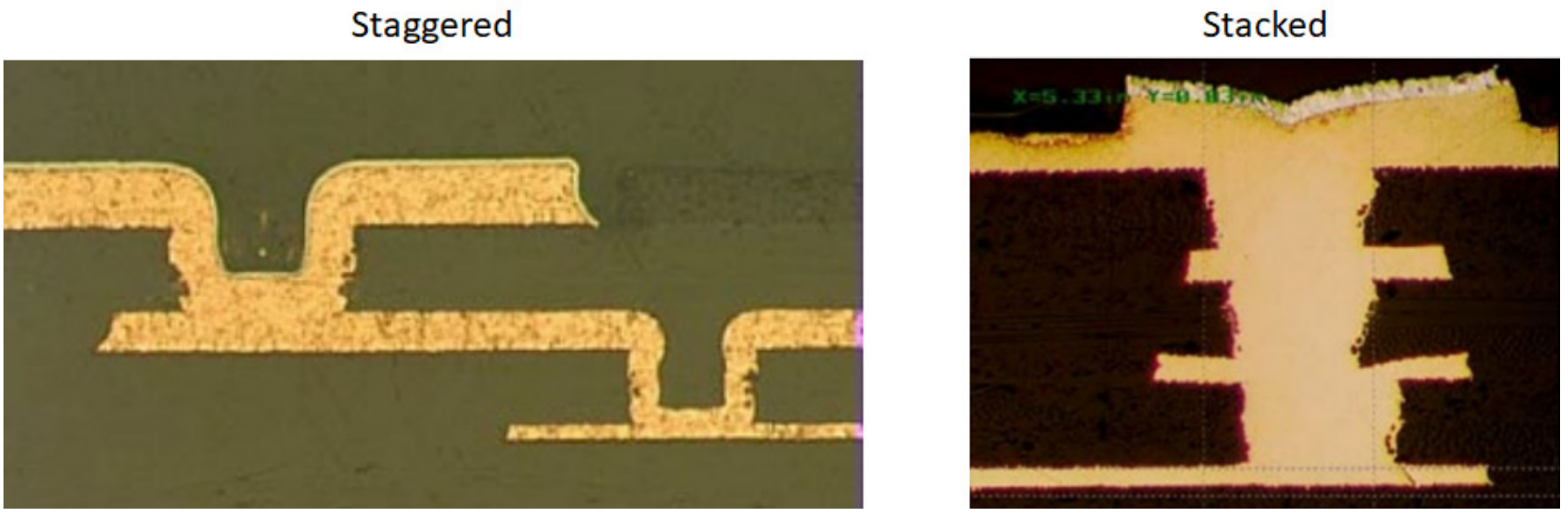
Blind microvias start in the surface layer and terminate 1 layer below the surface, although they could terminate or **2 layers** below the surface layer if the aspect ratio is kept low. If you need to span 2 layers, it's better to use stacked microvias (see below) or staggered microvias as these will be more reliable. Blind microvias could be filled or unfilled.

Buried Microvias

Buried microvias have basically the same structure as blind vias and span between two interior layers and do not reach either circuit board surface. Just like blind microvias, it's best the aspect ratio stays low and they span a single layer to ensure reliability and ease of fabrication. These vias are filled with copper, either using a plating process with pure copper or with a epoxy + copper resin to ensure a strong connection across the head of the microvia. It's important that the process being used for plating results in void-free structures to ensure maximum reliability.

Stacked and Staggered Microvias

You may be a bit hesitant to try incorporating lots of buried and blind vias into your designs, but the layer-by-layer process for forming low aspect ratio microvias makes them useful in stacked applications. Stacked microvias are simply stacks of buried vias, or a blind microvia stacked on top of buried microvias. This is the standard way to span between multiple layers in an HDI PCB. The internal buried microvias in the stack need to be filled with conductive paste and plated over to ensure strong contact as the next via in the stack is deposited and plated. The alternative to stacked microvias is staggered microvias, where microvias on successive layers are offset from each other.



Cross-sectional microscope images of staggered and stacked microvias. Image credit: Susy Webb, Overcoming the Challenges of HDI Design, AltiumLive 2018.

The design decision that needs to be made with stacked and staggered microvias, as well as individual blind/buried microvias, is the aspect ratio to be enforced in the design. Stacking is also important due to potential failure at the interface between vias in a stack.

Filled or Unfilled?

Microvias can be either filled or unfilled with copper. For buried microvias, it's important to fill the via hole with copper, especially if there will be any stacking. If any voids are left over in the interior of the via plating, then the via will experience high stress concentration along the via wall, which could lead to premature fracture during reflow or during operation. Blind microvias can be left unfilled, and this was typical in the early days of microvia fabrication and implementation. If blind microvias will be used in-pad, then they should be filled with a standard process.

The manufacturer will use pure copper or an epoxy +copper resin for plating. The typical process normally begins with conformal plating, followed by pulsed plating to fill in the body of the microvia with solid copper and eliminate voids. Plating processes that do not use some additive in the filler material typically results in void formation inside the body of the plating volume. Even if the microvia body is totally filled with copper, the copper may concentrate along the walls and the top surface of the if additives are not used during plating. Conformal plating also contributes to an uneven deposition of copper along the via body, leading to voiding.

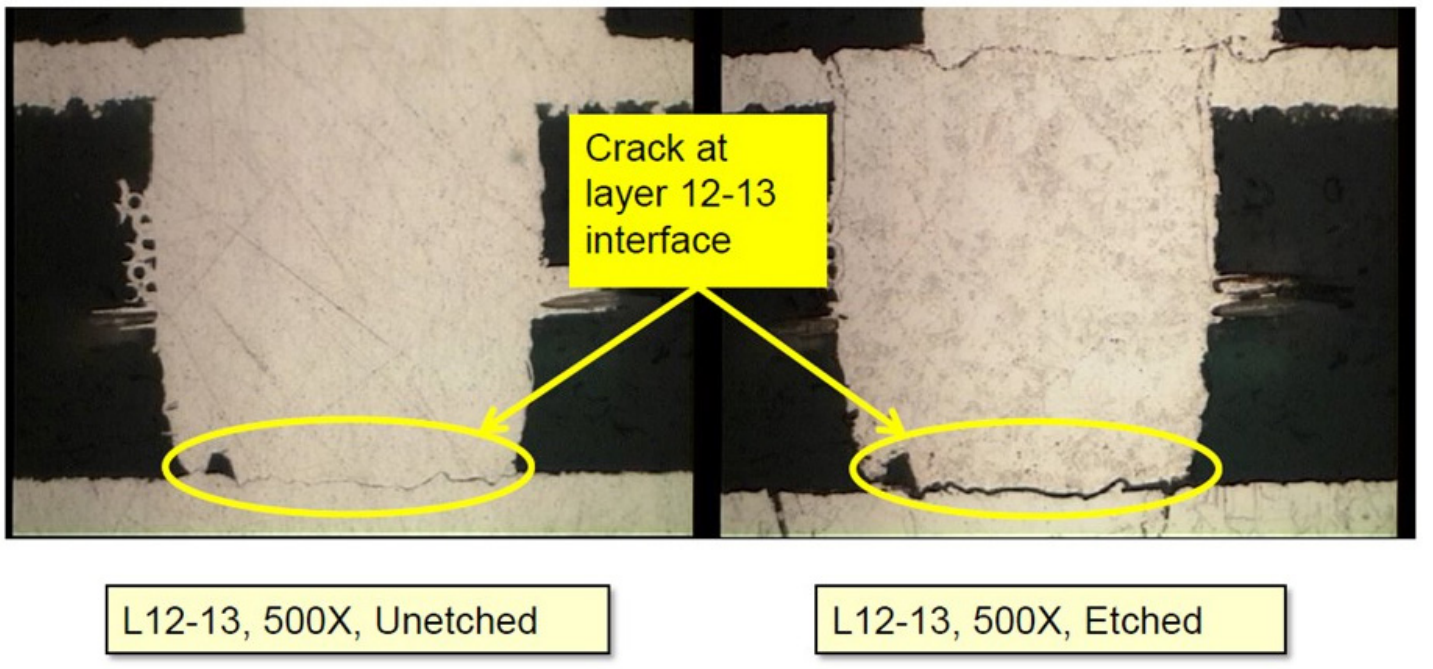
Reliability Debates

I mentioned above that there has been some debate around the reliability of individual blind/buried microvias and stacked microvias. In particular, the interface between microvias in a stack and the butt joint at any copper wrap plating are known to be points of failure. The exact time to failure appears to depend on several factors, including:

- The aspect ratio of each microvia in the stack
- The number of microvias in a stacked
- The size of any voids that form in the filling material during plating
- Copper plating thickness (either wrap plating or thickness of the via barrel) at the corner of the top pad/via hole

The reliability concerns center around thermal cycling. As the design is thermally cycled, including during assembly, the PCB substrate can expand and extert high stress on the thin copper plating used in a microvia. As a result, failure can occur at plated interfaces, meaning the interface between two stacked microvias, and at the interface between a via and its capture pad. The second most common location is at the knee (where copper slopes into the via at the top pad), particularly if some plating is removed and the remaining copper is very thin.

Some of the typical failure modes are shown below, specifically at the via/via or via/pad interface, as well as at the top of the via at the plating interface.



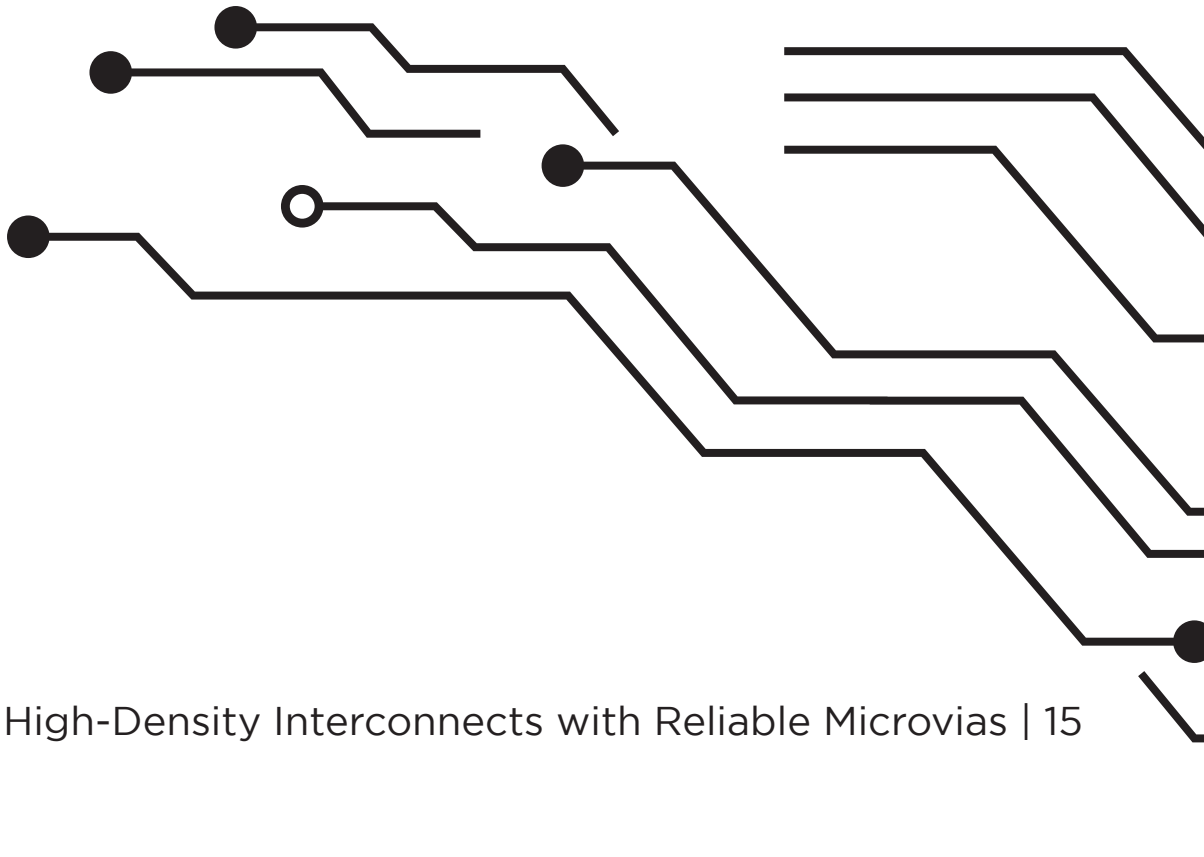
Read more these defects in Happy Holden's article on the IPC reliability warning.

Although the specific criteria that can be used to concretely judge reliability are still unclear, there are a few points everyone seems to agree on:

- Smaller aspect ratios tend to be more reliable. In the paper from Lesniewski (see below), 0.7 aspect ratio microvias could survive accelerated life testing, while aspect ratio 1 microvias failed after only a few thermal cycles.
- Voiding appears to be related to failure, but this depends on the shape of the void, volume void fraction, and aspect ratio. One cannot make a general statement that voids always increase failure rate for all aspect ratios and void sizes.
- Due to inconsistencies in reliability of stacked vs. staggered microvias, it's generally accepted that there should be no more than two microvias in a vertically stacked arrangement; other microvias in a vertical interconnect should be staggered.
- The presence of copper wrap plating on the top portion does not appear to be related to failure, rather the plating thickness at the butt joint is a greater predictor of failure.

For more information, take a look at these references, as well as the article from Happy Holden I've linked above.

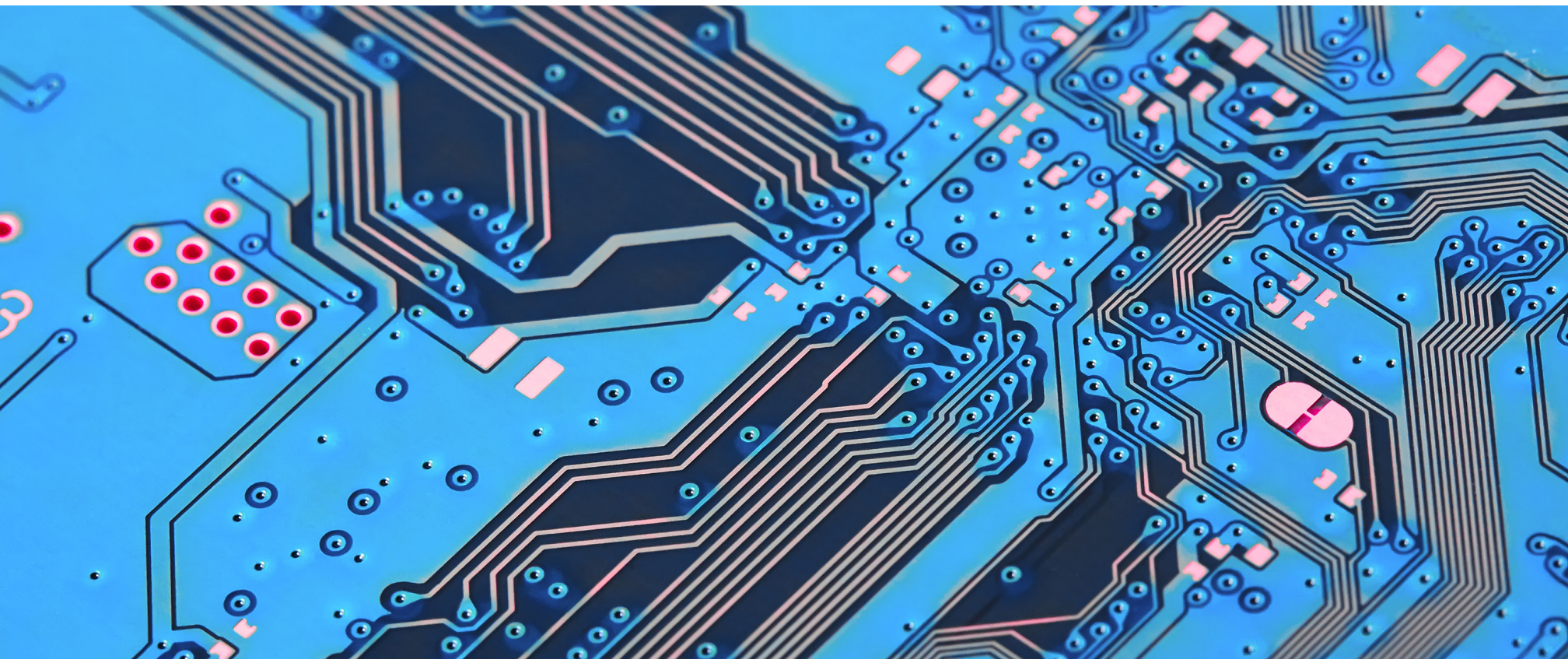
- Lesniewski, T. *Effects of Dielectric Material, Aspect Ratio and Copper Plating on Microvia Reliability.* Link.
- Heer, H., & Wong, R. *Reliability of Stacked Microvia.* Link.
- Birch, B. *Reliability Testing for Microvias in Printed Wiring Boards.* Link.



Space Advantages

Aside from some fabrication difficulties for less-advanced manufacturers, microvias are ubiquitous in HDI PCBs and they are responsible for saving space in these boards. For fine-pitch components in dense boards, they are required to ensure components can be packed into small spaces. Circuit board space is money, and microvias will help lower your costs. Aside from allowing more dense connections between layers and with smaller traces, they also allow you to save space by placing a via directly in-pad. Microvias-in-pad also save you space by making connections inside the pads of surface mounted technologies (SMTs). Microvias are especially well-suited for this because of their small form factor. Sometimes, normal vias are too large to fit inside pads for SMTs like fine pitch ball grid arrays (BGAs). Microvias can fit inside the pad without causing any fabrication issues.

In addition to BGA breakout, microvias-in-pad will fit inside the pads of even the finest pitch BGAs, and they can be even more useful in breakout channels. Even if you use microvias-in-pad to save surface space, you'll still need lots of layers to get those trace elsewhere on the circuit board. Using microvias can increase escape path width, possibly letting you use fewer layers to breakout a BGA.

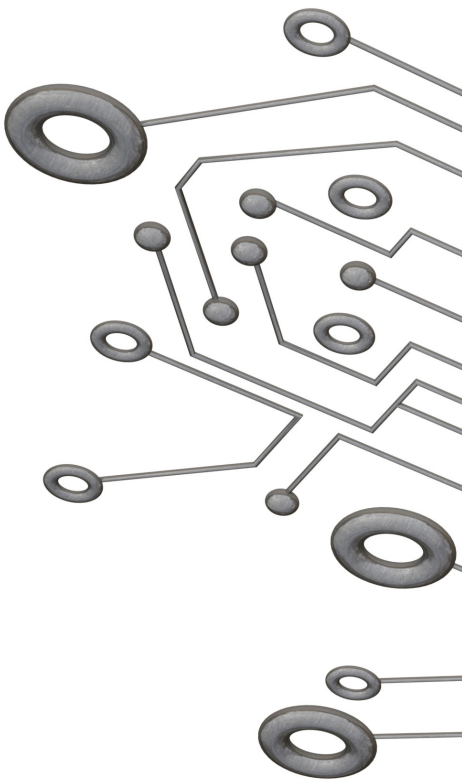


EMI Advantages

Microvias have had a major effect on signal integrity in HDI circuits. The fact that microvias carry smaller parasitic capacitance and inductance, simply due to their small size, is one factor that allows them to be packed closer together without increasing crosstalk and noise coupling strength. The smaller parasitics negatively compensate for the stronger electromagnetic field when HDI traces and microvias are closer together.

One of the big problems in high-speed circuits is signal radiation and reflection in vias. In addition, a resonance in a large via stub can couple with high field strength into a neighboring via. In essence, large vias make great high frequency radiating antennas, especially when a signal is allowed to resonate in a stub. A good way to reduce an antenna's power is to reduce its size. Microvias are basically like smaller antennas, so they will already have smaller emission and absorption cross section compared larger vias. Microvias are also made layer by layer, which means there won't be any stubs. As they are implemented in thinner dielectrics, they are also closer to GND planes and will have greater shielding. All of these points are reasons microvias and HDI interconnects in general tend to have fewer problems with radiation.

Now that you've got microvias in printed circuit design covered, you need the right PCB design software to create your next HDI PCB. Altium Designer® can help you enhance your advanced HDI PCBs with microvias and a wide range of other tools. Altium Designer on Altium 365 delivers an unprecedented amount of integration to the electronics industry until now relegated to the world of software development, allowing designers to work from home and reach unprecedented levels of efficiency.



Advanced High Density PCB Design in Altium Designer

HDI PCB design and manufacturing push electronics and circuit boards to their limits. As electronics become faster and more capable, they require greater functionality in a smaller package. From smartphones to smartwatches and other IoT devices, HDI design is slowly becoming the norm rather than the exception. Keeping up with new technology and design techniques means that designers need to rethink how they layout components, as well as design interconnects and vias in their boards.

If you want to be successful with your next high-density PCB design project, you need the right design tools to help with routing and rules checking. Only Altium Designer integrates rules checking into your layout and routing tools, giving you a complete platform for advanced electronics design and much more.

The only unified PCB design package with a full suite of CAD tools for high-density PCB design, layout, and routing on multilayer HDI boards.

Modern electronics carry more components and functionality than ever before, and designers need to understand many of the finer points of high density interconnect (HDI) PCB design. It starts from a simple idea: reduce the size of traces, vias, component, and pads in order to fit more components into a smaller area. However, this requires changing the manufacturing process, and any HDI PCB needs to be manufacturable at scale. Here's what goes into successful high-density PCB design and routing:

- HDI PCB Stackup Design
- Defining Microvia structures
- BGA Breakout in HDI Boards

Altium Designer gives you everything you need for success in these areas and much more. Here's how you can be successful when designing your next HDI PCB and how you can prepare for circuit board manufacturing with HDI PCB processes.

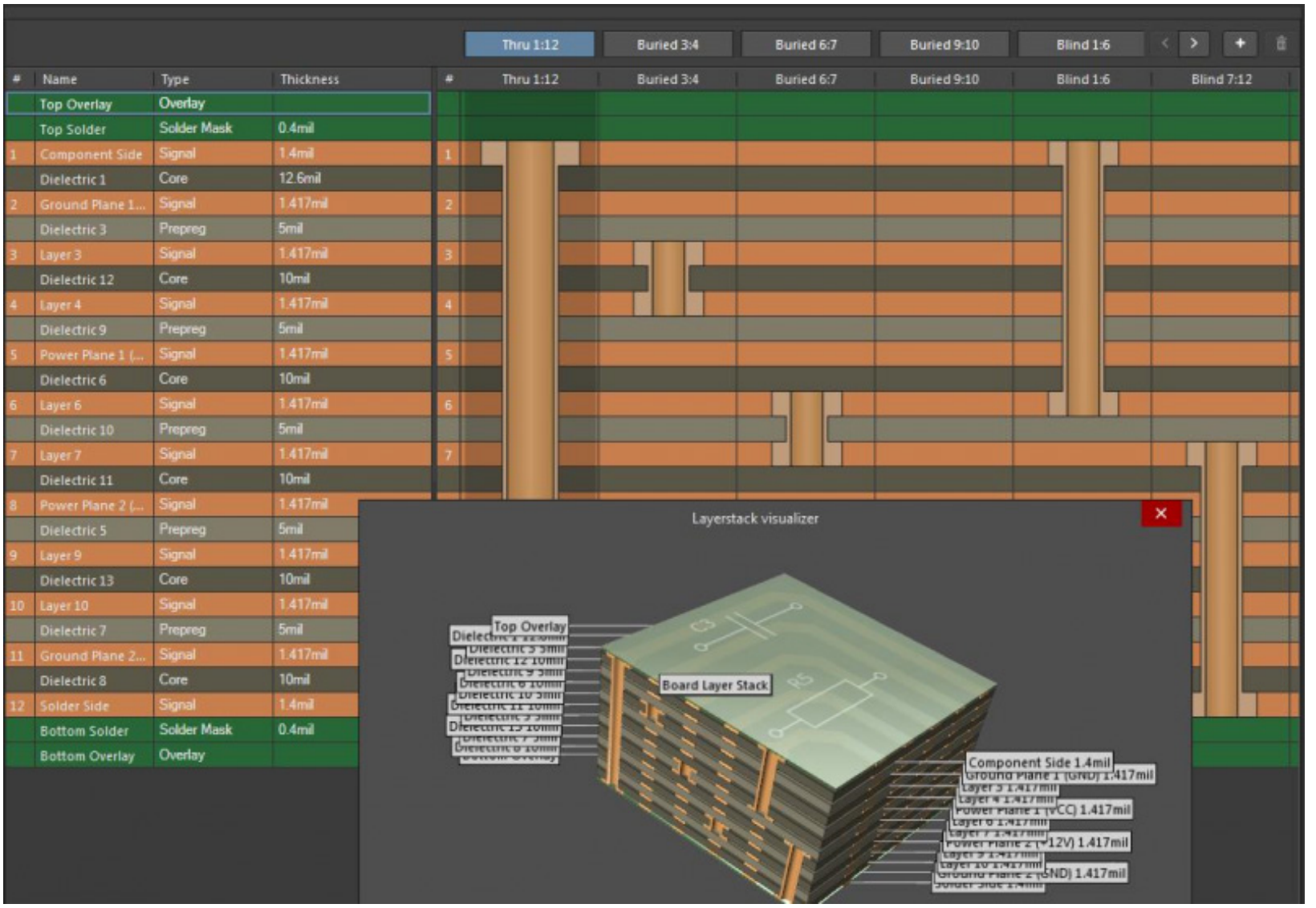
HDI PCB Stackup Design

Implementing HDI design techniques on your board requires designing the right stackup. You'll need to ensure that you can route the high density of signals you need between components while providing EMI shielding and ensuring signal integrity. Accessing the inner signal layers requires designing the right vias and designing landing pads that link directly to your traces. Your PCB stackup forms the foundation of your HDI boards, and working with the right stackup will make your routing and layout tasks much simpler.

Creating an HDI PCB Stackup

An HDI PCB stackup does not require a specific number of layers. Any circuit board with 8 to 32 layers or more could be considered an HDI board when the trace widths are small enough. Altium Designer gives you access to a powerful set of via design tools for working with multilayer HDI boards and a layer stack manager to create your new circuit board substrate. The right layer stack manager allows you to place as many layers as you like in your HDI circuit board and define via transitions between each layer.

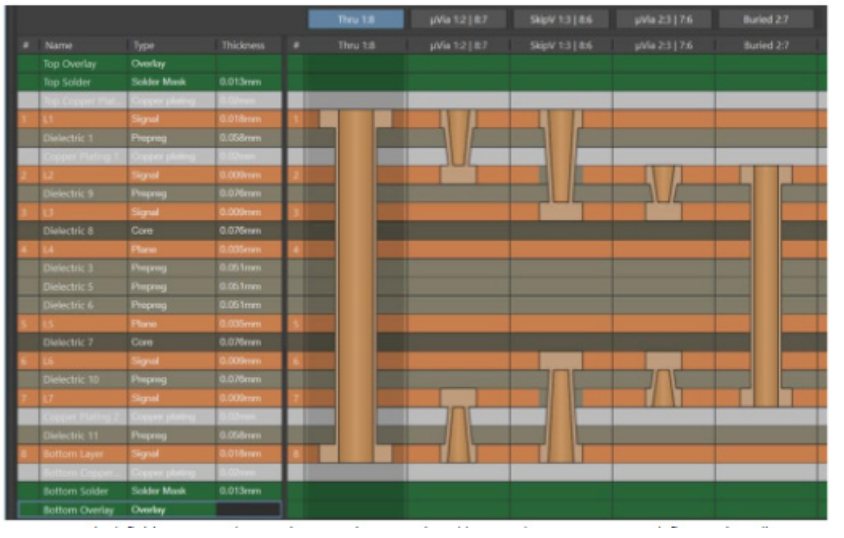
- Routing between the inner layers of your HDI PCB takes creative use of vias. You can save a significant amount of space with blind and buried vias. Learn about working with blind and buried vias in HDI PCBs.
- Multilayer boards are a mainstay in high-density PCB design, and you'll need to choose the right HDI stackup for your particular application. Learn more about designing your stackup for HDI PCBs.
- Designing vias for HDI PCBs is easier than you think when you use the right PCB design software. See how you can design blind and buried vias in Altium Designer.



Controlled impedance routing in HDI boards requires an accurate impedance calculator in your layer stack manager.

Defining Microvia Structures

HDI boards require the use of microvias for layer transitions. Microvias are simply small vias that require a specialty manufacturing process (i.e., other than mechanical drilling). These structures are defined by the IPC-2226 HDI Design Standard. The various microvia structures you can access in Altium Designer are shown below, which includes staggered, skip, and buried types of microvias.

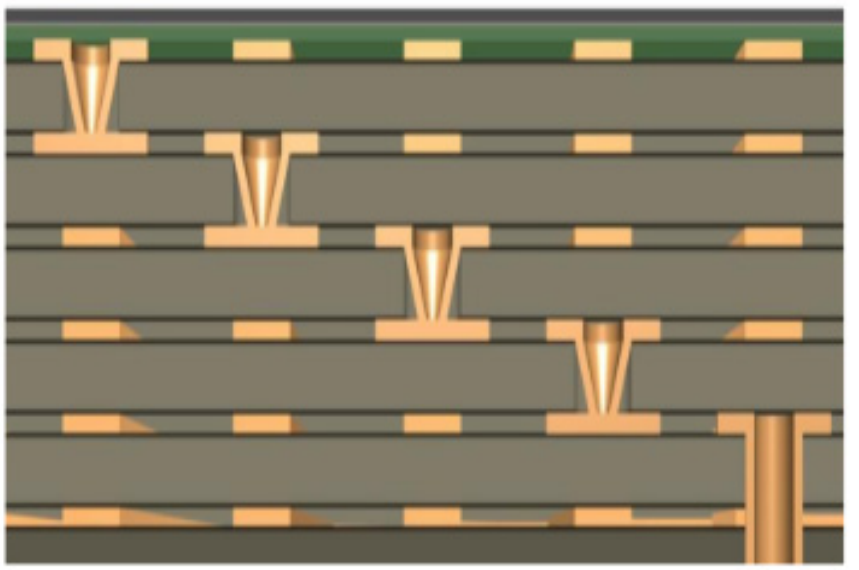


HDI PCB via definition in Altium Designer's layer stack manager.

Staggered Blind Vias

Staggered microvias on a single side or both sides with buried through-hole vias between inner layers is the most common and lowest cost HDI PCB layer stackup. When using multiple microvias to connect inner layers, it is preferred the microvias be offset by some angle and the vias not be stacked (e.g., as in a crankshaft). This will minimize any thermal excursions if the vias heat up to high temperatures. Be sure to contact your circuit board fabricator for material and process compatibility if you plan to produce an HDI PCB at high volume.

See how you can design blind and buried vias in Altium Designer.

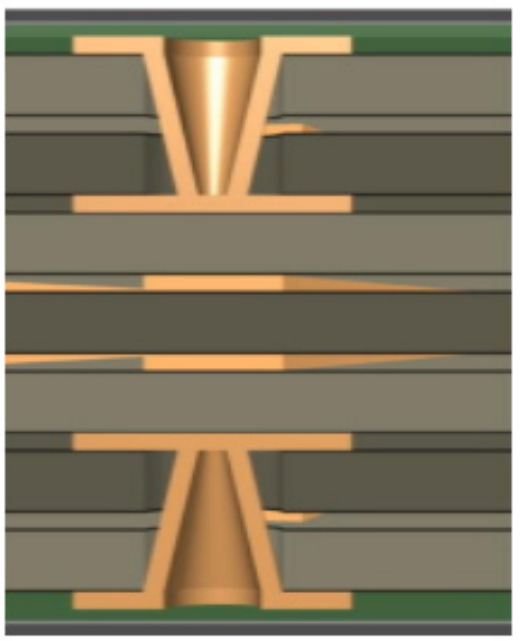


Build-up of multiple HDI PCB layers connected with buried vias.

Skip Blind Vias

A skip microvia is special in that it is used to 'skip' the next adjacent layer, as seen in Figure 7. Because a skip microvia can be the deepest of microvias, it is important that the designer be aware of a fabricator's capability to produce and metallize such a microvia. Many circuit board manufacturers will not have this capability and will give your board no-bid status if they spot this in your Gerber files. With all blind vias, the aspect ratio may be reduced to 0.7:1 or even 0.65:1, so that the surface pad and target pad will be larger than the via length. The via is quite susceptible to fracture at its neck when light copper foil is used to place these vias.

Learn more about skip vias in your high-density PCB layout

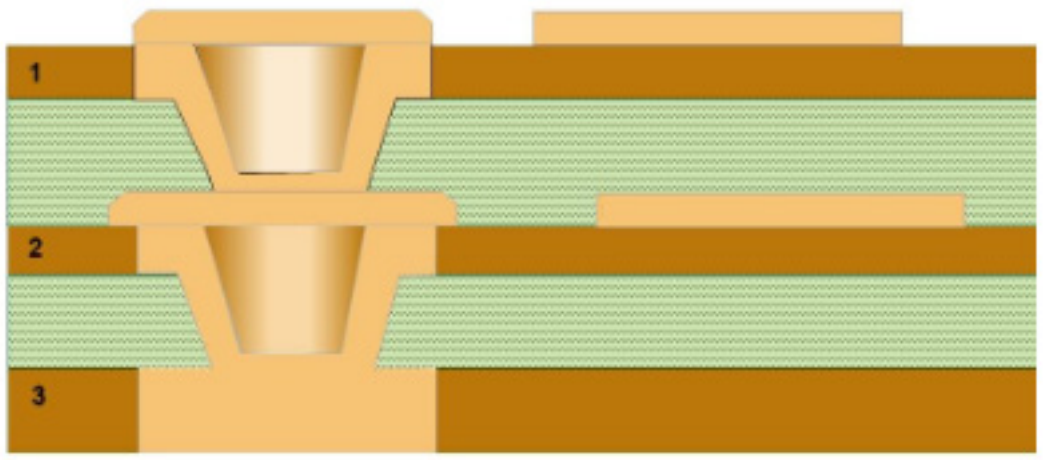


A skip microvia can be used to skip a layer in a multilayer circuit board.

Stacked vias

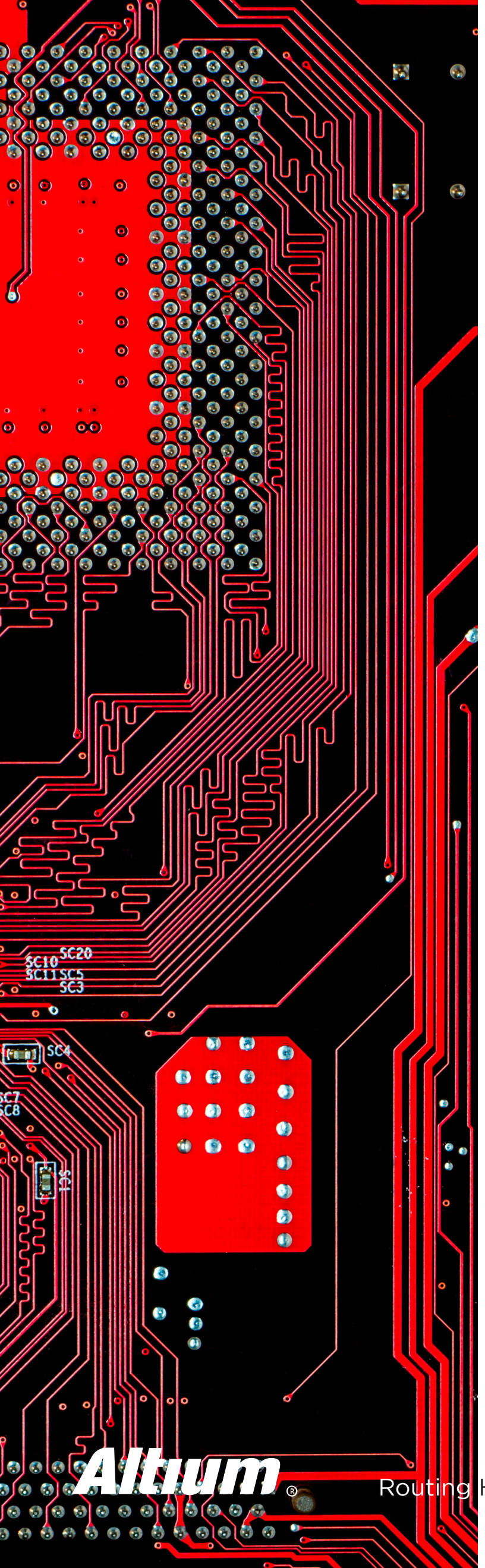
Stacked microvias use the least amount of board real-estate but are significantly more difficult to fabricate. This stems from the need for the target land of the top microvia having a solid metal surface to connect to. The process requires filling of the microvia either with conductive materials and plating it over (VIPPO) or with the use of "super-fill copper plating" capable of solid copper plating the microvia interior (see the image below).

Learn more about skip vias in your high-density PCB layout



Stacked microvias require a solid metal surface for the 'landing pad' on top of the microvia. The lower portion of the microvia is produced with a laser, and the void is filled and plated over.

Currently, it is recommended that stacked microvias not be stacked on top of a mechanically-drilled buried via. Reliability concerns have arisen from this practice. Be sure to contact your PCB fabricator about this construction and read the IPC White Paper on Performance-Based Printed Board OEM Acceptance-Via Chain Continuity Reflow Test: The Hidden Reliability Threat-IPC-WP-023 (May 2018).



Mechanically Drilled Blind/Buried Microvias

Microvias can also be mechanically drilled, although these usually have larger diameters (>6 mil) than laser drilled microvias and have low aspect ratio. The cost per via is also higher than the cost per laser drilled via as these thin drill bits fracture often and need to be replaced frequently.

Learn more about mechanically drilled and laser-drilled microvias.

BGA Breakout in HDI Boards

Fine-pitch BGA fanouts are routed either using microvia-in-pad or by using a microvia that is only touching the SMT pad. Note that, for 0.5 and 0.4 mm pitches, the via holes are not in the center of the lands. This is to increase spacing between traces on the inner layers beyond a minimum of 0.075 mm. When selecting design rules for fine-pitch BGAs, be sure to contact your PCB fabricator to determine which geometries and tolerances they can support.

In addition to the traditional N-S-E-W dogbone breakout of BGAs, microvias facilitate two new BGA breakout methods that greatly increase routing density and lower layer counts. This is thanks to the much smaller size of microvias. These two methods are channels and swing-via placement.

BGA Breakout in HDI Boards

Fine-pitch BGA fanouts are routed either using microvia-in-pad or by using a microvia that is only touching the SMT pad. Note that, for 0.5 and 0.4 mm pitches, the via holes are not in the center of the lands. This is to increase spacing between traces on the inner layers beyond a minimum of 0.075 mm. When selecting design rules for fine-pitch BGAs, be sure to contact your PCB fabricator to determine which geometries and tolerances they can support.

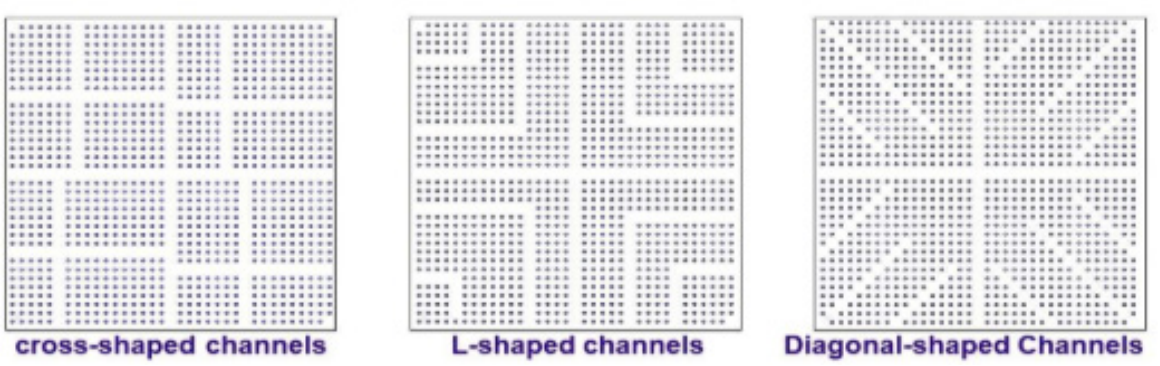
In addition to the traditional N-S-E-W dogbone breakout of BGAs, microvias facilitate two new BGA breakout methods that greatly increase routing density and lower layer counts. This is thanks to the much smaller size of microvias. These two methods are channels and swing-via placement.

Channels

When a BGA's total number of signal escapes begin to exceed 400 pins, microvias should generally be used for breakout as rows that cross the BGA, rather than on the peripheral. These form 'channels' on the inner-layers and far side of the circuit board. These channels allow access to internal signals in the BGA, thus fewer layers are required for total breakout.

The BGA in Figure 11 is an 1153 pin (34x34) BGA (1.0 mm pitch) and with 132 possible routes per layer (1 trace between vias) plus 20 traces in the channel (5 traces). This means that 8 layers would be required (plus 5 separating plane layers) to connect this BGA to the rest of the circuit board.

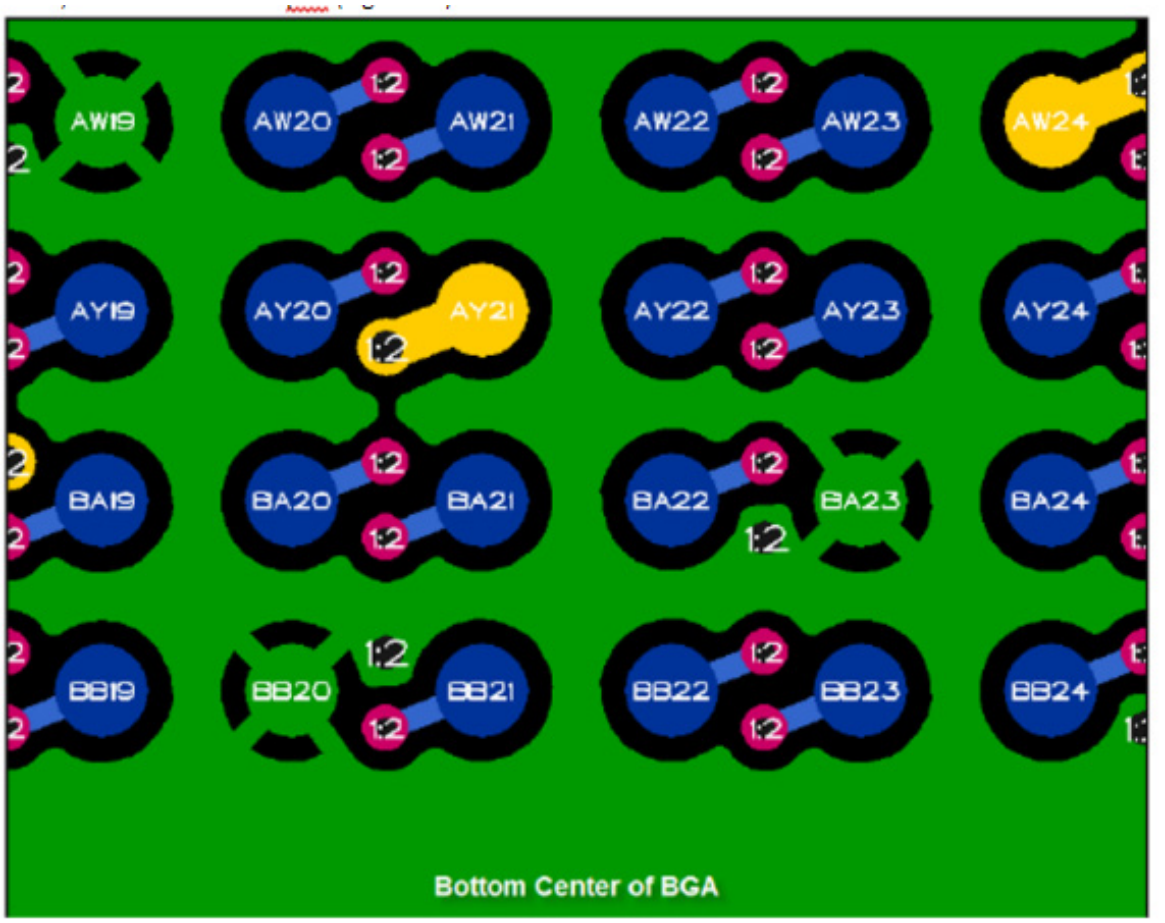
If we create more routing channels, we connect more traces per layer and reduce the total number of layers. Channel routing uses blind microvias to form up to 4 additional cross-shaped, L-shaped, or diagonal channels in a BGA fanout. These new channels allow up to 48 extra connections per layer (8x6 traces). Two routing layers and two plane layers can be eliminated.



Routing channels formed by microvias to ease breakout from large BGAs. Channels can be cross-shaped, L-shaped, or diagonal.

Swing Break-Outs for Boulevards

A swing via is actually a pair of vias that are fanned out between two BGA pads to maximize the available area for routing conductors between them. Instead of placing a single breakout via in a standard N-S-E-W dog bone fanout, smaller microvias are used to give enough room for two adjacent breakout vias, as shown in Figure 13. The microvia pads are so much smaller than a through-hole pad that there is room for a surface ground flood down to a 0.65 mm pitch.



Example of swing breakout for a large 0.8 mm pitch BGA that includes surface ground fill.

High-Density PCB Design in Altium Designer

With the right design software, you'll be able to define the trace geometry, via size, and layer stackup that you need to pack high functionality onto your board. Working with a design package that integrates your HDI circuit board design tools into a single interface gives you everything you need for HDI design in a single program.

Altium Designer Offers the Only Rules-Driven PCB Design Environment

As design rules are so important for ensuring manufacturability, you need a program that integrates your HDI circuit board layout features with online DRCs. In Altium Designer, the rules-driven design checks your HDI PCB layout against standard and custom design rules, which helps you spot and correct DFM errors quickly. You'll have access to all this and more in a single design program. No other design program provides this level of consistency and productivity.

- Altium Designer's rules-driven design engine allows your design tools to be easily adapted to advanced circuit boards, including HDI PCB designs. Learn more about the rules-driven design environment in Altium Designer.
- Microvia design is an important aspect of any high-density PCB layout. Altium Designer gives you the tools you need to design microvias for your next HDI PCB. Learn more about microvia design in Altium Designer.
- You can easily adapt the design tools in Altium Designer to HDI PCB circuit board thanks to the underlying rules-driven design engine. You'll be able to design your next high-density PCB layout to exacting industry standards. See how Altium Designer can be easily adapted to HDI design.

If you need to implement high-density PCB design and routing techniques in your PCB, you need a design platform that unifies your circuit board layout features with your design rules. Instead of using separate PCB programs with outdated workflows, you need to work in a single environment with all the tools you need. Watch as your HDI designs come to life with Altium Designer.

Altium Designer on Altium 365 delivers an unprecedented amount of integration to the electronics industry until now relegated to the world of software development, allowing designers to work from home and reach unprecedented levels of efficiency.

We have only scratched the surface of what is possible to do with Altium Designer on Altium 365. You can check the product page for a more in-depth feature description or one of the On-Demand Webinars.

How to Setup HDI PCB Layout and Routing in Your PCB Design Software

A HDI PCB layout can get very cramped, but the right set of design rules will help you design successfully.

More advanced PCBs are packing more functionality into smaller spaces, often with customized ICs/SoCs, higher layer counts, and smaller traces. Getting the layout for these designs correct requires a powerful set of rules-driven design tools that check your routing and layout against design rules as you create your PCB. If you're working on your first HDI layout, it can be difficult to see which design rules you'll need to set when starting your PCB layout.

In this article, we'll look at the critical design rules to set when preparing an HDI PCB layout and some tips for working more efficiently. Altium Designer includes a convenient interface that makes these rules easy to access and edit, but the rules shown here are universally applicable in any design platform.

Setting Up Your HDI PCB Layout

For an HDI PCB, there is generally little that distinguishes these products from what one would consider a standard PCB other than component and routing density. I've seen designers state that an HDI board is anything with 10 mil or smaller vias, 6 mil or smaller traces, or anything with 0.5 mm or smaller pin pitch. Your fabricator will tell you HDI PCBs use ~8 mils or smaller blind vias, where the smaller vias are laser-drilled.

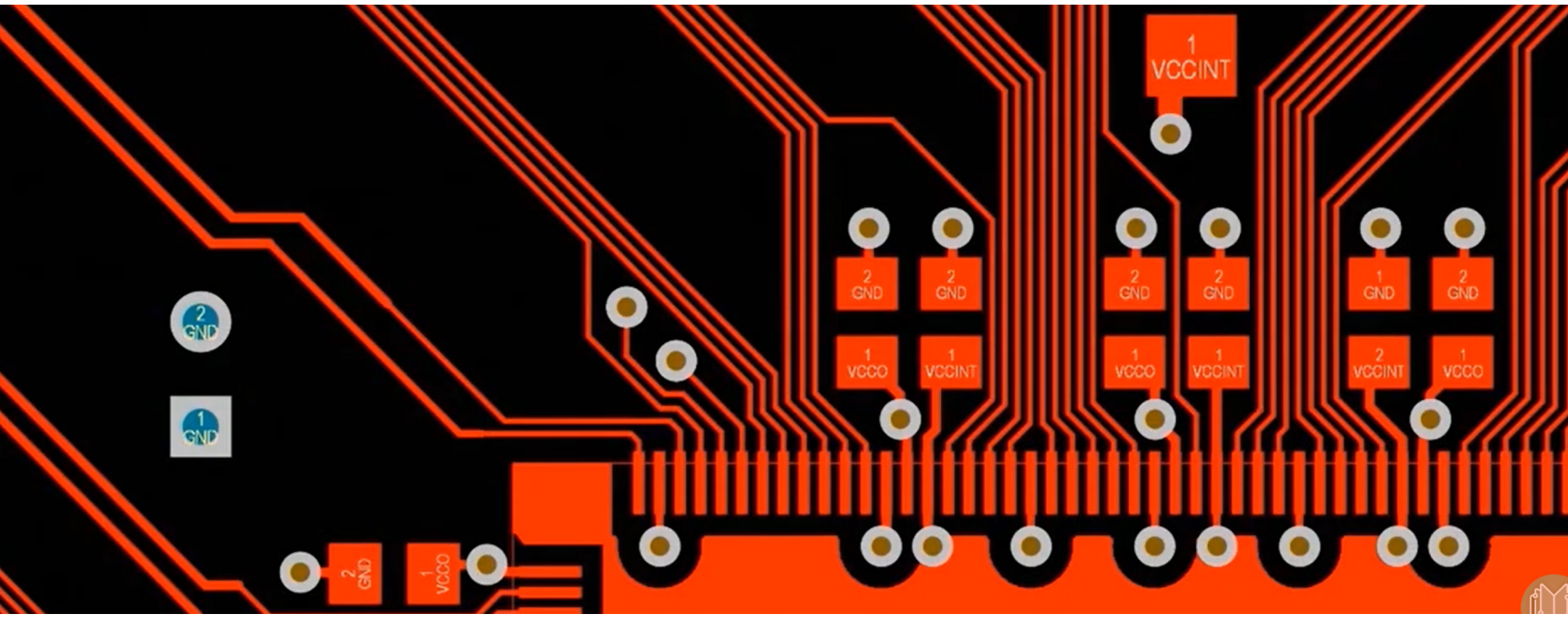
In some ways, they're all correct as there is no specific threshold for what constitutes an HDI PCB layout. Everyone can agree that, once a design contains microvias, it's an HDI board. In terms of design, you'll need to set up certain design rules before you ever touch your layout. You should gather your fabricator's capabilities before you set up your design rules. Once you've done this, you'll need to setup design rules and some layout features

- **Trace width and via sizes.** A trace's width is related to its impedance, and the trace width will determine when you enter the HDI regime. Once the trace width becomes small enough, vias will also become so small that they must be fabricated as microvias.

- **Layer transitions.** Vias need to be designed carefully based on aspect ratio, which also depends on the desired layer thickness. Layer transitions should be defined early so that they can be quickly placed during routing.

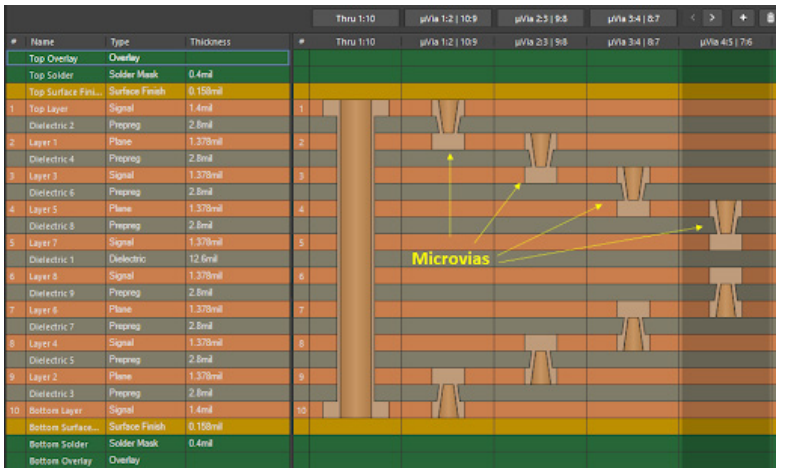
- **Clearances.** Traces need to be kept separated from each other, and from other objects that aren't part of a net (pads, components, planes, etc.). The goal here is to ensure compliance with HDI DFM rules and prevent excessive crosstalk.

Other routing constraints like trace length tuning, maximum trace length, and allowed impedance deviation during routing are also important, but they will apply beyond HDI boards. Here, the two most important points are via sizes and trace widths. Clearances can be determined in a number of ways (e.g., simulation), or by following a standard rule of thumb. Be careful with the latter as this may create a situation with excessive crosstalk on an inner layer or insufficient routing density.



Swing Break-Outs for Boulevards

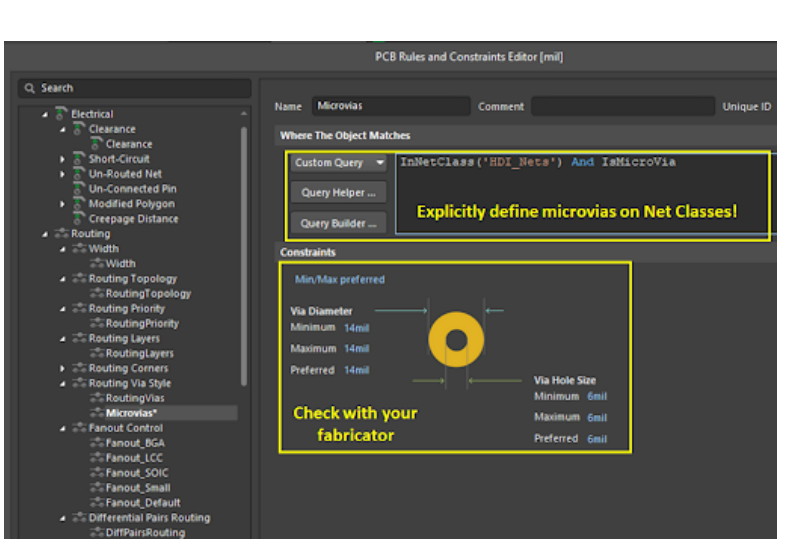
HDI stackups can range from several layers up to dozens in order to accommodate the required routing density. Boards with high pin count fine-pitch BGAs can have hundreds of connections per quadrant, so vias need to be set up when creating the layer stack for an HDI PCB layout.



Defining microvias in an HDI PCB stackup.

If you look at the layer stack manager in your PCB design software, you may not be able to explicitly define specific layer transitions as microvias. That's okay; you can still set up layer transitions and then set your via size limits in your design rules. In Altium Designer, you can create via transitions in the Layer Stack Manager and label them as microvias in the Properties panel.

This ability to specifically call out a via as a microvia is useful once you go to set up design rules and create via templates. To set up your design rules for routing with vias, you can define a design rule as only applying to microvias. This lets you set specific limits on clearances, via pad size, and hole diameter. In Altium Designer, you'll want to use the "IsMicroVia" portion of the custom query below to ensure the design rule applies to microvias on a specific Net Class.



Setting microvia design rules for HDI routing

Note that the via width and pad size defined here were taken from fabricator capabilities for an earlier project. You should consult with your fabricator regarding their capabilities before you start setting up design rules. Your trace width then needs to be set in your design rules to ensure your trace impedance is controlled to the desired value. In other cases, where impedance control is not needed, you may still want to limit trace width in an HDI board to keep routing density high.

Trace Width

You can determine the required trace width in a number of ways. First, for impedance controlled routing, you'll need one of the following tools:

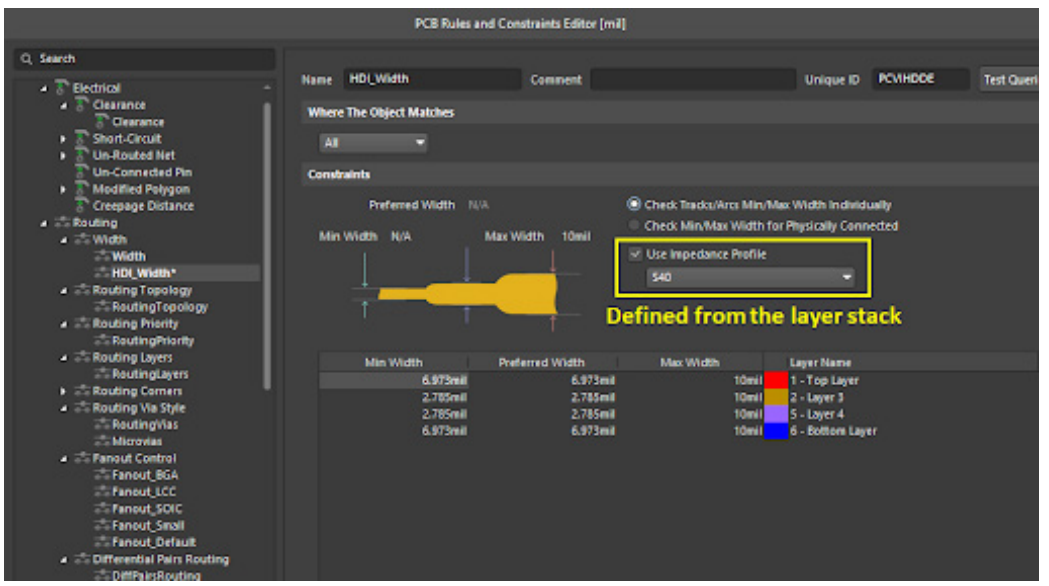
- A pen and paper to calculate the required trace size (the hard way)
- An online calculator (the quick way)
- A field solver integrated in your design and layout tools (the most accurate way)

I've discussed the drawbacks of using an online calculator for trace impedance calculations in a different article, and the same points apply when sizing traces for an HDI PCB layout.

To set up the trace width, you can define it as a constraint in your design rules editor, just like you would with via sizes. If you're not worried about impedance control, you can set whatever width you like. Otherwise, you need to determine an impedance profile for your PCB stackup and enter this specific width as a design rule.

There is a careful balancing act you'll need to play as the trace width can't be too large for your via landing pad size. If the impedance controlled trace width is too large, you should decrease the laminate thickness as this will force the trace width to decrease, or you can increase the landing pad size. As long as the landing pad size exceeds the value listed in the IPC standards, you'll be fine from a reliability standpoint.

Once you've determined the width you need for impedance control, just set this value as a design rule. In Altium Designer, you can use the integrated field solver to define an impedance profile, which can then be used to enforce a required width in your design rules.



Setting microvia design rules for HDI routing with stripline traces.

Clearances

Once you've done the two critical tasks shown above, you need to determine the appropriate trace clearance. Unfortunately, you shouldn't default to a 3W or 3H rule of thumb for spacing between traces as these rules are incorrectly applied to advanced boards with very high speed signals. Instead, it's better to run a crosstalk simulation for a proposed trace width and check whether this will produce excessive crosstalk.

Import From Schematic and Share on Altium 365

Once you've finished setting up your design rules, routing constraints, PCB layer stack, and via styles, you're ready to capture your schematics as an initial layout. If you're working with a remote team and you need to collaborate on an HDI PCB layout, you can share your new layout in your Altium 365 Workspace. Your collaborators will be able to edit the layout within Altium Designer, and your team can collaborate with your fabricator to ensure your board can be produced at scale. You'll also have access to a complete set of version control features, user access management tools, and component repository.

The design rules and constraints shown here can be easily applied to an HDI PCB layout thanks to the rules-driven design engine in Altium Designer®. Once you're ready to start your PCB layout, you can use Altium Designer and the Altium 365® to create a productive workflow for your remote PCB design team.

We have only scratched the surface of what is possible to do with Altium Designer on Altium 365. You can check the product page for a more in-depth feature description or one of the On-Demand Webinars.