REV STATUS OF SHEETS										
REV	-	-	-	-	-	-	-	-	-	-
SHEET	-	-	-	-	-	-	-	-	-	-

DWG NO: =DOC_NO_ASSY_DWG REV: .Ite

REVISIONS

ZONE	REV	DESCRIPTION	DATE	APPROVED
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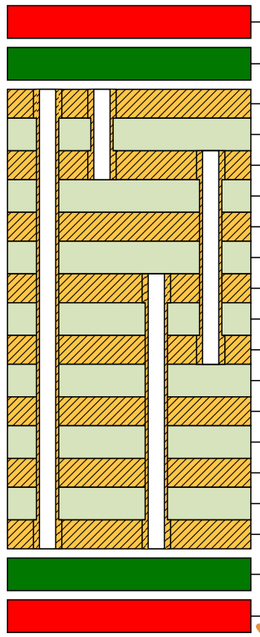
--	-	-----	--/--/--	-. -----
--	-	-----	--/--/--	-. -----
--	-	-----	--/--/--	-. -----

General Description

Company name	
Name/Part Number	PC4-SODIMM_V200_RC_A1_20141015
Number of boards	1
Board length	1182.10 mil
Board width	2741.16 mil
Number of layers	8
Board thickness	48.04 mil
Total number of holes	787
Total number of slots	0
Square holes	0
Surface Finish	ENIG
Solder Mask	LPI
Solder Mask color	Green
Legend	White
Minimum hole/pad diameter	7.87 mil
Minimum clearance/track	5 mil
Milled cutouts (yes/no)	no
Contour processing (milling/V-cut)	yes
Electrical testing (required/not required)	yes
Impedance control	yes

Layer Stack Legend



Material	Layer	Thickness	Dielectric Material	Type	Gerber
	Top Overlay			Legend	GTO
Surface Material	Top Solder	0.39mil	Solder Resist	Solder Mask	GTS
Copper	TOP	1.77mil		Signal	GTL
Core		*2.76mil*	*FR-4*	*Dielectric*	
Copper	SPLIT2	0.59mil		Signal	G1
Core		*3.15mil*	*FR-4*	*Dielectric*	
Copper	S3	0.59mil		Signal	G2
Core		*12.60mil*	*FR-4*	*Dielectric*	
Copper	VDD4	0.59mil		Signal	G3
Core		*3.15mil*	*FR-4*	*Dielectric*	
Copper	S5	0.59mil		Signal	G4
Core		*12.60mil*	*FR-4*	*Dielectric*	
Copper	S6	0.59mil		Signal	G5
Core		*3.15mil*	*FR-4*	*Dielectric*	
Copper	SPLIT7	0.59mil		Signal	G6
Core		*2.76mil*	*FR-4*	*Dielectric*	
Copper	BOTTOM	1.77mil		Signal	GBL
Surface Material	Bottom Solder	0.39mil	Solder Resist	Solder Mask	GBS
	Bottom Overlay			Legend	GBO

Total thickness: 48.04mil

Impedance Table

Transmission Line	Target Impedance	Trace layer	Wide Trace Width	Narrow Trace Width	Reference layers	Target Tolerance
Coated Microstrip	44	TOP	5.47mil	5.47mil	SPLIT2	10%
Offset Stripline	44	SPLIT2	2.93mil	2.93mil	TOP,S3	10%
Offset Stripline	44	S3	5.06mil	5.06mil	SPLIT2,VDD4	10%
Offset Stripline	44	VDD4	5.06mil	5.06mil	S3,S5	10%
Offset Stripline	44	S5	5.06mil	5.06mil	VDD4,S6	10%
Offset Stripline	44	S6	5.06mil	5.06mil	S5,SPLIT7	10%
Offset Stripline	44	SPLIT7	2.93mil	2.93mil	S6,BOTTOM	10%
Coated Microstrip	44	BOTTOM	5.47mil	5.47mil	SPLIT7	10%

Notes:

1. Title block with parameters from the PCB Project and Draftsman document.
2. A table with a description of the PCB.
3. Layer stack table that includes all information needed for board construction.
4. Impedance table with trace width values, layer information, and tolerances.
5. Drill drawing
6. Detailed drill table with hole sizes and tolerances.
7. Fabrication notes
8. Layer drawing that matches Gerber data generated from the PCB layout.

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PART NO: =PCB_PART_NUMBER

APPROVALS	DATE
ENGINEER: =PCB_ENGINEER	=PCB_ENGINEE
DESIGNER: =PCB_DESIGNER	=PCB_DESIGNE
CHECKER: =PCB_CHECKER	=PCB_CHECKE

Reference Documents

BOM DOC: =DOC_NO_BOM
ASSY DOC: =DOC_NO_FAB_DWG
SCH DOC: =DOC_NO_SCH_DWG
PCB DOC: =PCB_DWG_NO

THIRD ANGLE PROJECTION

NEXT ASSY | USED ON
APPLICATION

Altium™

=Address1
=Address2
=Address3
=Address4

DESIGN ITEM: .Item
DESIGN ITEM REVISION: .ItemRevision

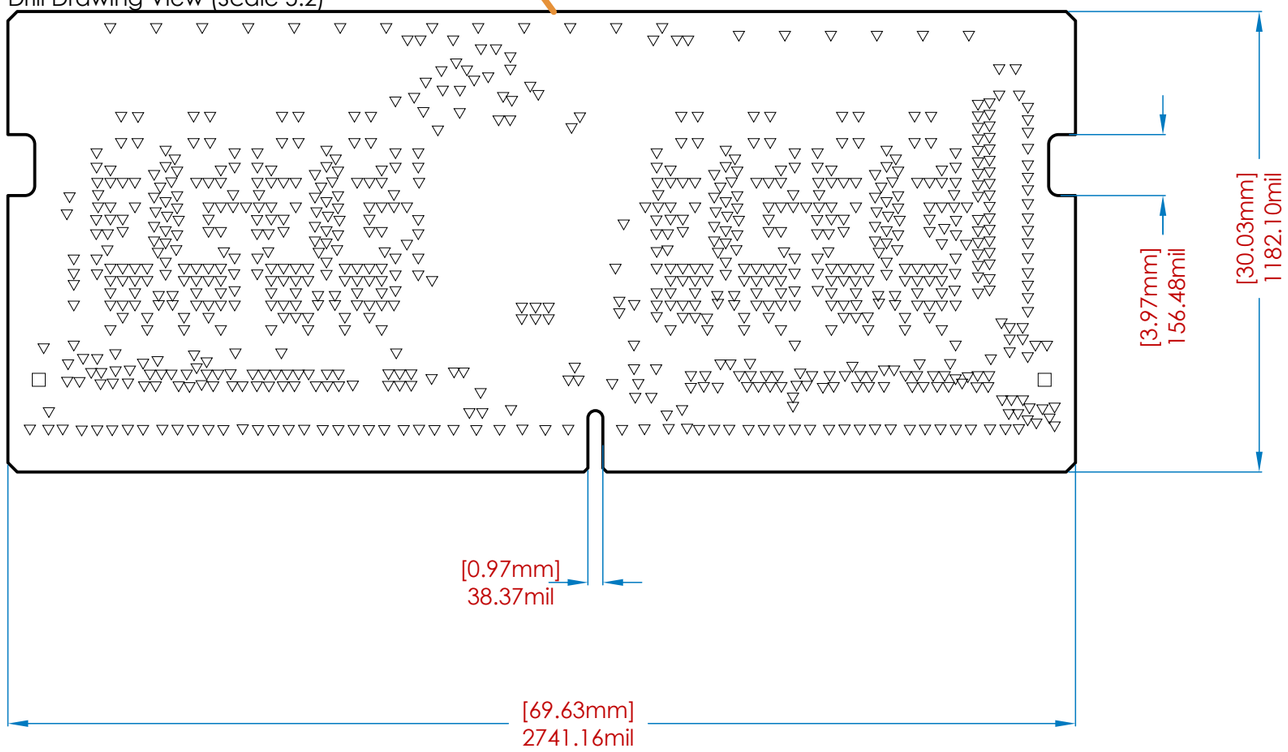
TITLE: =PCB_TITLE_1 =PCB_TITLE_2

SIZE: A3 | CAGE CODE: =CAGE_CO | DWG NO: =DOC_NO_FAB_DWG | REV:

SCALE: | FILE NAME: | SHEET: 1 OF 3

DWG NO: =DOC_NO_ASSY_ REV: .Ite

Drill Drawing View (Scale 5:2)



Drill Table

Symbol	Count	Hole Size	Plated	Hole Tolerance
▽	785	7.87mil	Plated	+0.00mil/-3.00mil
□	2	70.87mil	Non-Plated	+/-1.00mil
	787 Total			

NOTES: UNLESS OTHERWISE SPECIFIED.

1. FABRICATE PER IPC-6012A CLASS 2.
2. FOR BOARD THICKNESS AND IMPEDANCE DETAILS REFER STACKUP DOCUMENT.
3. PRINTED WIRING BOARD SHALL COMPLY WITH REQUIREMENTS OF ANSI/J-STD-003.
4. SURFACE FINISH: ENIG
5. SOLDERMASK ON BOTH SIDES OF THE BOARD SHALL BE LPI, COLOR GREEN.
6. SILK SCREEN LEGEND TO BE APPLIED PER LAYER STACKUP USING WHITE NON-CONDUCTIVE EPOXY INK.
7. THIS PRINTED WIRING BOARD IS DESIGNED WITH A MINIMUM CONDUCTOR WIDTH AND SPACING OF 4 MIL & 4 MILS.
8. ALL VIAS ARE TENTED ON BOTH SIDES UNLESS SOLDERMASK OPENED IN GERBER.
9. ALL VIAS ON PAD SHOULD BE FILLED WITH NON CONDUCTIVE EPOXY AND SURFACE SHOULD BE FLAT. FLATNESS TOLERANCE FOR VIA ON PADS: +0.000 /- 0.001 INCHES ON BOTH SIDES. THE MANUFACTURER IS REQUESTED TO SIZE PER THEIR SOLDERMASK TOLERANCE.
10. SOLDER MASK OPENING IS KEPT SAME SIZE AS PAD (1:1) FOR ALL COMPONENTS
11. VENDOR SHOULD FOLLOW ROHS COMPLIANT PROCESS AND Pb FREE FOR MANUFACTURING
12. MANUFACTURER'S IDENTIFICATION, DATECODE LETTER SHALL BE SILKSCREENED ON SOLDER SIDE OF THE BOARD.
13. TRACE WIDTH SHOULD BE ACCURATELY ETCHED. MAX TOLERANCE +/- 1 MIL
14. ALL DIMENSIONS ARE IN INCHES UNLESS OTHERWISE SPECIFIED.
15. FLATNESS REQUIREMENTS:
A. BOW AND TWIST OF ASSEMBLY SUB-PANEL OR SINGULATED PWB SHALL NOT EXCEED 0.7% OF LONGEST SIDE
B. TEST IN ACCORDANCE WITH THE CURRENT REVISION OF IPC-TM-650 2.4.22
16. PCB MATERIAL REQUIREMENTS:
A. FLAMMABILITY RATING MUST MEET OR EXCEED UL94V-0 REQUIREMENTS. PCB MUST BEAR THE UL94V-0 REGISTERED MATERIAL ID NUMBER.
B. Tg 170 CELSIUS OR EQUIVALENT.
C. EQUIVALENT MATERIAL SHALL BE RoHS COMPLIANT, HALOGEN FREE AND APPROVED BY CUSTOMER.
17. LAYER TO LAYER REGISTRATION SHALL BE WITHIN +/-2 MIL
18. IMPEDANCE CONTROL REQUIREMENTS: VENDOR MAY ADJUST DESIGN GEOMETRIES UP TO +/-20% TO ACHIEVE TARGET IMPEDANCE. ADJUSTMENTS BEYOND 20% OF LINE WIDTH, SPACING OR DIELECTRIC THICKNESS SHALL REQUIRE APPROVAL FROM CUSTOMER.

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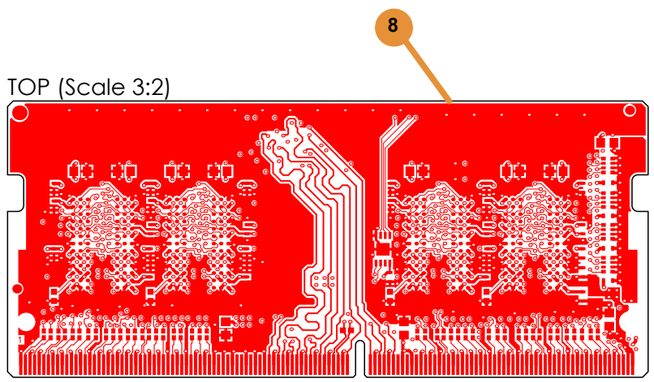
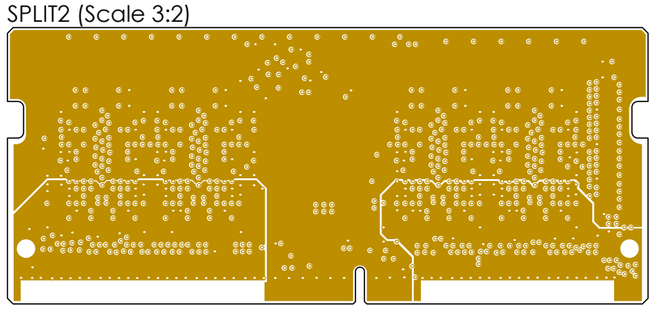
SIZE:	CAGE CODE:	DWG NO:	REV:
A3	=CAGE_CO	=DOC_NO_FAB_DWG	
SCALE:	FILE NAME:	SHEET: 2 OF 3	

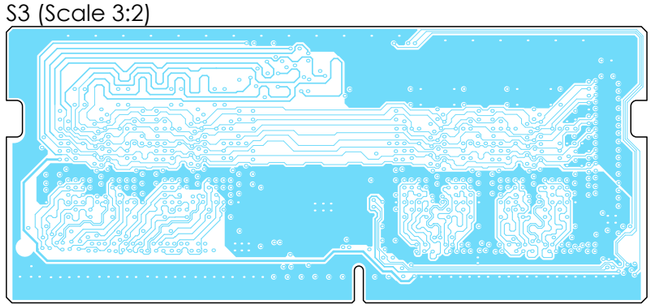
TOP (Scale 3:2)



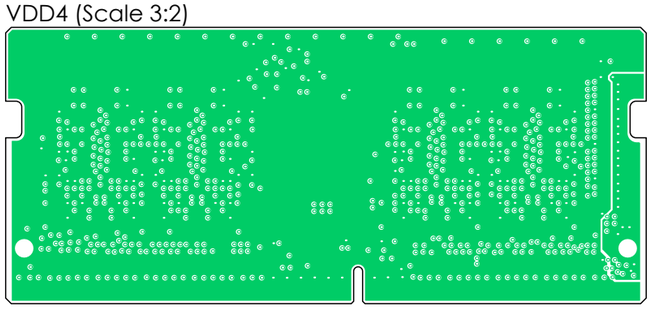
SPLIT2 (Scale 3:2)



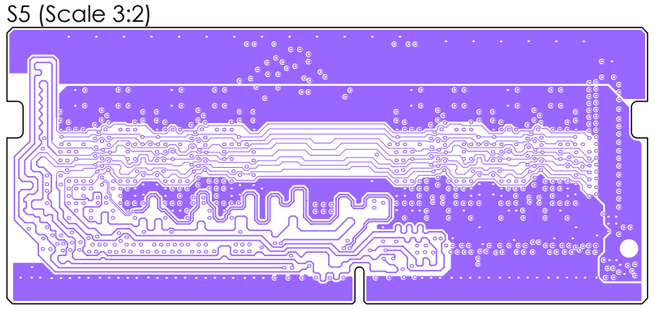
S3 (Scale 3:2)



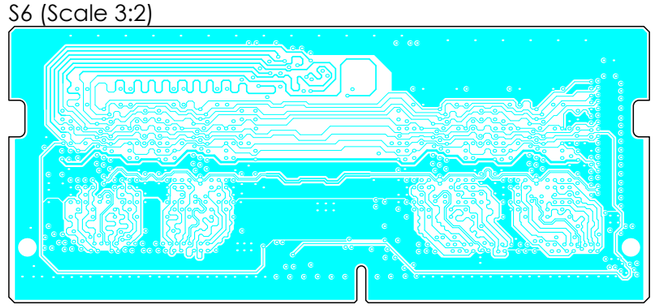
VDD4 (Scale 3:2)



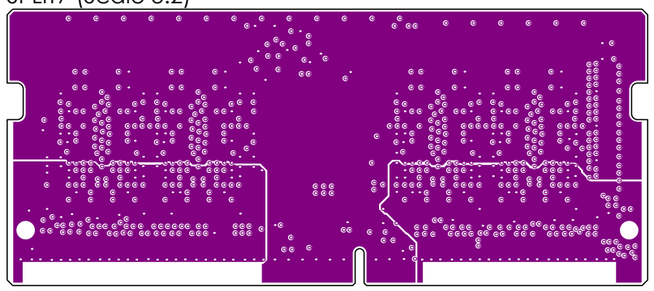
S5 (Scale 3:2)



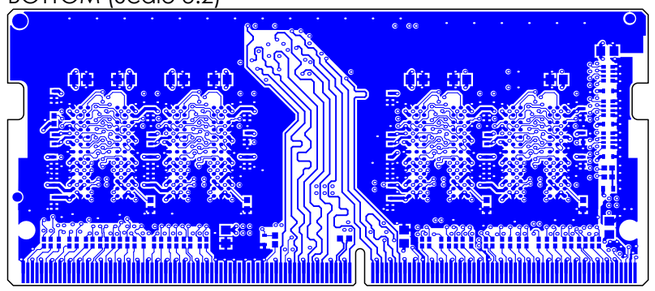
S6 (Scale 3:2)



SPLIT7 (Scale 3:2)



BOTTOM (Scale 3:2)



SIZE:	CAGE CODE:	DWG NO:	REV:
A3	=CAGE_CO	PC4-	
SCALE:	FILE NAME:	SHEET: 3 OF 3	

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DWG NO =DOC_NO_ASSY_ REV .lte