

Altium[®]

QUICK GUIDE

Constraint Manager



Introduction

The Constraint Manager in Altium Designer is a powerful tool that simplifies and streamlines the complex task of PCB design. Central to this is a unified table-based editor that consolidates all your design rules and constraints, whether they are electrical or physical in nature. This brings everything into one place, saving you the time and effort of navigating through multiple menus and settings.

One of the significant advances offered by this feature is the unified access to nets, classes, and rules, both from the schematic level and the PCB editor. Now, with this integrated approach, designers can effortlessly input and modify constraints at both the schematic and layout levels, which enhances workflow and ensures design cohesiveness.

The Constraint Manager also allows you to redefine rules flexibly, meeting the shifting requirements of your design as it evolves. Added to this is the Class-to-Class Clearance Matrix, an intuitive interface that helps you specify clearances between various component classes, thereby aiding in compliance with industry standards.

Overall, the Constraint Manager is a key enhancement in Altium Designer. It not only makes rule and constraint management simpler but also significantly improves your design workflow by integrating rule management across different stages of the design process.

Benefits of the Altium Designer Constraint Manager



Unified Access to Constraints

With the Constraint Manager, you can access and modify design rules and constraints from both the schematic and PCB editor. This reduces the time spent toggling between different design stages, improving your overall workflow.



Table-Based Editor

The feature offers a table-based editor that brings all your design rules and constraints into one place. This centralized location aids in quick rule verification and modification, reducing the chances of design errors.



Class-to-Class Clearance Matrix

This tool allows you to specify clearances between different classes of components through an intuitive interface. This helps in meeting compliance requirements with ease, thereby improving the reliability of the final product.



Redefinable Constraints

The ability to easily redefine rules gives you the flexibility to adjust to the changing requirements of your design project. This ensures that your design stays aligned with both technical and business goals, without having to rework your constraints from scratch.



Physical and Electrical Constraints

The Constraint Manager allows you to set both electrical and physical constraints within the same framework. This enables a more holistic approach to design, ensuring that all aspects, from signal integrity to mechanical fit, are accounted for.



Improved Productivity

The feature's unified and table-based approach allows for easier and quicker constraint management. This leads to improved productivity as designers spend less time managing constraints and more time on actual design work.



Streamlined Workflow

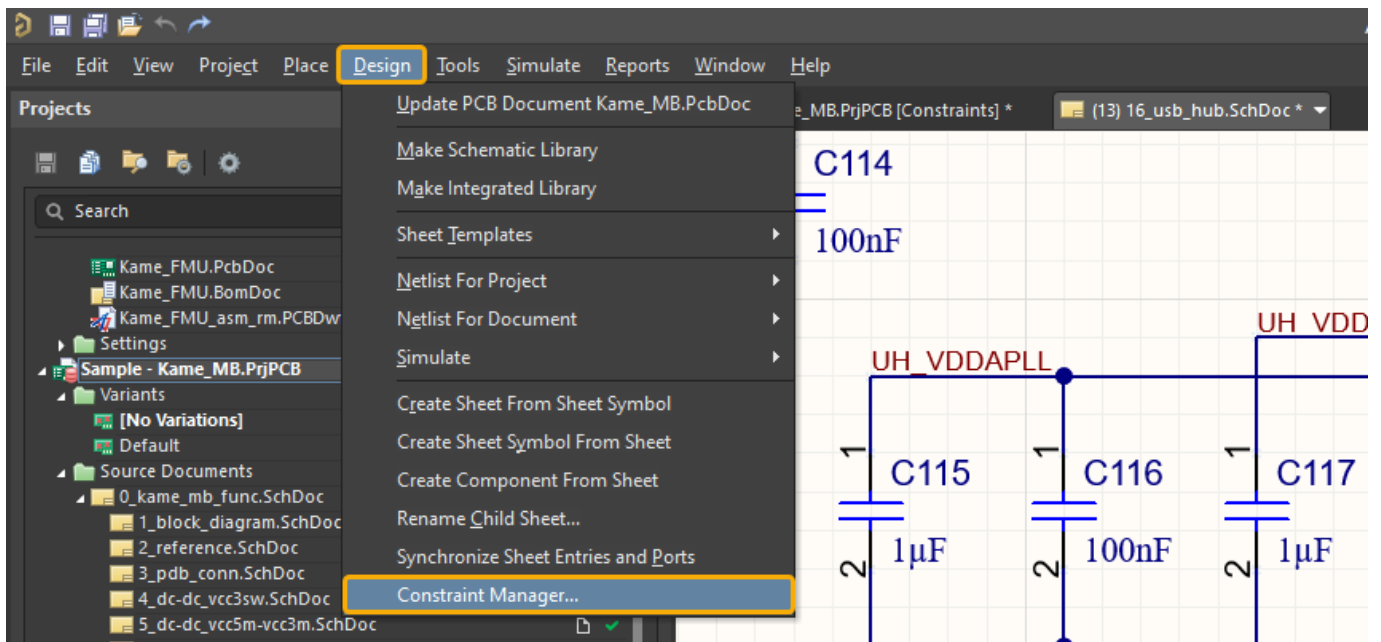
The feature's ability to manage constraints from both schematic and PCB design stages in one place streamlines the design process. This results in a faster time-to-market for the product.

Constraint Manager Use Case

Constraint Manager simplifies the PCB design process by letting you manage all your design rules in one place. It connects the schematic and PCB layout, making sure that what you plan is what you get. This makes it easier to communicate design intent and ensures that your board is made right the first time.

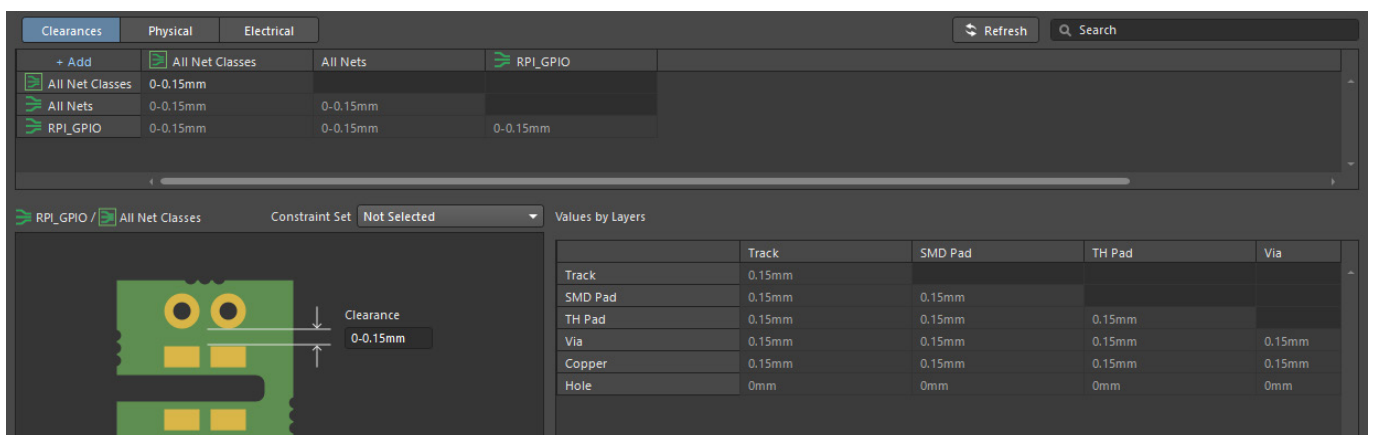
Here is one example that illustrates the capabilities of Constraint Manager in a real-world application:

1. Starting in the schematic editor, go to **Design** and open **Constraint Manager**



2. After opening the **Constraint Manager document**, we can easily manage rules for all nets in the project. The interface, accessible from the schematic editor, is divided into three tabs:

2.1. Clearances for defining minimum distances between Net Classes,



2.2. Physical for setting physical constraints such as Track Width, Differential Pairs details, Clearance, Via Style, and Polygon Connects,

The screenshot shows the 'Physical' tab in the Constraint Manager. The main table lists constraints for various signal types. The 'CAN' constraint is highlighted, showing a preferred width of 0.1mm and a preferred diff pair gap of 0.4mm. Below the table, a detailed view for the 'CAN' constraint is shown, including a diagram of a differential pair with a 'Max Uncoupled Length' of 12.7mm. The diagram shows two parallel tracks with a central via, and arrows indicating the uncoupled length. The 'Values by Layers' table on the right shows the constraint values for the top and bottom layers.

Scope	Constraint Set	Min Width	Preferred Width	Preferred Diff Pair Gap	Clearance	Via Style
All Nets		0.1mm	0.125mm	0.254mm	0.12mm	1.27mm, 0.7112mm
All Differential Pairs		0.1mm	0.381mm	0.254mm	0.12mm	1.27mm, 0.7112mm
CAN		0.1mm	0.1mm	0.4mm	0.12mm	1.27mm, 0.7112mm
CSI		0.1mm	0.1mm	0.13mm	0.12mm	1.27mm, 0.7112mm
@BMC_USB_D		0.1mm	0.381mm	0.254mm	0.12mm	1.27mm, 0.7112mm
@EXP1_USB_D		0.1mm	0.381mm	0.254mm	0.12mm	1.27mm, 0.7112mm
@USBA1_D		0.1mm	0.381mm	0.254mm	0.12mm	1.27mm, 0.7112mm
@USBA2_D		0.1mm	0.381mm	0.254mm	0.12mm	1.27mm, 0.7112mm

Min Width	Min Gap	Preferred	Preferred	Max Width	Max Gap	Layer
0.1mm	0.254mm	0.1mm	0.4mm	0.7mm	0.7mm	[1] Top
0.1mm	0.254mm	0.1mm	0.4mm	0.7mm	0.7mm	[2] Bott

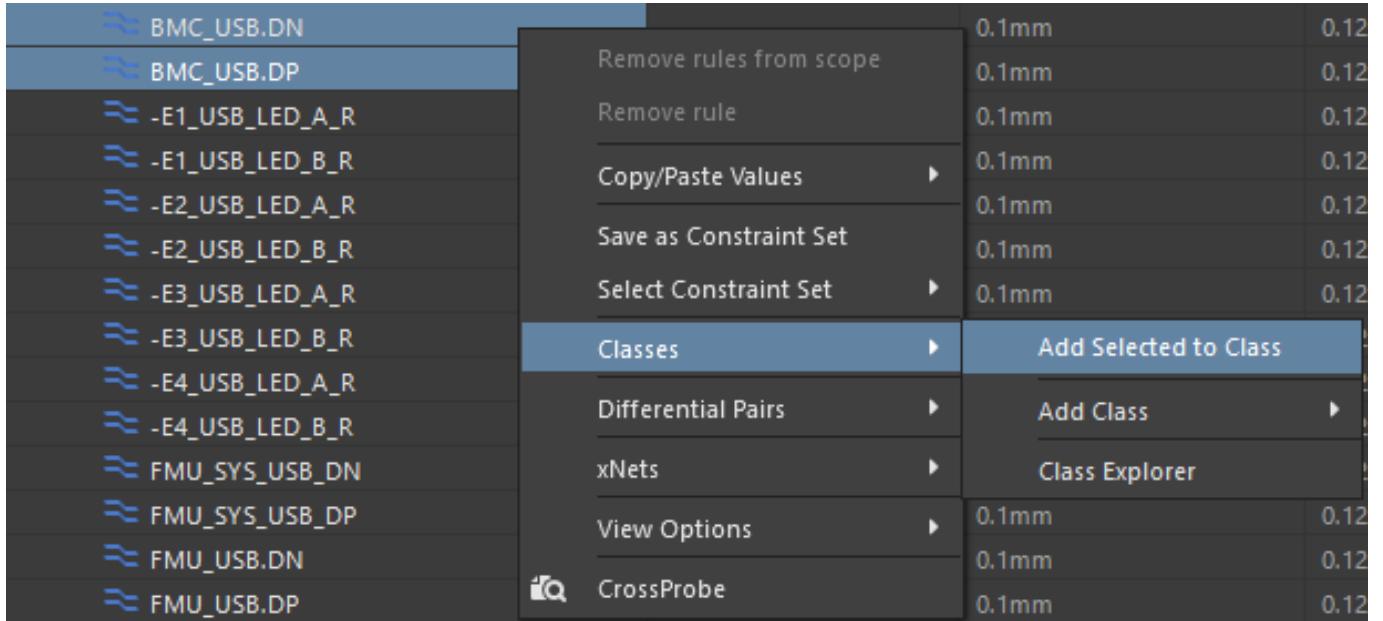
2.3. Electrical for specifying electrical constraints like Topology, Impedance, Maximum Via Count, Min/Max Total Length, Max Stub Length, and Max Via Stub Length.

The screenshot shows the 'Electrical' tab in the Constraint Manager. The main table lists constraints for various signal types. The '5-19.M_ON' constraint is highlighted, showing a topology of 'Shortest'. Below the table, a detailed view for the '5-19.M_ON' constraint is shown, including a diagram of a network topology with nodes and connections. The diagram shows a network of nodes connected by lines, with a 'Shortest' topology constraint. The 'Values are inherited from All Nets Net Class' is noted at the bottom.

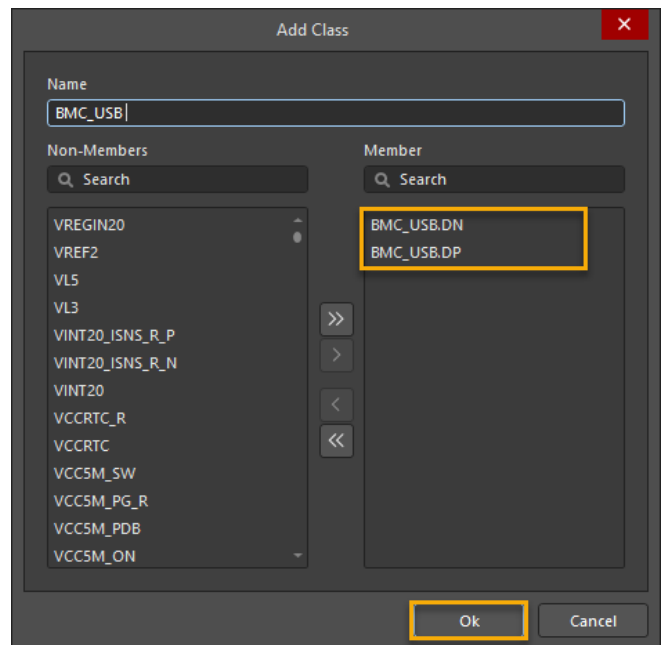
Scope	Constraint Set	Topology	Impedance	All Layer Sets	Maximum Via Count	Min / Max Tc
All Nets		Shortest		All Layers		
All xNets		Shortest		All Layers		
3-18Port		Shortest		All Layers		
5-19		Shortest		All Layers		
5-19.M_ON		Shortest		All Layers		
5-19.MPWR_ON		Shortest		All Layers		
5-19.VCC3M_PG		Shortest		All Layers		
5-19.VCC5M_PG		Shortest		All Layers		
7-9		Shortest		All Layers		
18-20		Shortest		All Layers		

3. All **Nets** can be easily grouped into classes, differential pairs or xNets. To do this, you should select the nets you want to add to group , and then **right-click** then choose the desired type:

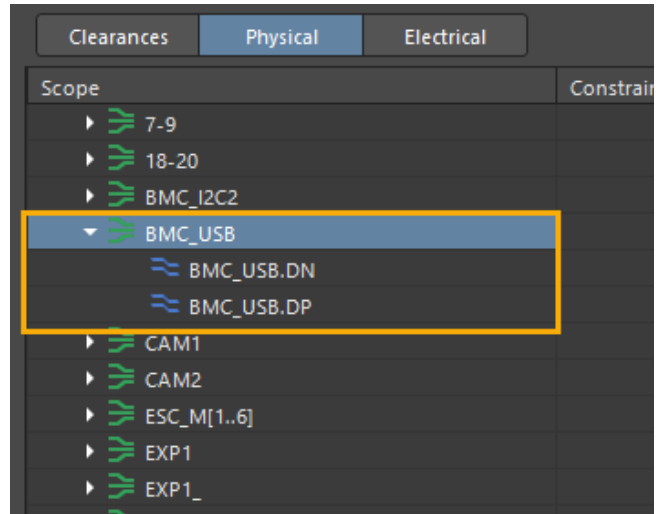
3.1. Classes



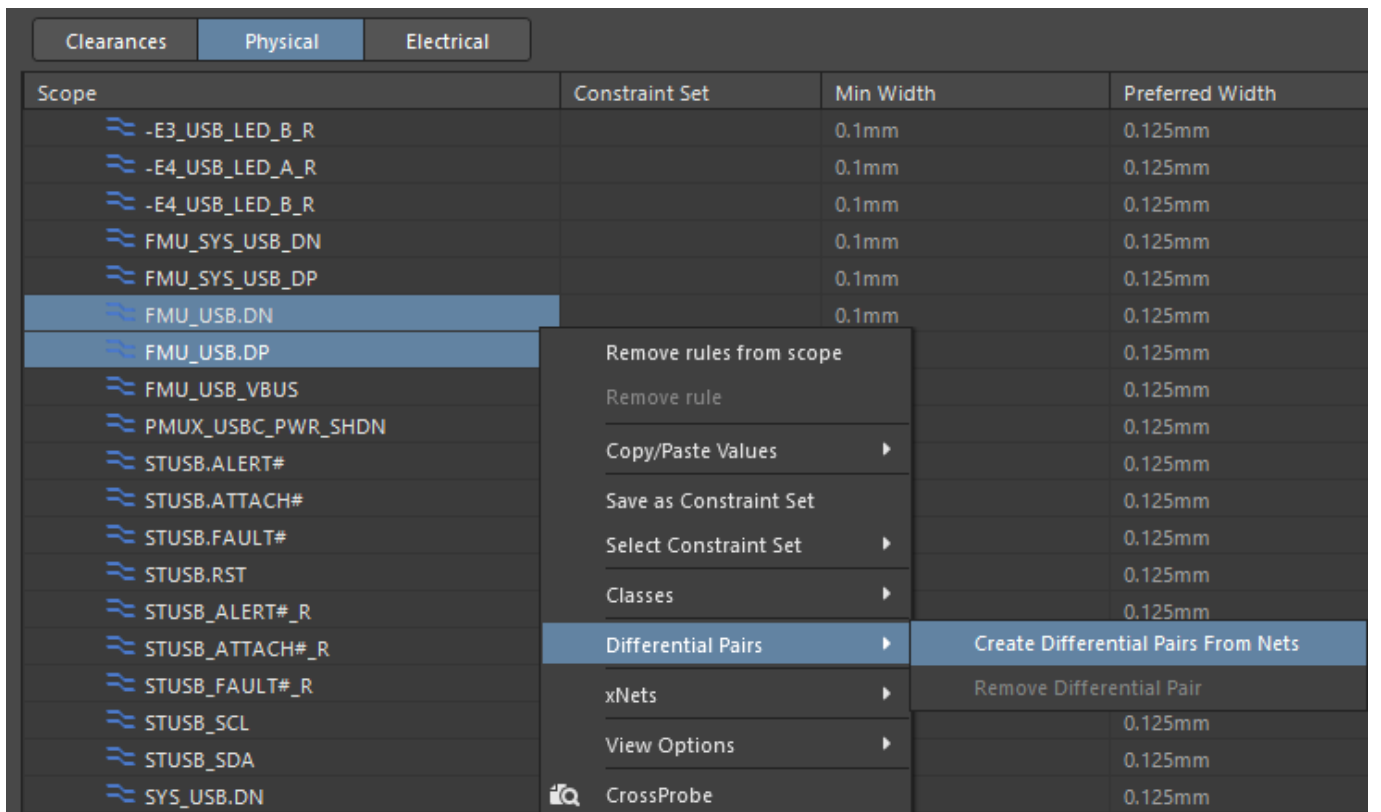
Then, in the appearing window, you can name the new class, add '>>' or remove '<<' signals to a member of the class. After setting all options, click 'OK'.



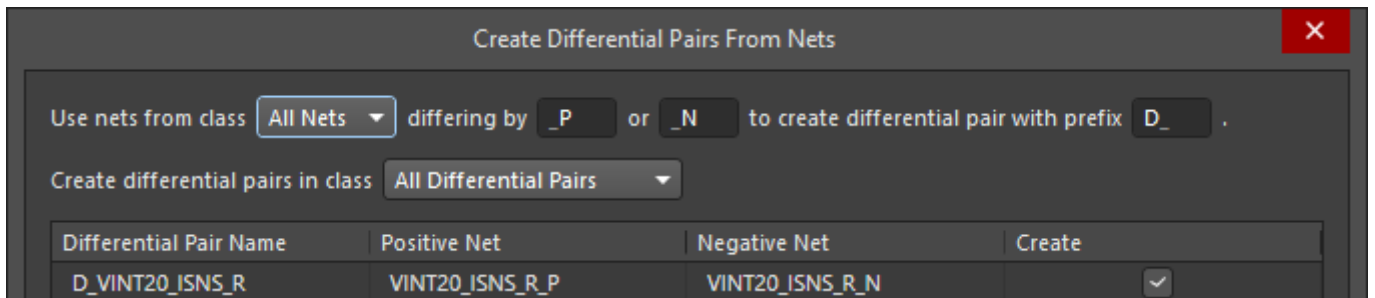
The newly created **Class** will immediately appear in the tabs.



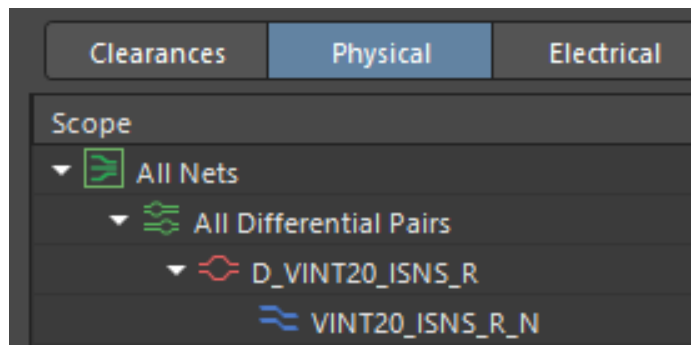
3.2. Differential Pairs



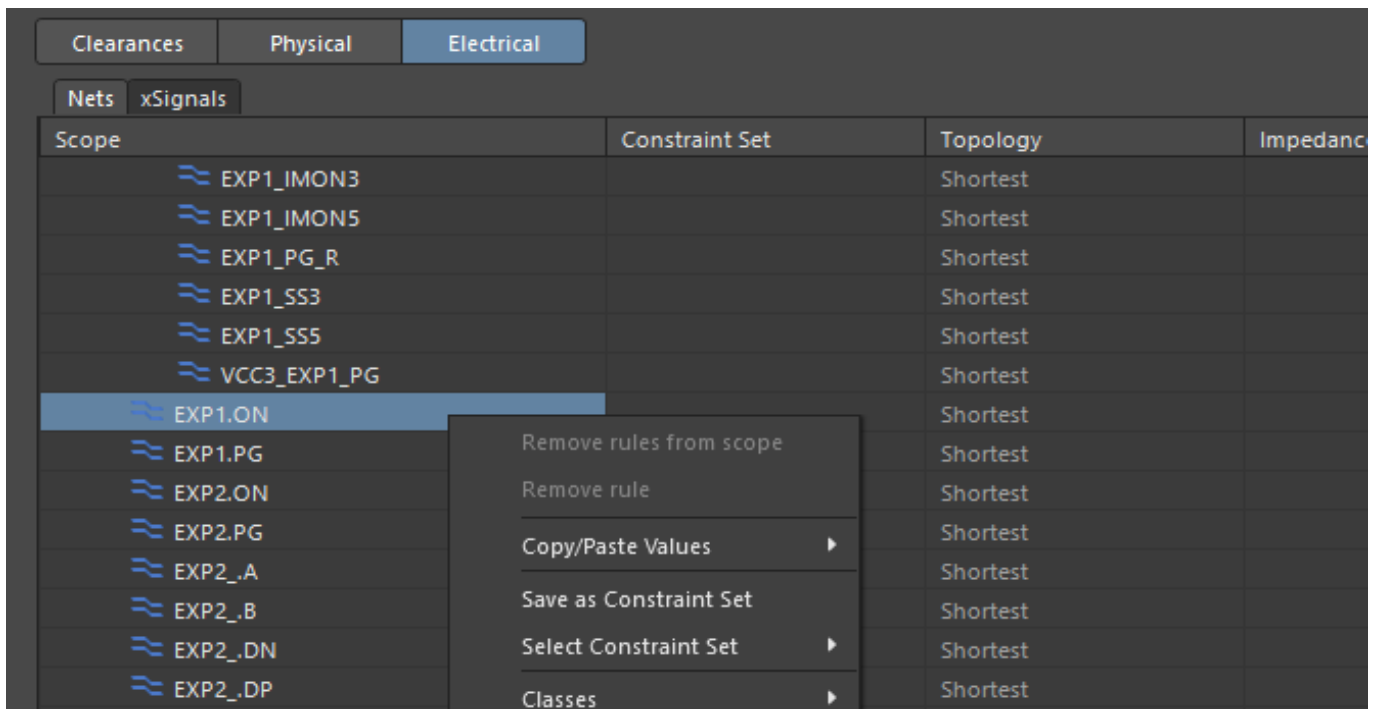
either change or leave the **differentiating suffixes** (_P and N) and the **prefix** (D_) that will be used to create the differential Pair Name. After making your selections, click 'Execute'.



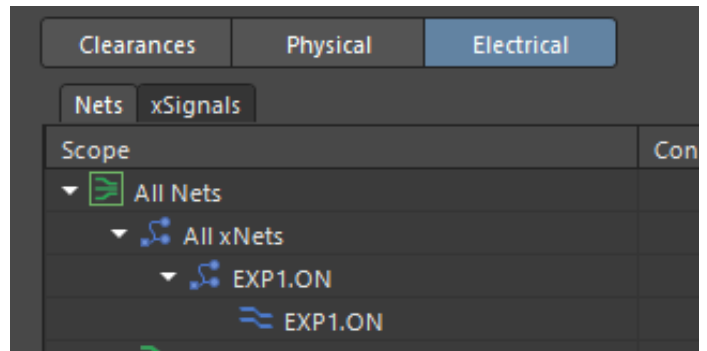
The newly created **Differential Pair** will immediately appear in the tabs.



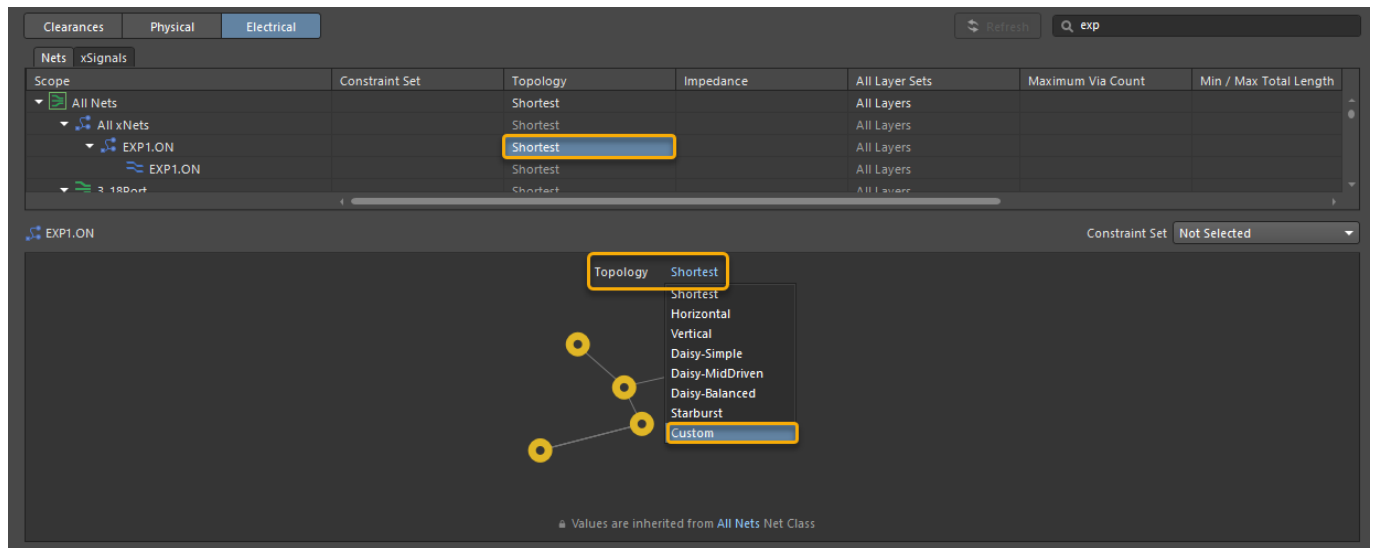
3.3. xNets



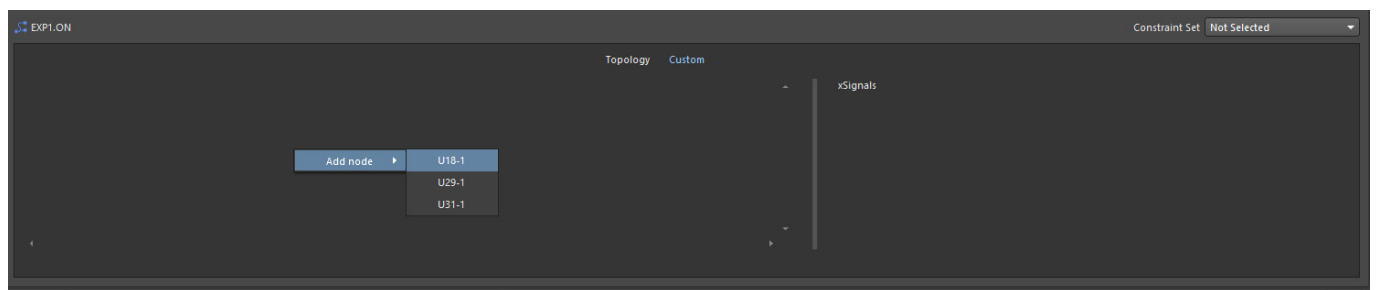
The newly created **xNet** will immediately appear in the tabs.



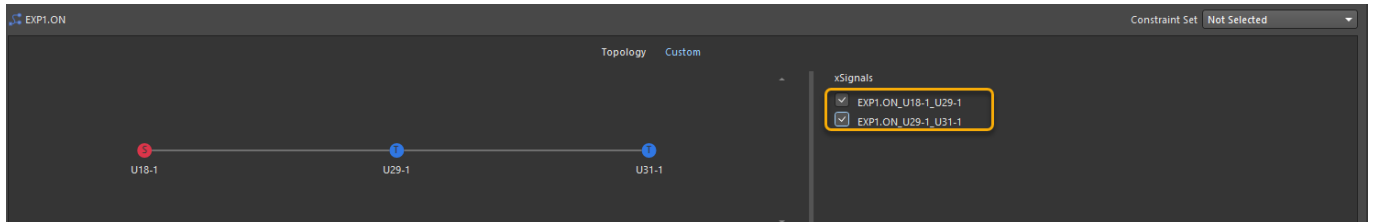
4. In the added **xNets**, you can set individual **xSignal** rules. To do it go to the **'Topology'** column. In the bottom panel, then near the topology menu, select **'Custom'** from the dropdown list



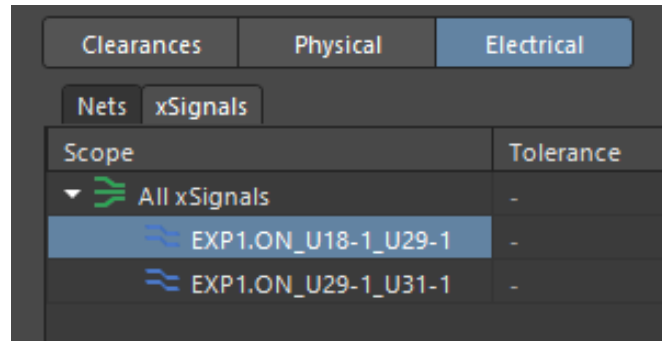
Then, in the topology window, add all the nodes by **right-click** at empty window then **Add node** then add all nodes.



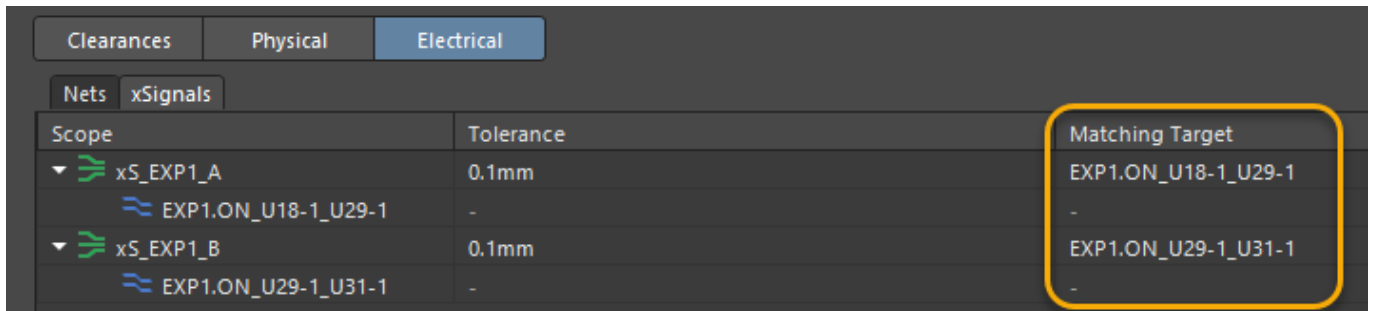
Next, check the checkbox for the xSignal you want to define.



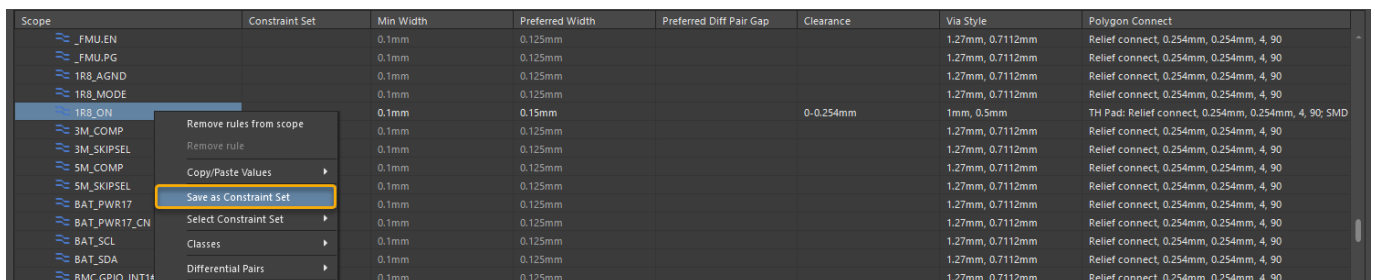
Now, in the xSignal sub-tab, the previously selected pairs will appear.

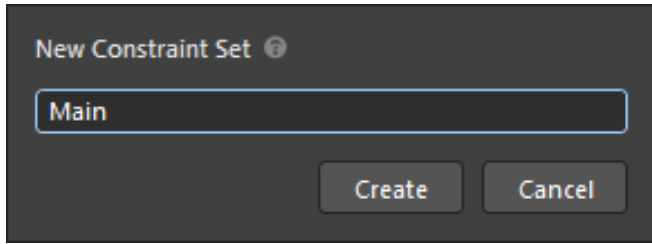


To define length **Tolerances** and **Marching Target**, each xSignal should be added to the class.



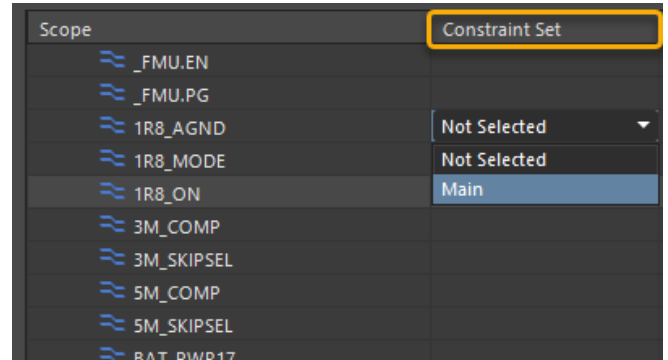
- The new feature is the ease of defining a **Constraint Set**, which is a defined set of parameters that we can later conveniently assign to nets or classes. To define such a Set, **right-click** on the row of rules you desire, then choose the option **Save as Constraint Set**.



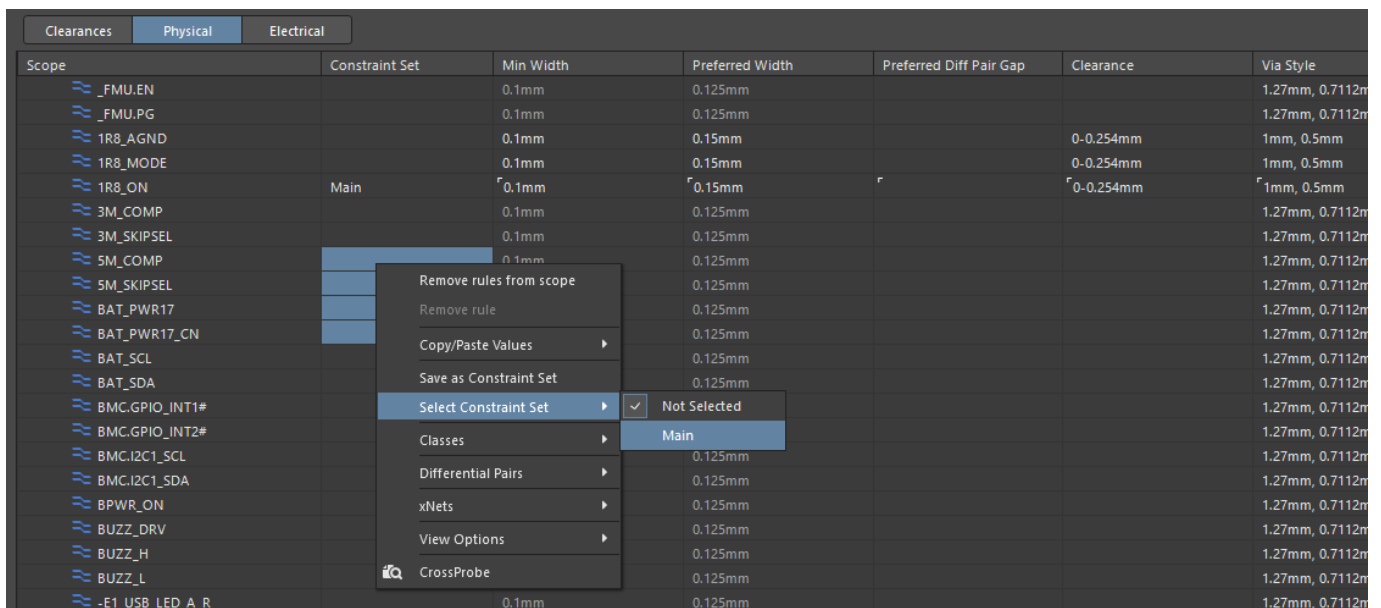


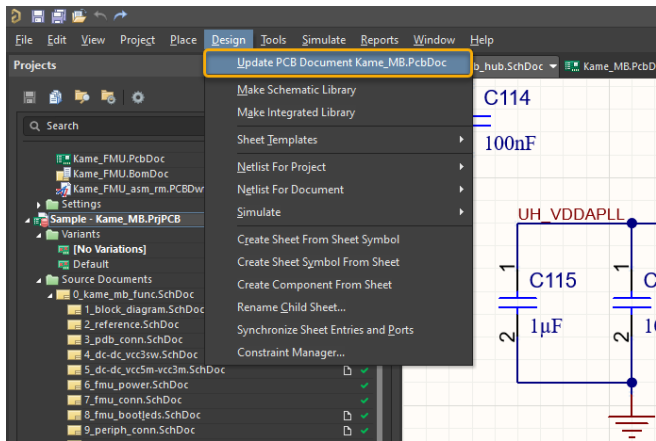
6. In the appearing window, you should enter the desired name of the constraint set.

7. Now, we can assign our constraint set to any class or net by clicking on the cell in the **Constraint Set** column and selecting our set from the **dropdown list**.



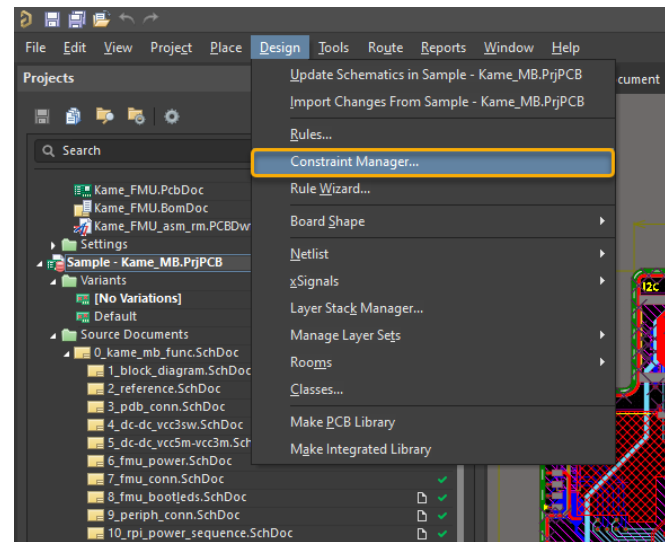
or select more than one and **right-click>Select Constraint Set>'Constraint Set Name'**





8. After finishing the editing in the Constraint Manager, you need to transmit all the information to the PCB by selecting the command **Design > Update PCB Document**.

9. In the PCB editor, similarly to the Schematic, you can access the Constraint Manager by selecting **Design > Constraint Manager**.



10. The Constraint Manager, accessible from the PCB level, is also divided into tabs. However, in addition to the **Clearances**, **Physical** and **Electrical** tabs available in the schematic, in the PCB there is also an **All Rules** tab, which is a compilation of all rules and is inspired by the old version of the Rules Manager.

Scope	Constraint Set	Topology	Impedance	All Layer Sets	Maximum
All Nets		Shortest		All Layers	
FMU		Shortest		All Layers	
FMU.EN		Shortest		All Layers	
FMU.PG		Shortest		All Layers	
3-18Port		Shortest		All Layers	
3-18Port.BMC_GPIO_B3		Shortest		All Layers	
3-18Port.BMC_GPIO_B5		Shortest		All Layers	
3-18Port.BMC_I2C3_SCL		Shortest		All Layers	
3-18Port.BMC_I2C3_SDA		Shortest		All Layers	
3-18Port.BMC_I2C4_SCL		Shortest		All Layers	
3-18Port.BMC_I2C4_SDA		Shortest		All Layers	
3-18Port.ESC_EN		Shortest		All Layers	
3-18Port.ESC_PG		Shortest		All Layers	
5-19		Shortest		All Layers	
5-19.M_ON		Shortest		All Layers	
5-19.MPWR_ON		Shortest		All Layers	
5-19.VCC3M_PG		Shortest		All Layers	
5-19.VCC5M_PG		Shortest		All Layers	
7-9		Shortest		All Layers	
7-9.FMU_BUZZ		Shortest		All Layers	

All rules:

Rule Class	Priority	Name	Object Match	Second Object Match	Minimum
Electrical (16)					
Short-Circuit (1)					
Un-Routed Net (1)					
Un-Connected Pin (0)					
Modified Polygon (1)					
Creepage (0)					
High Speed					
Parallel Segment (0)					
Length (0)					
Matched Lengths (2)					
Stub Length (0)					
Vias under SMD (0)					
Via Count (0)					
Back Drilling (0)					
Return Path (0)					
Routing					
Width (2)					
Routing Topology (2)					
Routing Priority (1)					
Routing Layers (2)					
Routing Corners (1)					
Routing Via Style (552)					
Fanout Control (5)					
Differential Pairs Routing (7)					
Plane					
Power Plane Connect Style (3)					
Power Plane Clearance (2)					
Advanced Rules	1	Outline/NPTH clearance	(IsThruPin and (PadsPlated = 'False')) or IsBoardCutoutRegion or IsBoardOutline	All	0.25mm
	2	L5 clearance	OnLayer(L5)	All	0.15-0.2mm
	3	Polygon clearance 18um	InPolygon and (OnLayer(Top) or OnLayer(Bottom) or OnLayer(L3) or OnLayer(L6))	All	0.15-0.2mm
	4	Polygon clearance 35um	InPolygon and OnLayer(L5)	All	0.2mm
	5	CSI via clearance	InDifferentialPairClass(CSI) and IsVia	InDifferentialPairClass(CSI) and IsVia	0.15mm
	6	USB via clearance	InDifferentialPairClass(USB) and IsVia	InDifferentialPairClass(USB) and IsVia	0.1mm
	7	CAN via clearance	InDifferentialPairClass(CAN) and IsVia	InDifferentialPairClass(CAN) and IsVia	0.7mm
	8	CSI clearance	InDifferentialPairClass(CSI)	All	0.6mm
	9	USB clearance	InDifferentialPairClass(USB)	All	0.5mm
	10	CAN clearance	InDifferentialPairClass(CAN)	All	0.7mm
	11	Top clearance	OnLayer(Top)	OnLayer(Top)	0.1mm
	12	GND1 clearance	OnLayer(GND1)	All	0.2mm
	13	Power clearance	OnLayer(Power)	All	0.15mm
	14	GND2 clearance	OnLayer(GND2)	All	0.2mm
	15	Bottom clearance	OnLayer(Bottom)	OnLayer(Bottom)	0.1mm
	16	Clearances Matrix	Matrix	Matrix	0-0.7mm

Conclusions

Centralized Rule Management: Constraint Manager serves as a one-stop hub for rule definition and management, streamlining the design workflow for increased productivity. This centralized approach eliminates the need to jump between multiple tools or panels, making it easier to maintain a consistent set of rules across the design.

User-Friendly Tabs: With user-friendly tabs like Clearances, Physical, and Electrical, Constraint Manager makes it easy to focus on specific design aspects. This targeted approach allows designers to more efficiently optimize various elements, such as spacing between traces or electrical properties, without getting overwhelmed by the full complexity of the project.

Intuitive Navigation: Intuitive navigation within Constraint Manager promotes quicker learning curves for new designers and greater efficiency for seasoned professionals. Its layout is designed to be easily understood, minimizing the time needed to get acquainted with its functions and capabilities.

Comprehensive 'All Rules' Tab: The All Rules tab offers a comprehensive view of all constraints, making it easier for engineers to identify conflicts or inconsistencies. With all the rules listed in one place, designers can quickly assess the status of their design rules, which saves time and reduces the risk of errors.

Continuous Improvement: Ongoing improvements and feature rollouts for Constraint Manager demonstrate its value as an indispensable tool in electronics design. Its continual evolution ensures that it stays aligned with industry needs, making it a reliable tool for both current projects and future advancements in electronics.