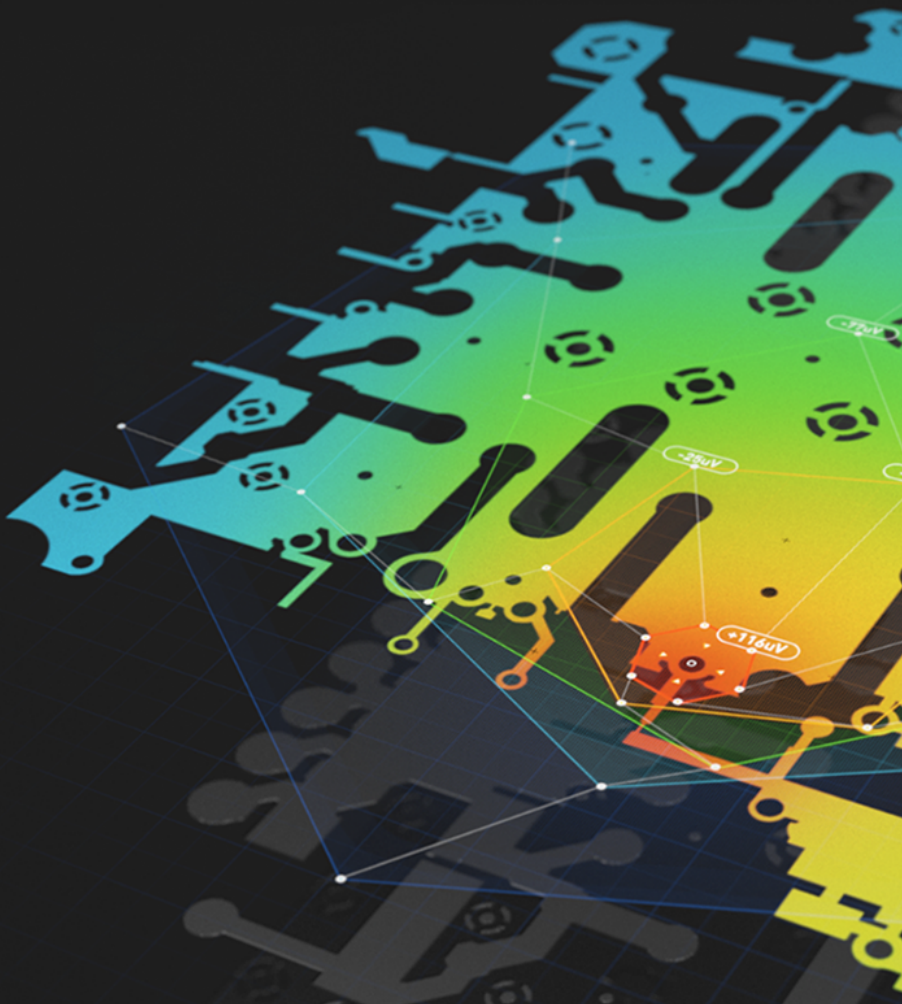
Altium®

PDN Analyzer User Guide



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THE PURPOSE OF DC POWER INTEGRITY (PI-DC)

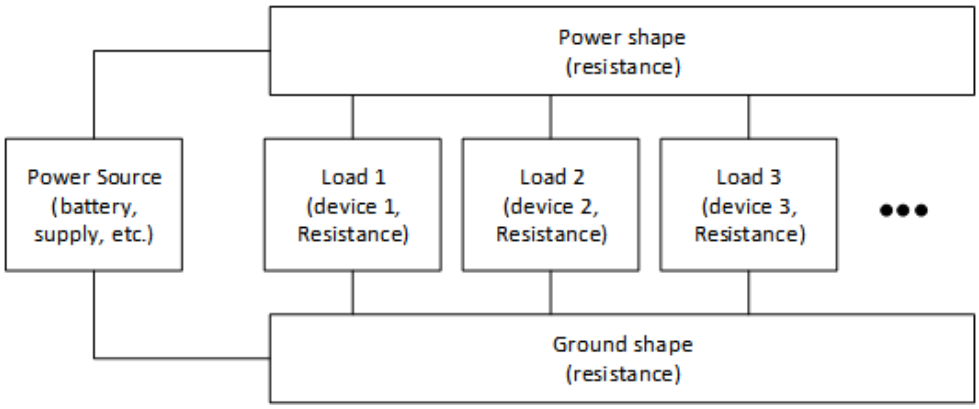
As digital designs continuously increase in density and complexity, it's more difficult and critical than ever to fully understand the impact of design decisions on the voltage and current performance of your Power Distribution Network (PDN). Rather than discovering PDN issues as a post-design afterthought to resolve with physical prototypes, today's PCB designers need a way to accurately identify and resolve PDN issues at design time, not after.

With PDN Analyzer powered by CST® in Altium Designer®, we've made PDN analysis an approachable and intuitive process for every PCB designer, regardless of their experience level. Inside this demonstration guide we'll guide you step-by-step through an initial PDN Analyzer setup, so you can become comfortable with optimizing your PDN at design time without ever relying on a physical prototype.

The Need for PDN Analysis at Design Time

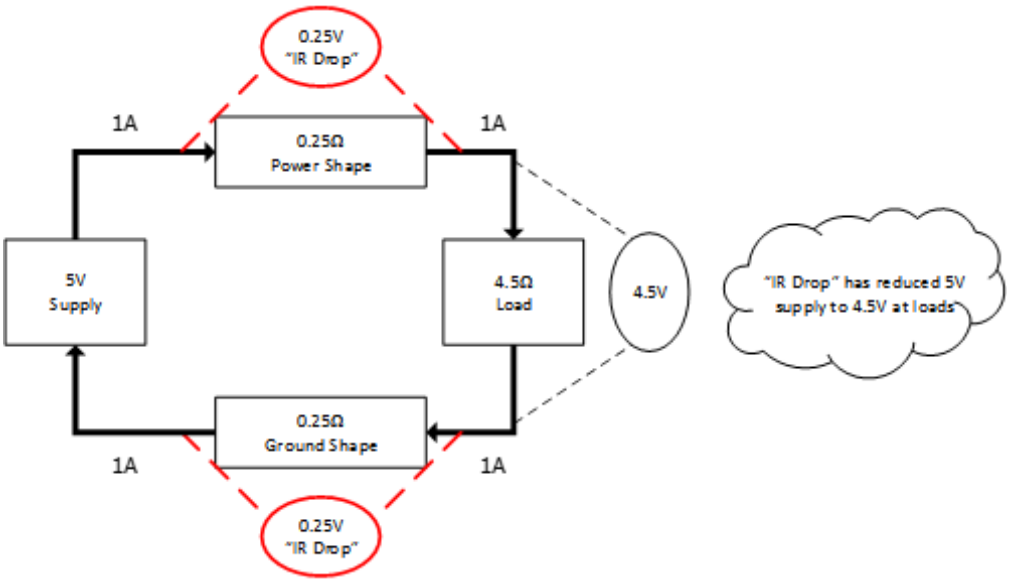
How do you currently ensure that adequate copper has been provided from your voltage sources to your loads? Are the planes providing the appropriate voltage range to not starve the loads? In a typical PCB design process, these questions often go unanswered, and engineers typically rely on a set of established standards to keep themselves within a conservative range of values to hopefully avoid PDN issues. This reliance on guesswork set an engineer up for catastrophic failures that can undermine your product's reliability and reputation if not caught in a prototype.

Every design needs to accommodate proper power consumption requirements for the chips on a board. The most critical step in doing this is to provide adequate copper for DC power delivery. When power consumption goes unchecked and unoptimized, IR-drop sets in, with the resisting of the power and ground shapes consuming voltage, robbing it from the loads that need it most.



Block diagram of basic power and ground shapes

The figure above shows a simple block diagram of the power source and ground shapes (traces and planes) which deliver power to the various loads (memory, microcontrollers, etc.). Notice that all the loads are tied to the same power and ground shapes, and depend on those shapes to provide their operating voltage(s). In general, we tend to assume that those power and ground shapes have zero ohm resistance, which is never true, and that assumption can cause problems. Because of the relatively large currents involved, even small resistances in the power and ground shapes can cause significant power consumption and voltage drops.



Demonstrating the IR Drop effect between a supply source and load

The figure above demonstrates an example of the problems that can arise if the resistance of the power and ground shapes aren't properly considered. Even though each shape has a relatively small resistance of only 0.25 ohm, they have caused the voltage at the load to drop from 5V to 4.5V. The designer has to be aware of this drop and ensure it can be accommodated, or change the design to reduce it, otherwise it may fail in the field.

Of course, this problem seems easy to solve – make your power and ground shapes short or large enough to only represent an insignificant resistance, using the following relationship: $R = \rho * L/A$, where:

- R is the total resistance of a shape (trace or plane)
- ρ is the resistivity of the material used for the shape (typically copper, $\rho \approx 1.7\mu\Omega$-cm)
- L is the length of the shape
- A is the cross-section area of the shape (width * thickness)

If you make your power and ground shapes short, thick, and wide, you will minimize their resistance. However, the difficulty with this process is that overly large shapes consume valuable routing space and may limit the amount of space for other voltage shapes. The design which has the properly sized power and ground shapes will be more compact and use less layers than one which arbitrarily uses overly large planes. The intent of PI-DC is to inform the designer whether their power and ground shapes are adequate and not excessive.

Another consideration for IR drop is the fact that the amount of power consumed follows the relationship I2R, and a small increase in current through a resistance causes a large increase in power consumption. This manifests itself as reduced battery life or the design heating up significantly when the power or ground shapes aren't large enough to accommodate the current passing through them. Ensuring very small IR drop through power and ground shapes, minimizes power consumption in those shapes.

At the extreme, if a shape is resistive enough (very narrow and long) and has sufficient current flowing through it, that shape essentially becomes a fuse, melting the copper shape, causing the design to fail, and possibly presenting a dangerous situation. IPC-2152 addresses this issue, but with pessimistic assumptions (for instance, no nearby thermally conductive copper) and designers often use that specification with the most conservative assumptions such as a minimum temperature increase allowed.

While PI-DC cannot replace IPC-2152 as a guideline for thermal considerations, it can provide valuable insight into how a design can safely be optimized by studying the voltage drops and current densities of a PCB's power delivery system. A design optimized for the lowest current density and voltage drop between the sources and loads will also generate lower heat decreasing the likelihood of thermal issues.

Another aspect PI-DC addresses is the amount of vias used for power delivery. The problem is quite similar to that of sizing the shapes properly. If there are not enough vias, voltage is lost and power is wasted through IR drops. If too many vias are used, valuable routing real estate is wasted. If too many vias are used for a particular voltage, those vias pass through shapes on other layers, reducing their copper cross-section and causing problems for those other voltages. Similar to shape dimensioning, analyzing the voltage at the load allows for proper via sizing and/or numbering.

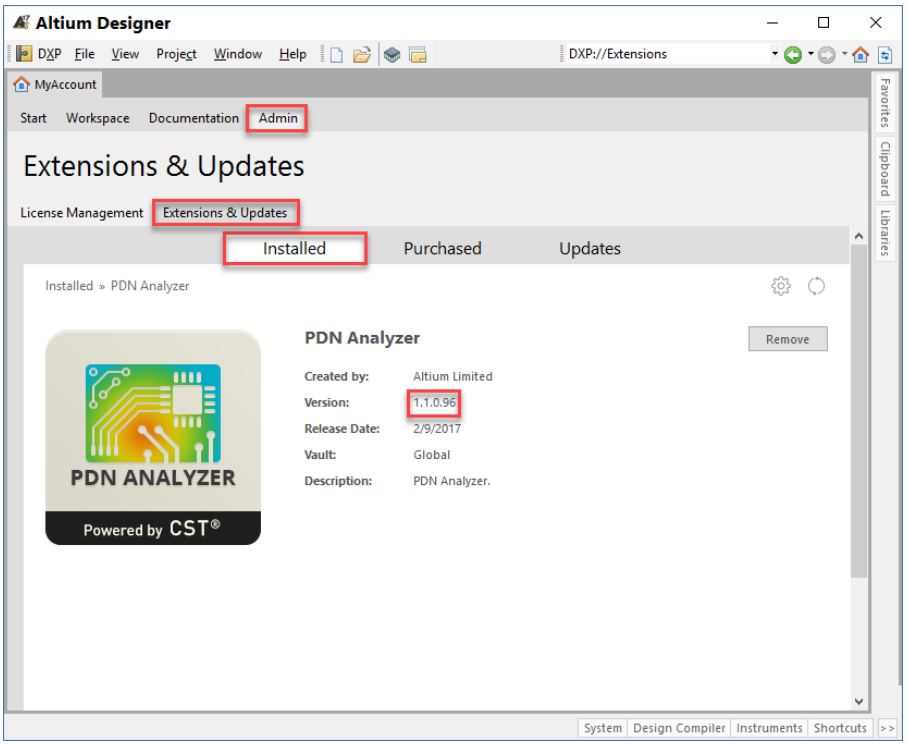
In the absence of reliable data on the voltage drop through the various power and ground shapes and vias, the designer is forced to be conservative, using excessive plane shapes and vias, consuming valuable design real estate and increasing layers and design form factor. PDN Analyzer provides accurate information about a design's DC power distribution suitability in an easy-to-use, straightforward, and speedy manner that enables designers to make the most efficient power distribution designs possible.

Not only are the results suitable for final design verification, but they can also be used in the planning stages of a design to architect power delivery as efficiently as possible. PI-DC is an invaluable tool in achieving the most efficient and robust power delivery network possible, and PDN Analyzer makes running that tool straightforward, intuitive and efficient.

FIRST-TIME SETUP FOR PDN ANALYZER

PDN Analyzer is supported on Altium Designer version **17.0.0** or later and requires a 64-bit Windows operating system. To verify that the PDN Analyzer extension is installed, follow these steps:

1. Sign into your AltiumLive account in Altium Designer.
2. Select to **DXP » Extensions and Updates » Installed**.
3. Verify that the extension displays as shown in the figure below:



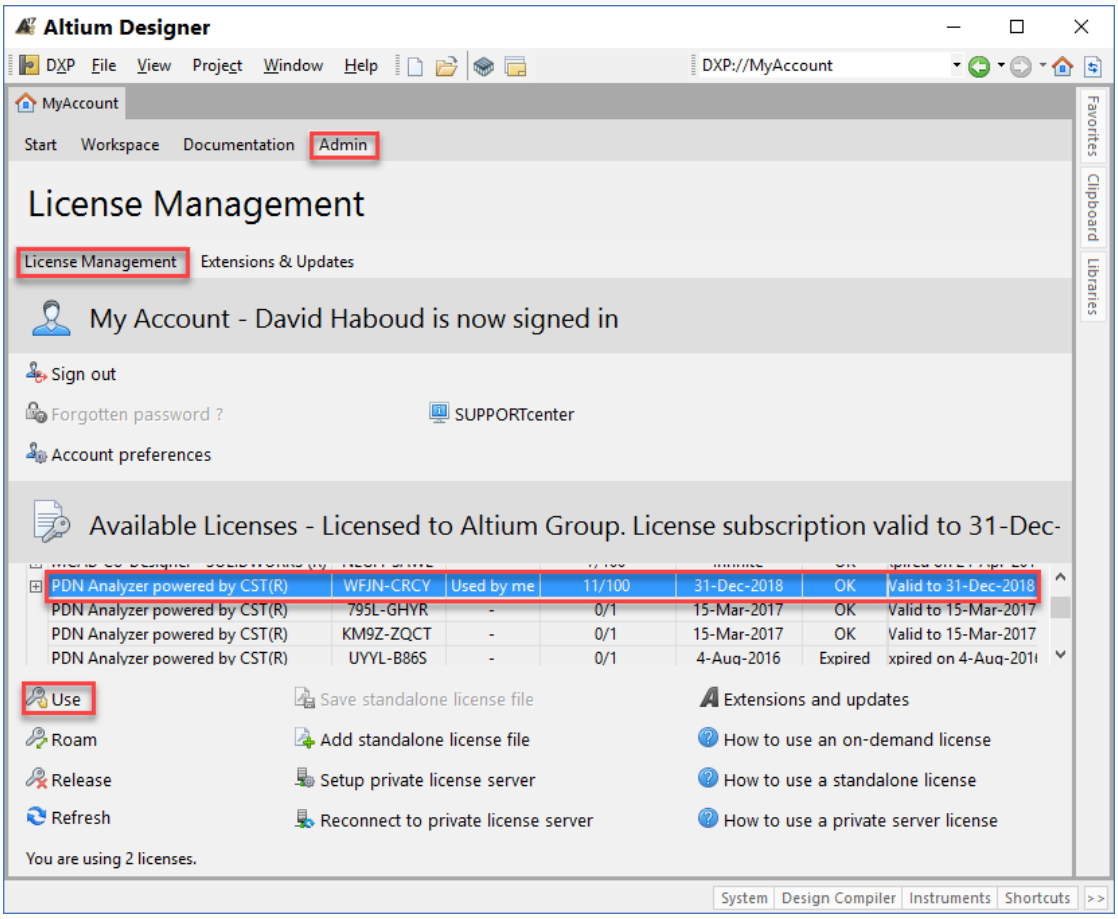
Verifying PDN Analyzer as an installed extension

If PDN Analyzer is not installed, follow these steps:

1. Select **DXP » Extensions and Updates**.
2. Select the **Purchased tab**
3. Select the Download icon next to the PDN Analyzer extension listing
4. Once downloaded, restart Altium Designer to complete the installation

Keep in mind, the PDN Analyzer extension requires a separate license in addition to your active Altium Designer license. Activating your PDN Analyzer license can be accomplished with the following steps:

1. Open Altium Designer, then select **DXP » Extensions & Updates**
2. In the License Management window, select your PDN Analyzer license as shown in *the figure* below
3. Select **Activate**



Activating a PDN Analyzer license in Altium Designer

WORKING WITH THE PDN ANALYZER INTERFACE

With your PDN Analyzer extension installed and activated, we can now begin the process of configuring the interface, running your first analysis, and viewing the results.

Configuring Your Analysis

Configuring your analysis is simple with the PDN Analyzer extension. The configuration process can be summarized into four easy steps:

1. Define the **Source Power Net**, **Load Power Net**, and **Ground Net**.
2. Define the **Source** device and **Load** device(s) relative to one specific **DC Power Rail** of interest.
3. Define **Source** net **Voltage** and maximum **Current**.
4. Define **Load** net **Current** and minimum **Voltage** levels relative to one specific power net.

The entire configuration setup can be saved to a configuration file and reloaded at any time. Note that all analysis is performed on a single power rail per simulation. Analyzing multiple **DC Power Rails** requires defining and saving multiple setups into unique configuration files. You can then individually analyze all power nets of interest. If critical attributes are not defined or are incorrectly defined, a message is displayed indicating the error and prevents the simulation from running.

Running Your Analysis

Once you have defined your configuration successfully, the **Ready to Simulate** message will appear, allowing you to perform a DC analysis. The analysis engine calculates the DC resistance across the entire path of copper objects connecting the source power and ground pins to all load power and ground pins. The resulting DC voltage drop is subsequently displayed for the user to determine the integrity of the power net. Analysis run times vary depending on design size and complexity.

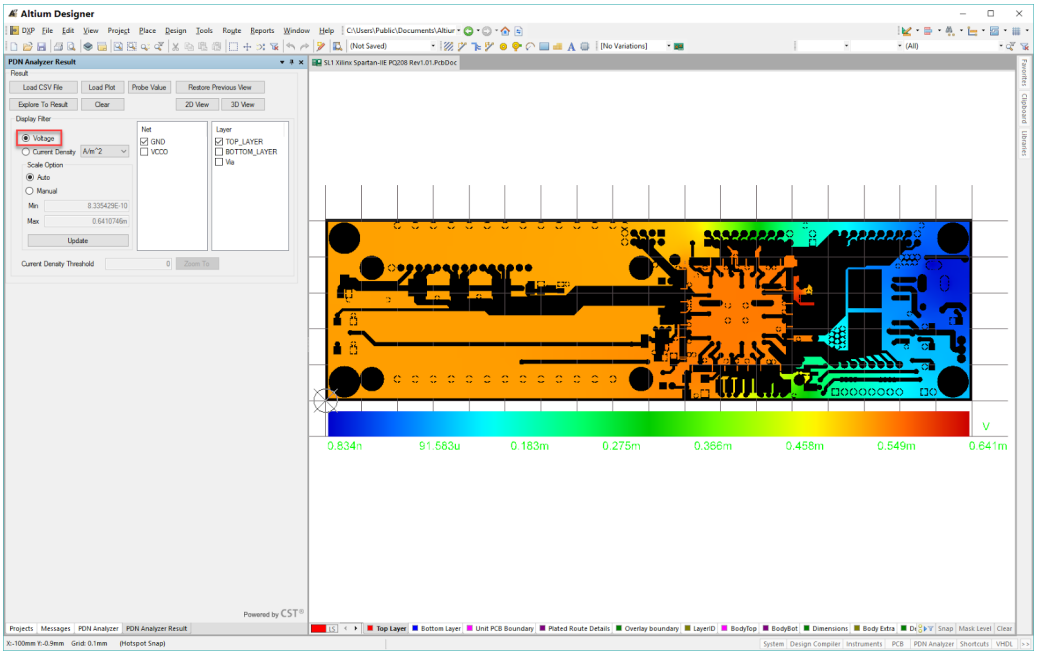
Viewing Your Analysis Results

When the design analysis completes, the graphical results will be annotated on the physical copper objects of the analyzed net and may be viewed in 2D or 3D mode. The **Ground Net**, **Power Nets**, and **PCB Layers** graphical results display can be toggled individually, allowing you to pinpoint any section of your PDN.

Display Filter Modes

Voltage Mode:

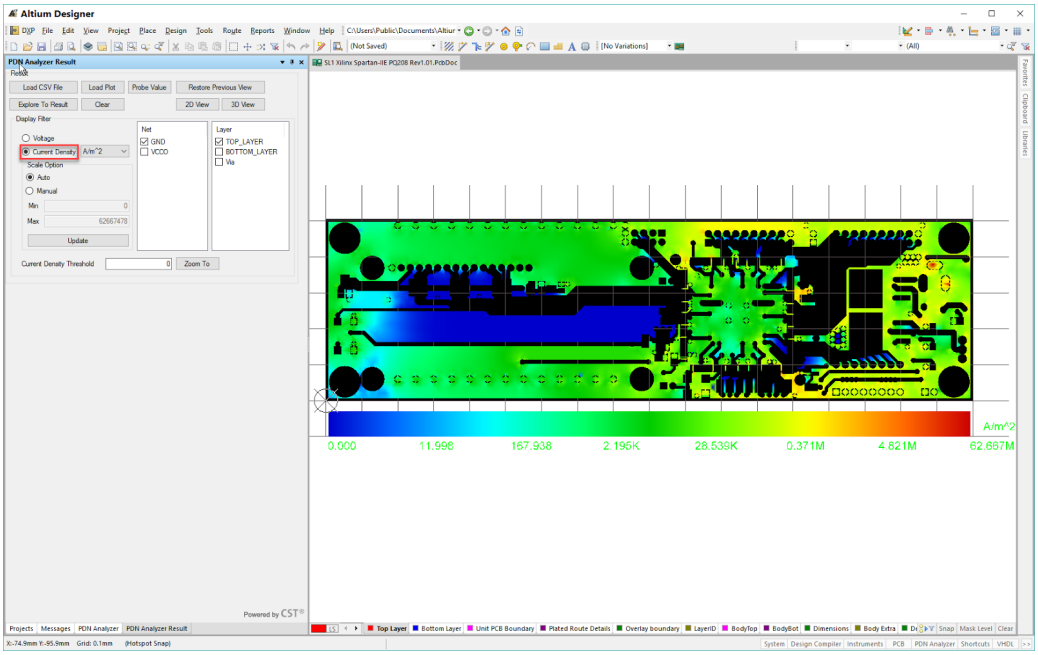
The display annotates a color coded range of values reflecting the minimum to maximum DC voltage calculated at specific points in the physical copper.



Display Filter Voltage Mode

Current Density Mode:

The display annotates a color coded range of values reflecting the minimum to maximum Current density as **Current** (**uA**, **mA**, or **A**) per **Area** (**square mils**, **square mm's**, or **square meters**). This is useful to determine where the width/area of a copper trace, polygon, or plane needs to be altered to achieve optimum Current distribution..



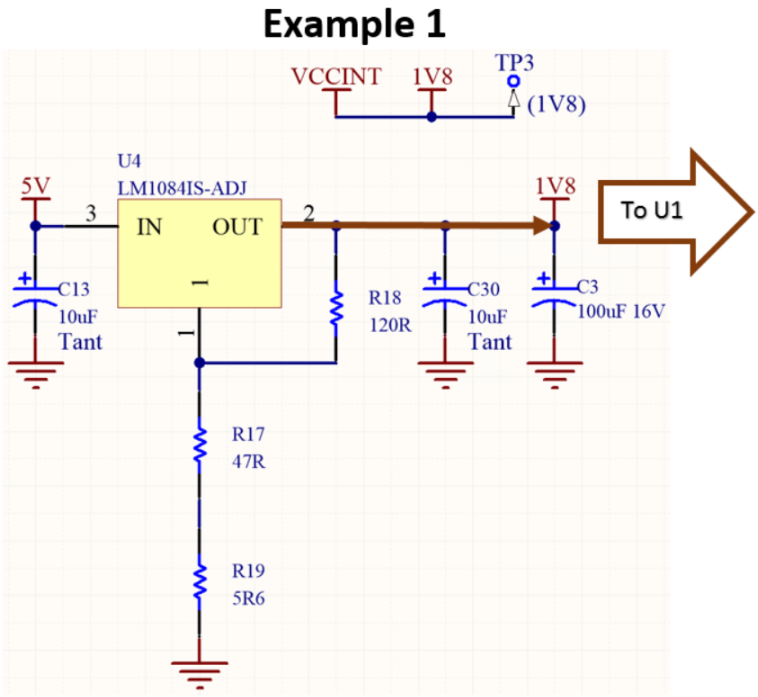
Display Filter Current Density Mode

Note: The **Voltage** or **Current Density mode** values of a precise point in the copper can be displayed as a text value by selecting **Probe value** in the results panel and clicking on the desired location.

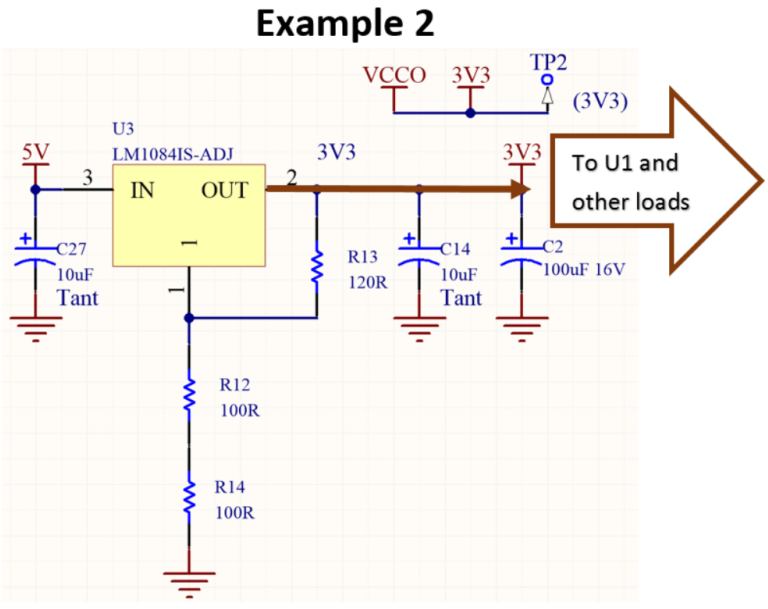
PRACTICAL EXAMPLES AND DEMONSTRATIONS

We will be using the SpiritLevel design for the examples in this section. By default, these files can found in the example folder of your Altium Designer installation folder: **C:\Users\Public\Documents\Altium\ADxx\Examples\SpiritLevel-SL1**

We will focus on the following examples:

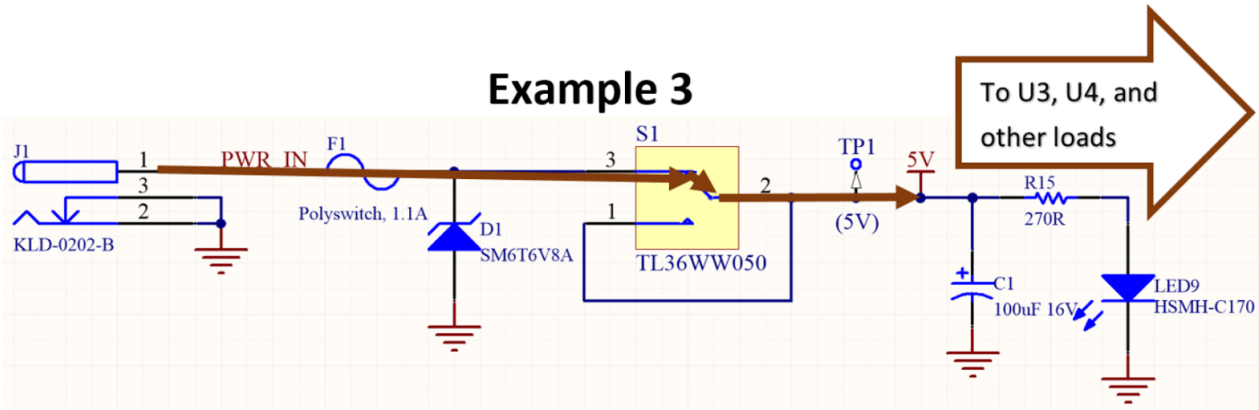


Example project 1: VCCINT (1.8V) from U4 to U1



Example project 2: VCCO (3.3V) from U3 to U1

PWR_IN (5V) from J1 through F1 and S1 to U3, U4, and other loads

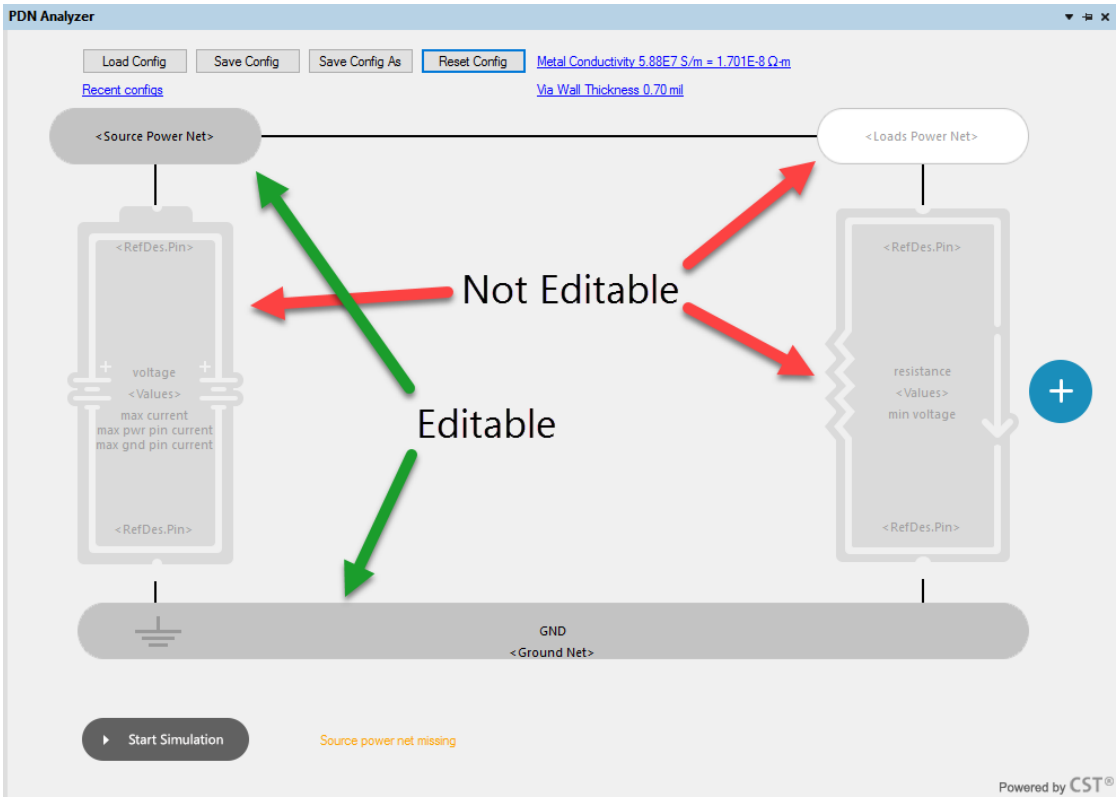


Example project 3: PWR_IN (5V) from J1 through F1 and S1 to U3, U4 and other loads

Example 1 Setup: VCCINT (1.8V)

Launching PDN Analysis

1. Open a schematic or PCB document of SpiritLevel and open the PDN Analyzer extension (**Tools > PDN Analyzer**). This launches the extension within a separate panel as shown in the figure below:

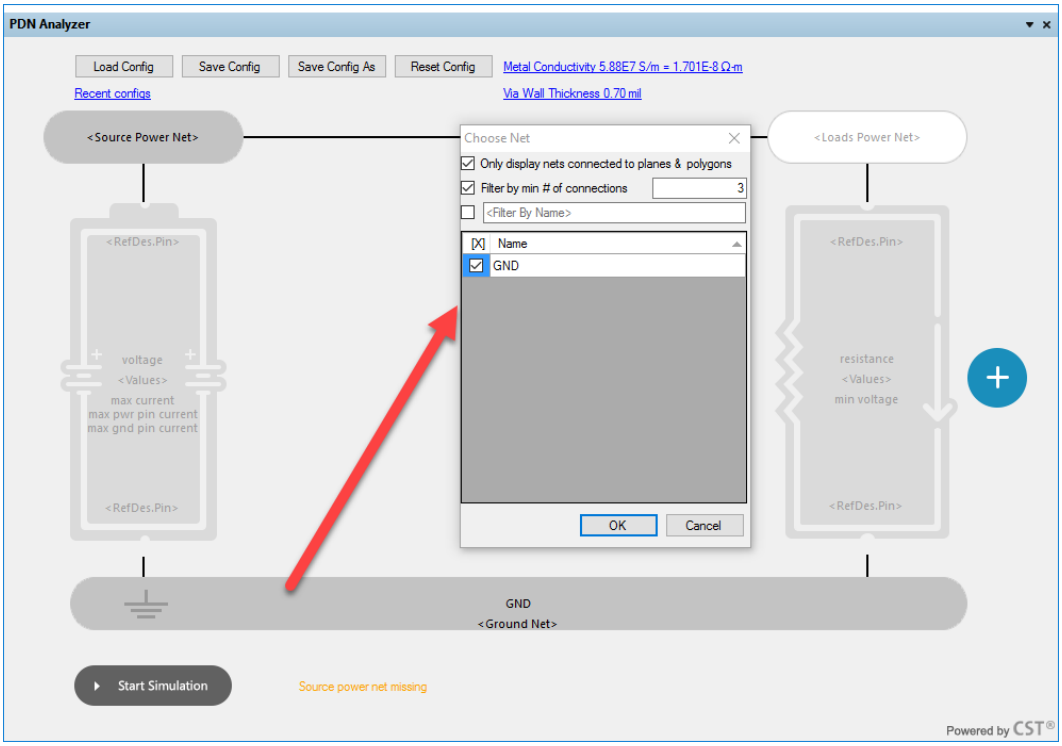


Opening the PDN Analyzer interface

The options outlined below provide a brief overview of the settings you will see on the PDN Analyzer interface. If some of these elements are not visible then you may have to resize the interface panel. Items with subdued background and muted text aren't yet editable – other information must be supplied before these are enabled for editing. Items that are bolder in shading and with clear text can be edited as necessary.

- **Load Config** allows loading PDN Analyzer configurations that have been previously saved.
- **Recent configs** has a double purpose:
  - Displays the current configuration name after it has been loaded or saved.
    - ◊ If the configuration has been altered since loading or saving, an asterisk will be appended to the displayed name.
  - Provides a quick drop-down selection capability of previously saved or loaded configurations.
- **Save Config** allows saving PDN Analyzer configurations.
- **Save Config As** allows saving PDN Analyzer configurations with a specific name.
- **Reset Config** clears any configuration entries.
- The **Metal Conductivity** option displays the current net conductivity value and allows modifying the inputs into that value, including base metal conductivity and temperature compensation.
- **Via Wall Thickness** defines the thickness of the **barrel** portion of the via. The barrel material is the same as specified in the Metal Conductivity form.
- The **Start Simulation** button at the bottom left is only enabled once all required parameters are provided.

2. Click on the <**Ground Net**> symbol at the bottom of the canvas to view its setup form and verify that **GND** is already selected as the ground net. If it wasn't, it would be selectable here. The net named **GND** is selected by default, so this step shouldn't be necessary for this design.

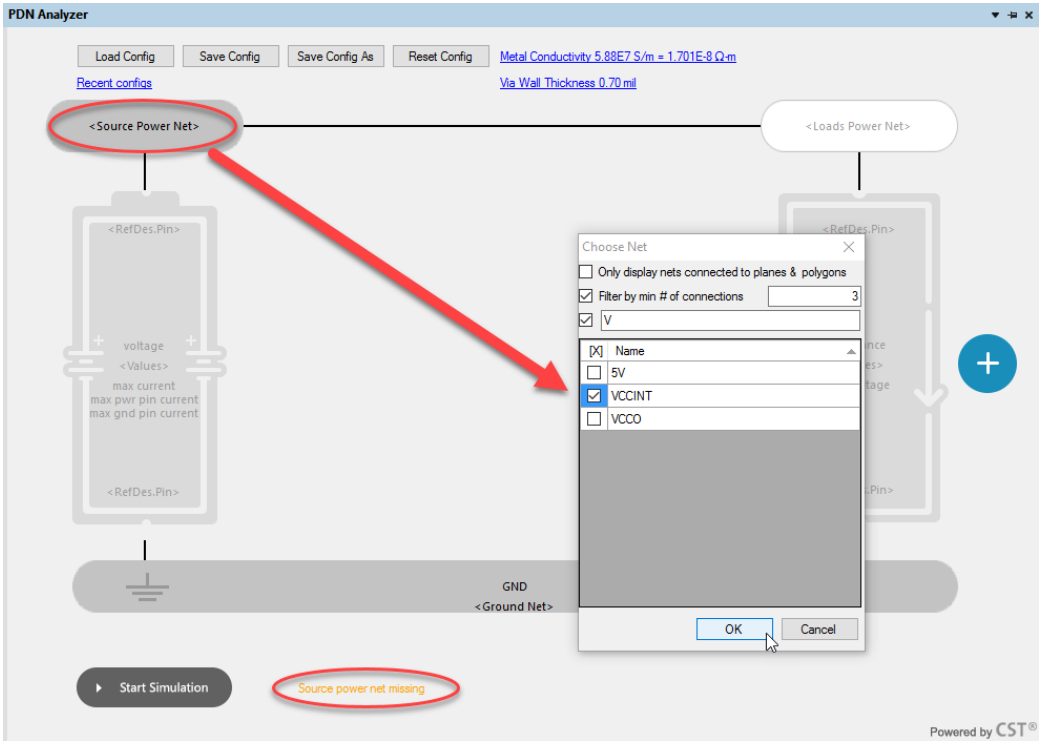


Verifying the Ground Net

a. Note the **Source power net missing** message at the bottom of the canvas. Generally, the message displayed here will indicate the next setup step that should be taken in preparation for simulation.

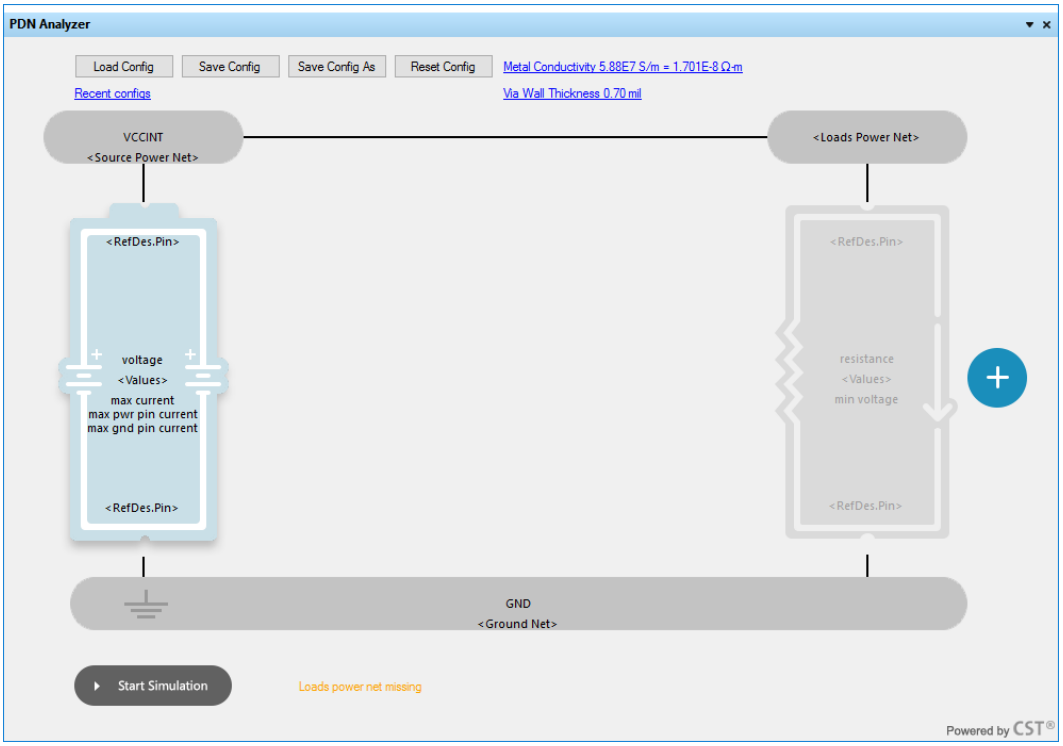
3. Select the **<Source Power Net>** icon to choose the power delivery net you want to evaluate as shown in the figure below (**VCCINT** in this case). The filter options are set by default to list only likely power nets.

4. Enable the box next to **VCCINT** and press **OK**.



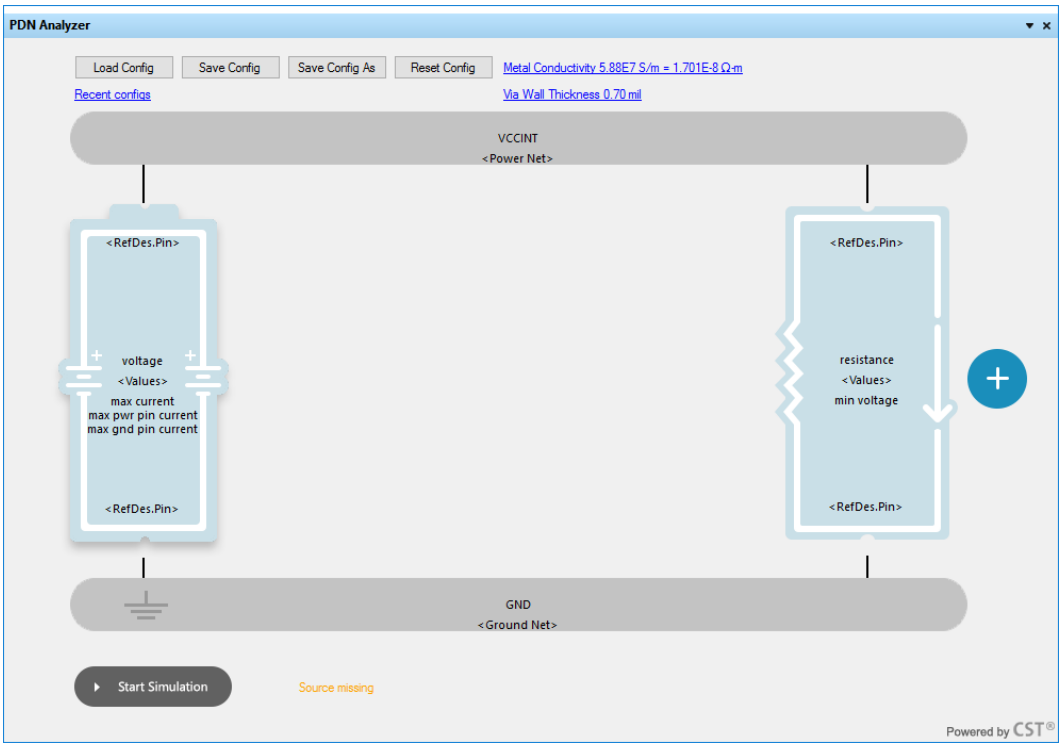
Identifying the Source Power Net

5. Notice that the **<Source Power Net>** icon background changes to blue to indicate it has been filled in, and the message next to the simulation button changes. Also note that the voltage source and **<Loads Power Net>** symbols changed from their grayed-out state (see figure below) to signify that they can now be edited.



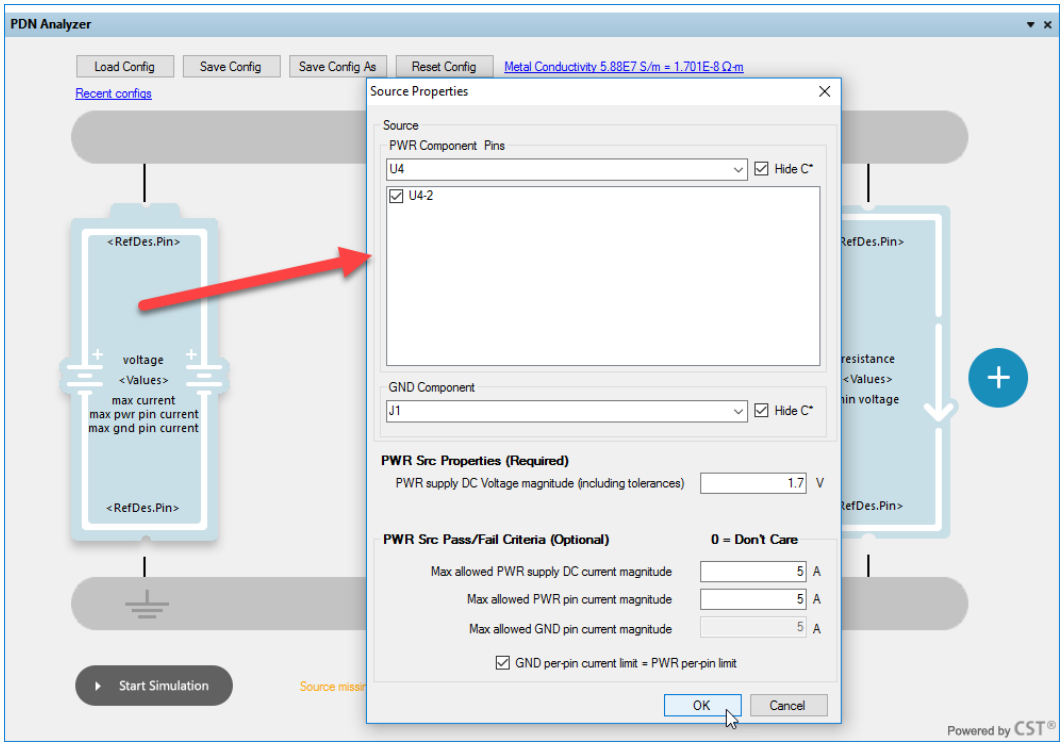
Source Net and Voltage Source Configured

6. Select the **<Loads Power Net>** symbol in the upper right corner of the PDN Analyzer canvas (figure above). In this case the load power net is the same as the source power net (VCCINT), so **OK** can immediately be pressed to accept the default.
   a. Note that the **Source Power Net** and **Loads Power Net** symbols have now been merged (see figure below) to indicate that they are the same net (**VCCINT**). Note also that the load on the right of the canvas is now enabled for editing, and the message now prompts us to define the voltage source.



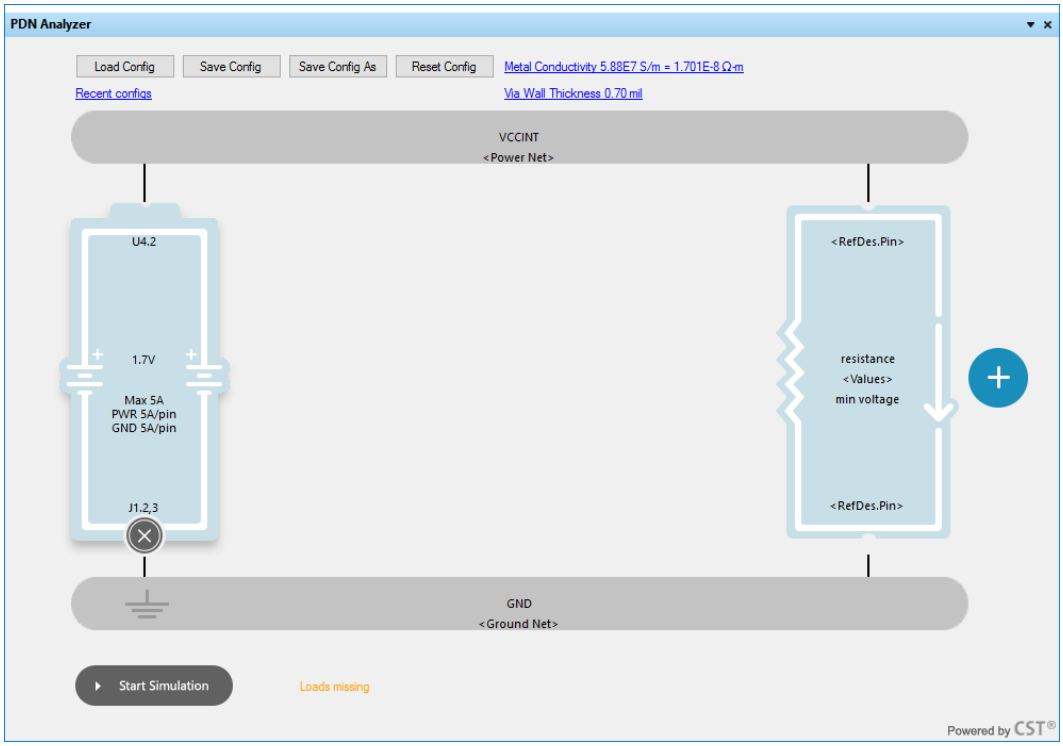
Power Net Setup Complete

7. Select the source **<RefDes.Pin>** icon to choose the source connections and parameters as shown in figure below.
8. Choose **U4** and **U4-2** as the **power source** and **pin**, since they deliver power to this network. Use the **Hide C*** option to filter out capacitors while locating the **U4**. Since **U4** is a **series pass** (**linear**) **regulator**, it provides the power to this network but not the ground node.
9. Select **J1** as the **Ground Component**. Both **J1** pins (pins 2 and 3) that have a connection to the **GND** net will be used.
   a. We've chosen to derate the input 1.8V by 5%, or 0.1V, so we chose 1.7V as our simulation Voltage.
   b. We've also selected 5A as the maximum current the part, and each of its pins, can deliver.
   c. By default, the ground pin max current is set to match the PWR pin current. This is fine for this example.



Voltage Source Setup

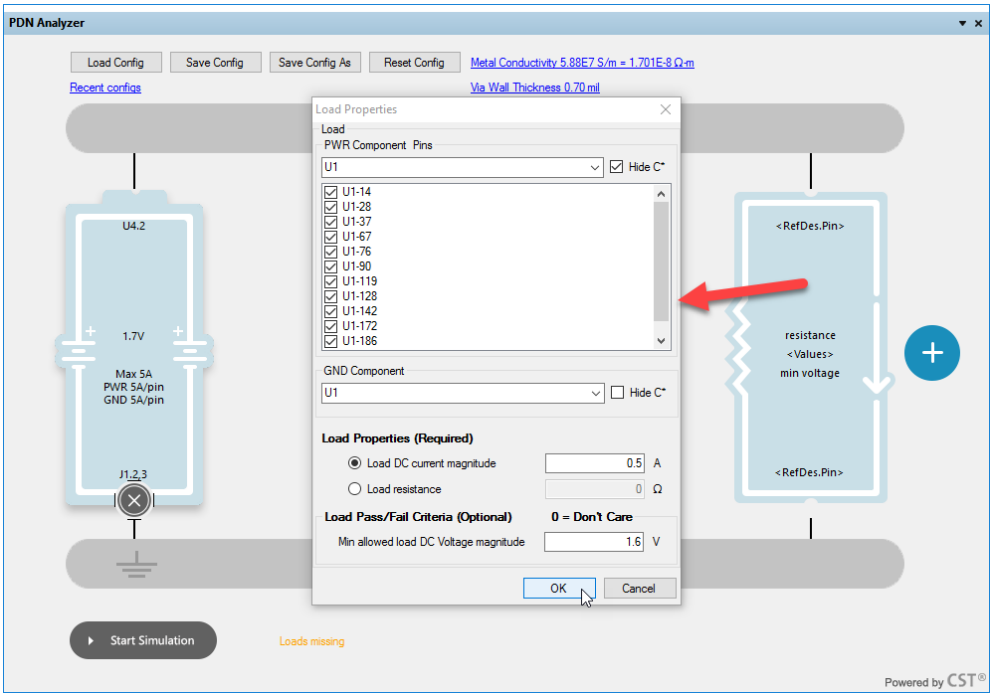
10. Select **OK** to commit to the voltage source settings. The message at the bottom changes to **Loads missing** (figure below), indicating that we aren't ready to simulate yet...



Voltage Source Configured

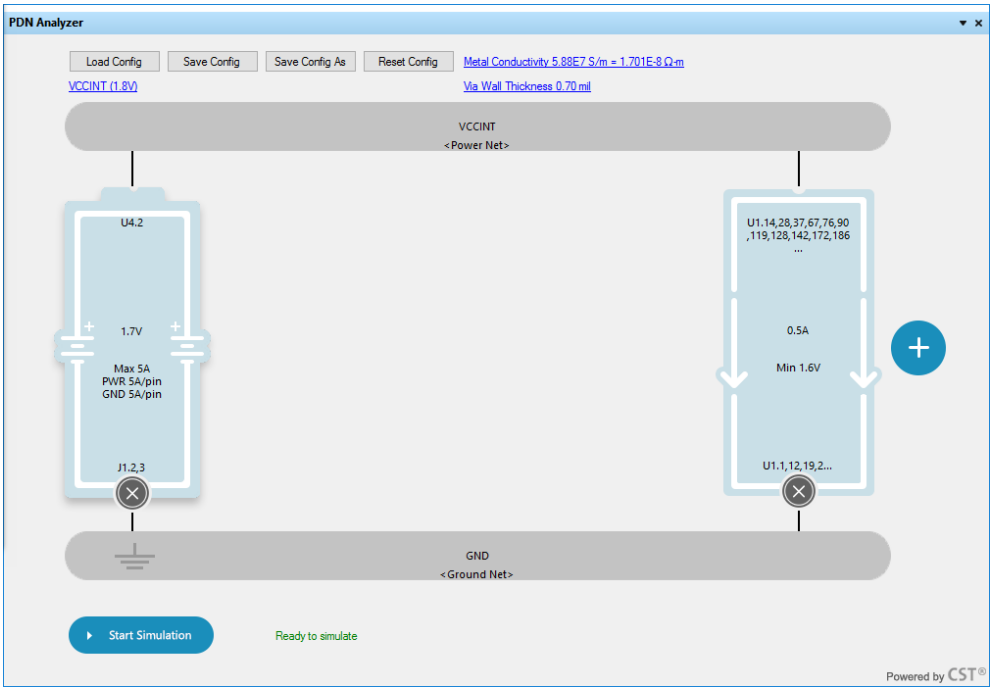
11. Select the **<Loads Power Net>**. In this case it is the same as the source power net (**VCCINT**), so Ok can immediately be pressed after the **<Loads Power Net>** icon has been selected. **VCCINT** is displayed in blue as the source and loads power net and the message next to the simulation button has changed.

12. Select the load **<RefDes.Pin>** icon to choose **U1** as the load and enter the following parameters:
    - Assign 1.6V as the allowed minimum (for this example, we're allowing a 10% DC drop, 1.8V – 10% = 1.6V).
    - Assign 0.5A as the load DC current magnitude.
13. Select **OK** to complete the load definition. The message at the bottom of the canvas indicates that we are ready to simulate.



Configuring the Load

Note: In this case we're assuming all the pins of **U1** have the same parameters, meaning the **0.5A** load current will be equally divided between the power/ground pins of **U1**. If some pins had different parameters, only a subset of pins would be selected and assigned parameters and a separate **U1** with the other pins would be added with their parameters.



Ready to Simulate

14. All the boxes are blue, indicating they've been filled out, and the message next to the button indicates we're ready.

PDN Analyzer allows queueing of multiple simulations (configurations) so that they can be run in batch mode. While PDN Analyzer simulations are often quite short in duration, some very complex boards with many voltage rails can yield lengthy simulation runs for each rail. Batch simulation allows the user to run these simulations while away from the computer and return to a host of results that are ready to view.

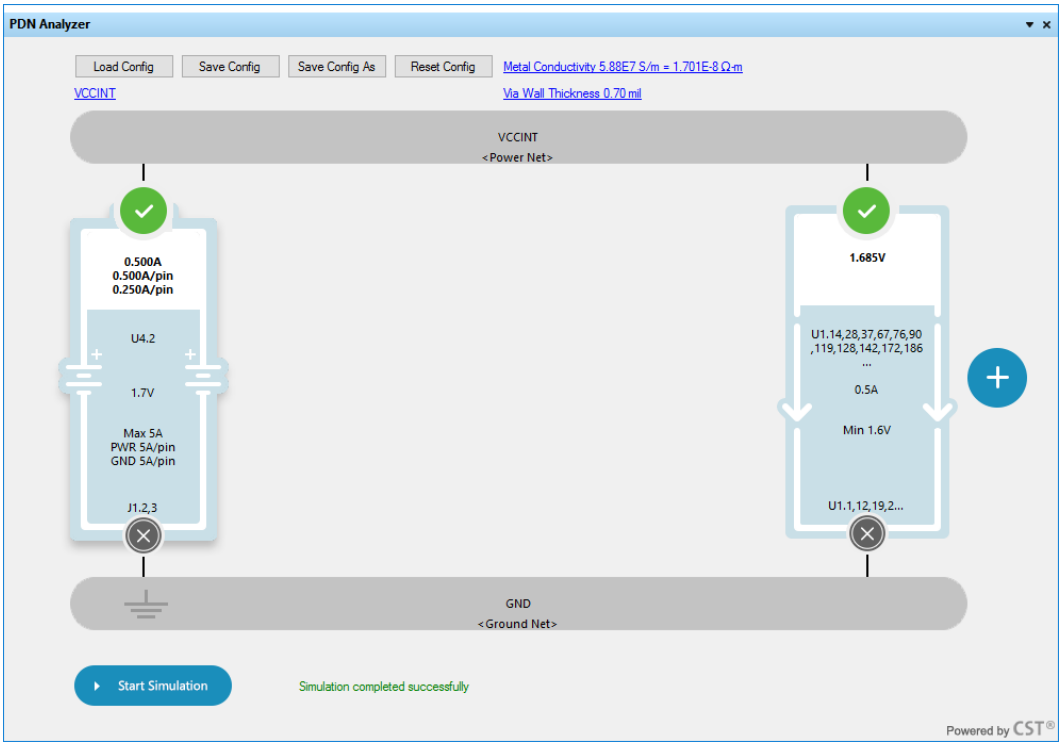
After saving this configuration per the next step, you may choose to configure the remaining two examples (Nets **VCCO** and **PWR_IN**) and saving them for batch simulation. New configurations would be created after saving the current config, and the selecting the **Reset Config** button at the top of the PDN Analyzer canvas.

15. Click on the "Save Config As" button to save this configuration. Provide **VCCINT (1.8V)** as the configuration name and select "Save" to complete the action.

Note: The configuration name is now displayed below the **Load Config** button. Clicking on the name will allow you to quickly choose between this and other saved configurations.

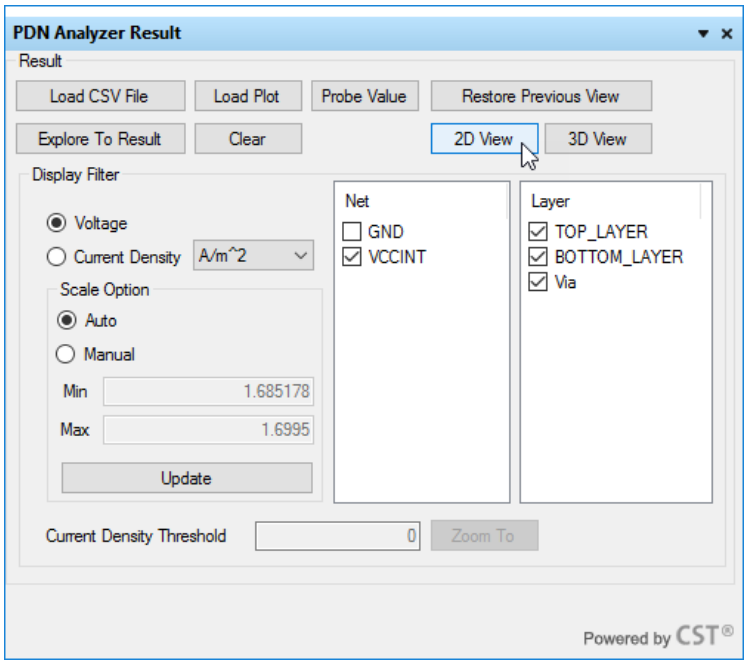
16. Press the **Start Simulate** button at the bottom left corner to continue.

17. Review the simulation results on the PDN Analyzer canvas per figure below. Depending on your display options, it may take you to the message or results windows. Notice that neither the maximum current of the source nor the minimum allowed voltage at the load were violated, so green checkmarks appear above them. Violations would have been indicated by red X's.



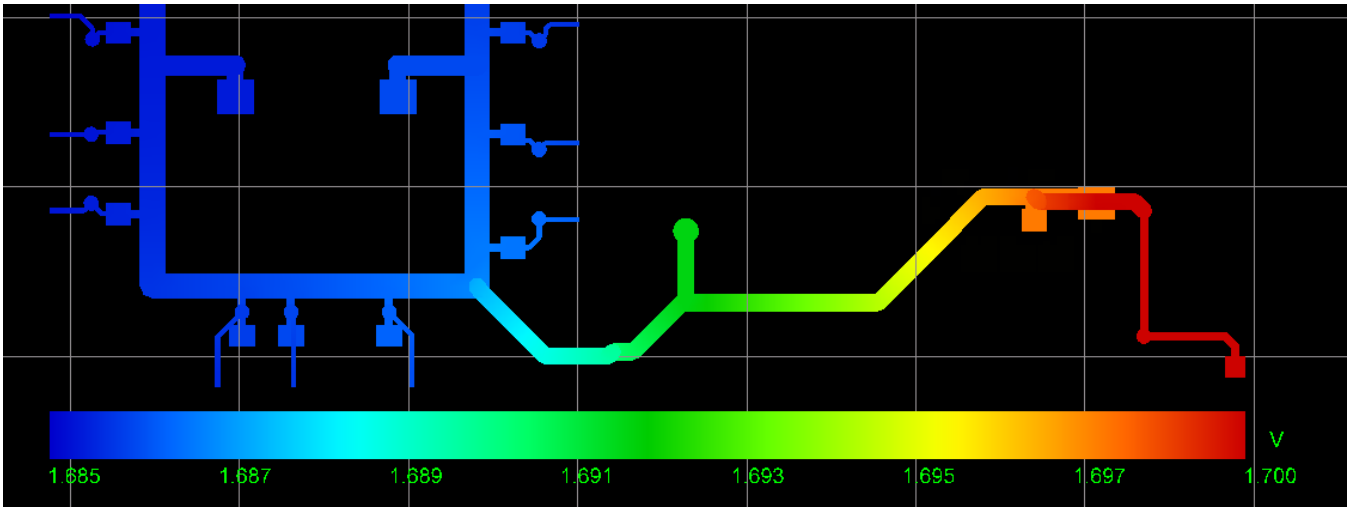
Reviewing PDN analysis results with no errors found

18. View the results of the voltage net graphically. Select the **PDN Analyzer Result** window, **VCCINT** as the **Net**, and **Top**, **Bottom**, and **Via layers**. To Switch between a **2D** and **3D view** select either **2D View** or **3D View**. (**Voltage** Display, **Auto** Scaling, **VCCINT** as the **Net**, and **Top**, **Bottom**, and **Via** layers enabled).



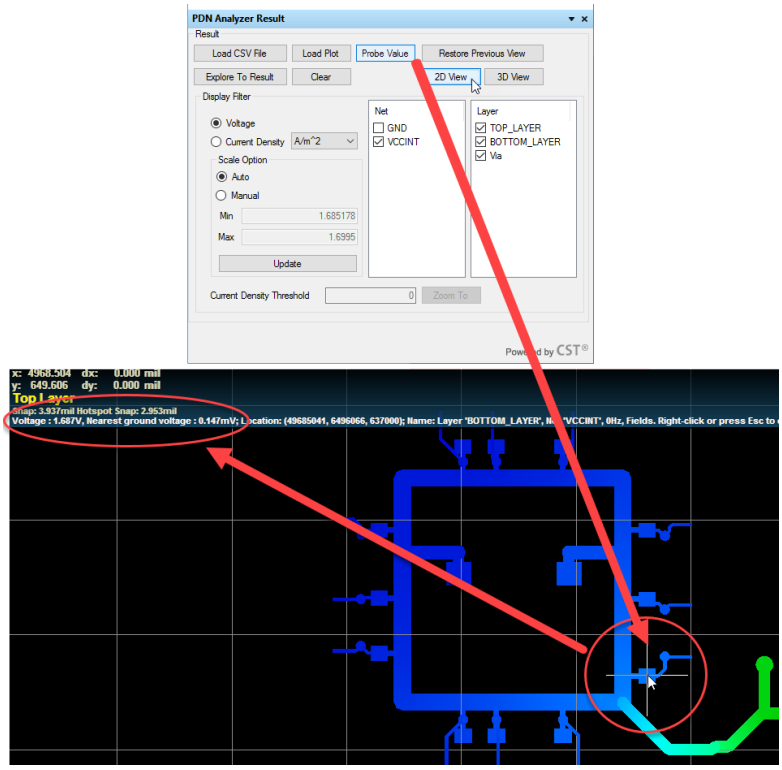
Configuring the PDN Analysis result view for 2D viewing

19. Select the **2D View** button, and then select the **...PcbDoc** sheet in Altium Designer to bring it to the front. Your results should look similar to below in **2D View**:



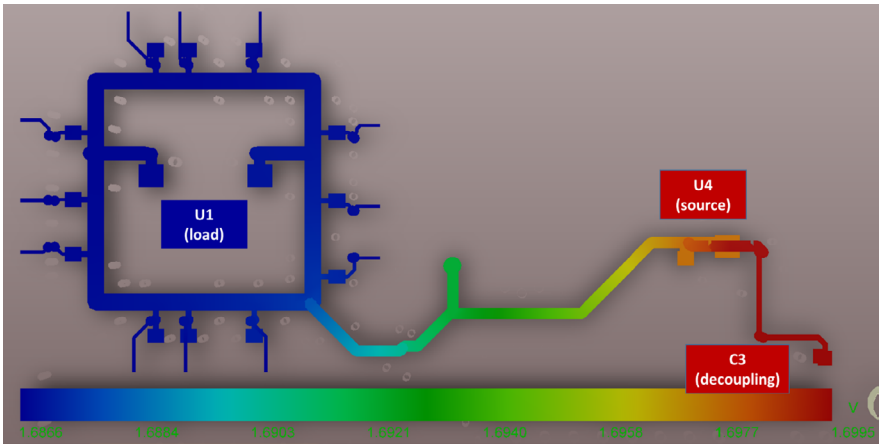
Voltage Drop Plot (2D View)

20. In the **PDN Analyzer Result Window**, select the **Probe Value** button and **click** on a section of the **VCCINT** route to view the voltage at that location as well as at the **nearest ground location**.



21. Select the "3D View" button for a 3D view per Figure 13 below.

Your result should look similar to the figure below in when switched to **3D View**:



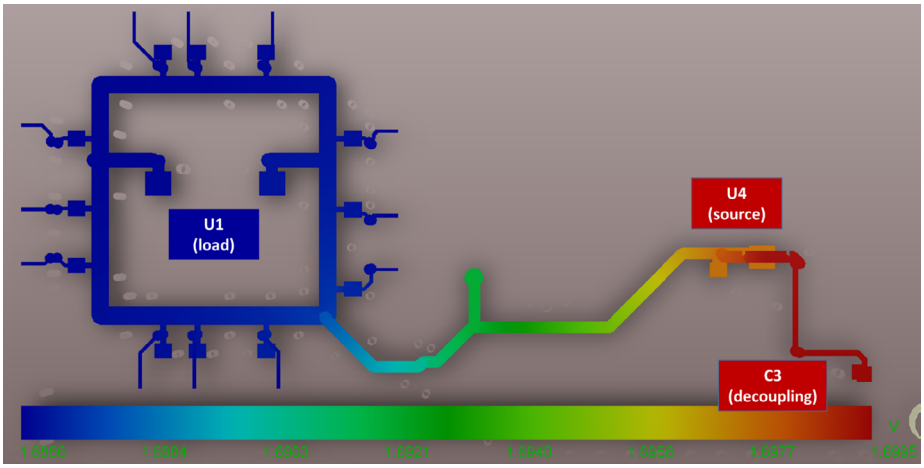
Voltage Drop Plot (3D View)

Please make note of the following details on the current gradient overlay:

- The highest Voltage displayed is **1.7V**, at the **Source** (**U4**).
- There is no significant DC Voltage drop between **U4** and **C3** since the capacitor was not defined as a load (as is normally the case, as capacitors are considered open circuits under DC conditions, and therefore would not be modeled).
- The lowest Voltage displayed is **1.69V**, at the **Load** (**U1**).

- Though the image may seem to suggest a large voltage drop across this power delivery shape (due to the **Auto Scale** Option setting, which automatically spreads the color spectrum across the resulting voltage range), there is actually very little voltage drop (less than **15 millivolts**) when a load of **0.5A** is assumed.
- If you view the **Voltages** in **3D**, you'll be able to see that there is some voltage drop at the three vias (a difference in color between the top and bottom of the vias) and in the track between **U4** and **U1**.

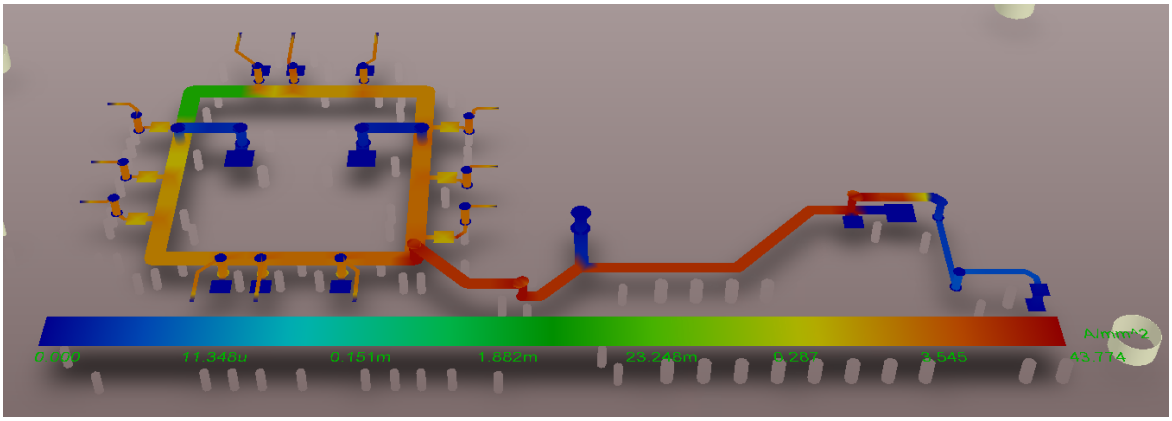
If you view the **Voltages** in **3D**, you'll see the voltage drop across the three vias (a color change from the top to the bottom of the vias) and in the track between **U4** and **U1**.



3D View Showing Via Voltage

20. View the current density results of the voltage net graphically. Select the Current Density radio button in the PDN Analyzer Result window, and change the units to A/mm2.
21. Select VCCINT as the Net, and both Top, Bottom, and Via layers.

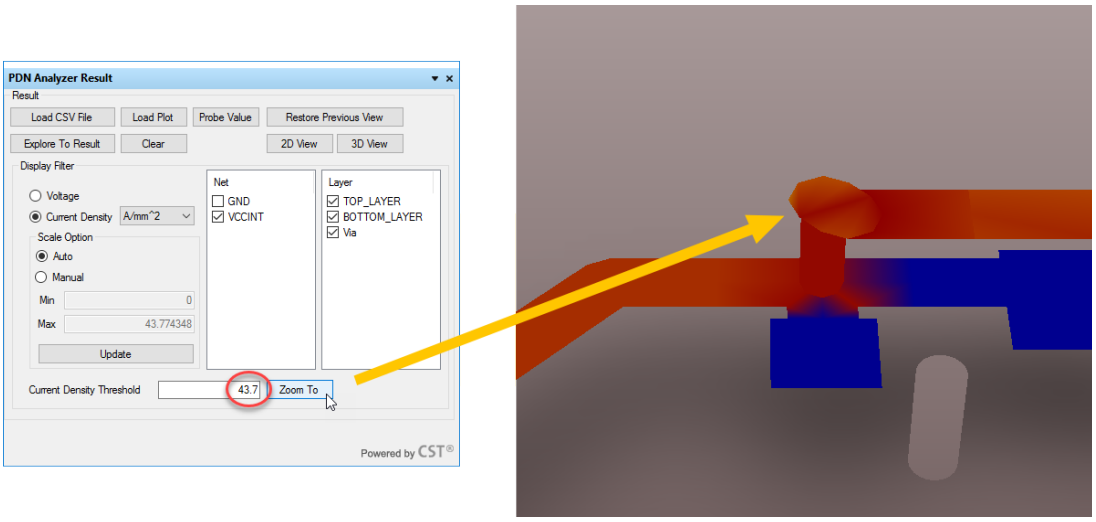
Notice (Figure below) that the track between **U4** and **U1** has the highest current density and should be the first portion to widen if there were excessive voltage drop on this net. Also note in the **PDN Analyzer Result** window, that the current density ranges from **0 A/mm²** to **43.77 A/mm²**.



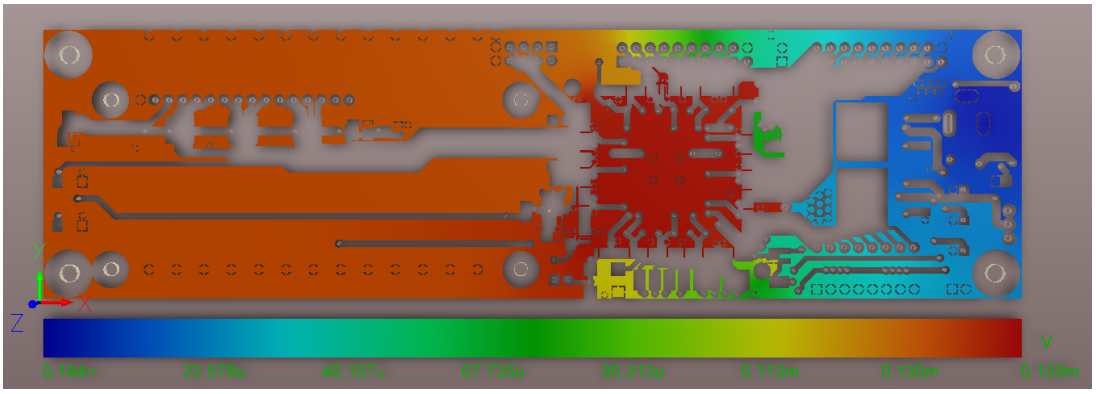
Viewing the current density results for the VCCINT net in 3D

To locate the **hottest** copper areas automatically, perform the following step:

a. Enter a value just under the **Max** reported value of **43.77** into the **Current Density Threshold** field as shown below – use **43.7** in this case. Now, clicking on the **Zoom To** button will zoom and center the first mesh element that it comes to, which exceeds the threshold value. Repeatedly clicking **Zoom To** will cycle through all mesh elements that exceed the threshold value.

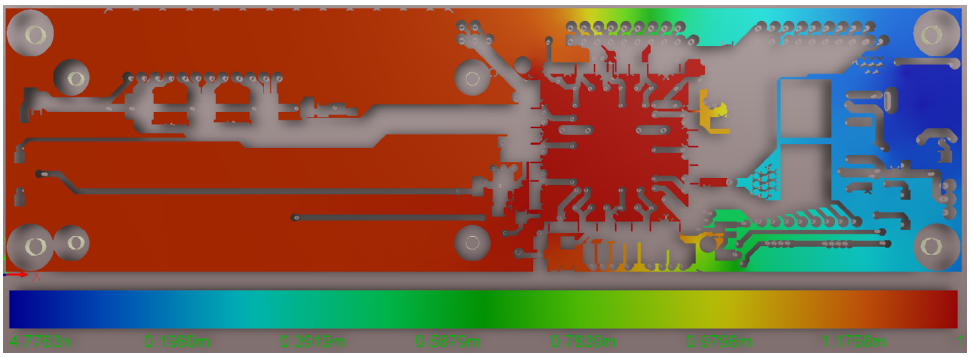


22. Select the **Voltage** radio button, and enable **GND** as the **Net** as well as **TOP_LAYER**. Notice that there is very little voltage rise on the large **GND** shape - the maximum voltage is only **158uV**.



GND Plane Voltage

23. View the voltage results of the **ground** net graphically. Select **GND** as the **Net** and the **Top** layer. Notice that there is hardly any voltage on the large GND shape, the maximum voltage is only **1.17mV**.

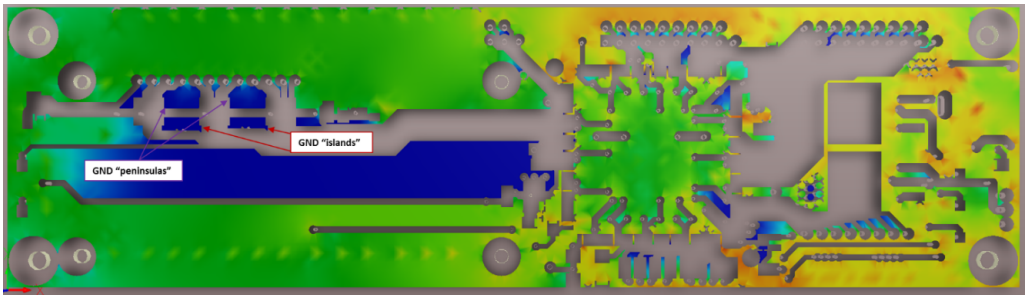


Viewing the current density results for the ground net in 3D

Analyzing the Results

If you switch to **Current Density** and view the **GND** net, you'll see that there may be an issue with this design – there are both peninsulas and islands in the **GND** shape, as indicated by their blue color (no current flow). Of course, this only represents the DC current flow for **VCCINT** – all other DC voltages must be checked before we can know that portions of a **GND** shape are unused.

It is also essential to check that ground shapes aren't used for AC current return before removing them, perhaps by replacing capacitors with **1k-ohm** resistors in a simulation to view their impact on the return path. It is obvious that even small connections in a critical location (bottom left of **U1**) would convert the large **GND** peninsula to a less problematic ground shape.



Identifying peninsula and island issues in the GND shape

These peninsulas and islands can cause problems due to AC and transient voltage characteristics and should be avoided. Power delivery shapes should also have connection points on all their major sides.

You will also notice in this view that the current flowing from left to right is limited to narrow strips above and below **U1** in the design. If the total current travelling in this design was significant, that would be problematic and the voltage on the ground plane would be significantly higher than the **1.17mV** on the design. Viewing the ground shapes using the current density display can give valuable insights into a design's layout.

Example 2 Setup: VCCO (3.3V)

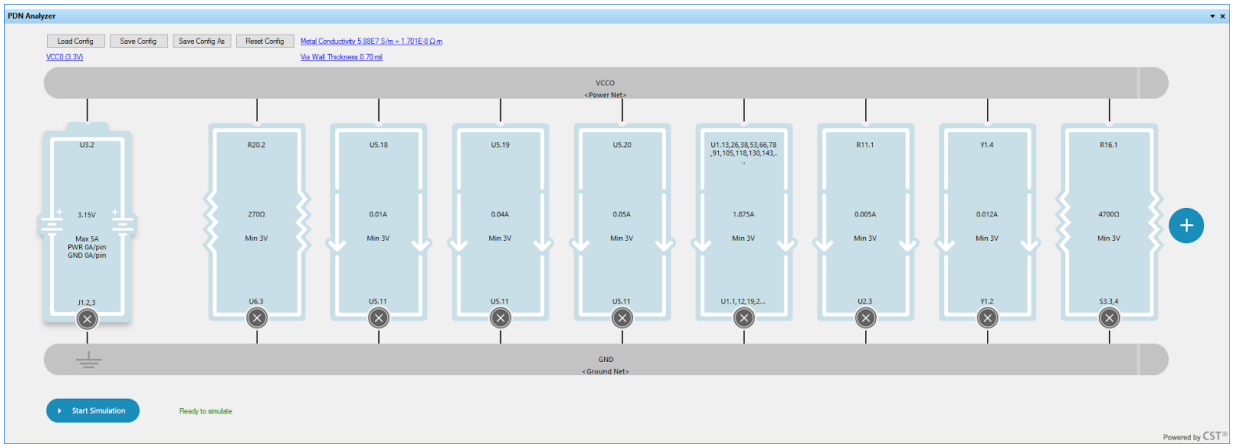
This example demonstrates the following features in PDN Analyzer:

- The ease of adding multiple loads to a simulation.
- The value of a graphical representation of a simulation topology to ensure accurate entry of parameters.
- The ability to assign different current values to particular pins for a load device (U5, in this case).

Follow the steps below to complete the setup for this example:

1. Run a similar exercise for the **SpiritLevel VCCO (3.3V)** power and ground nets. In the **PDN Analyzer** window, save your current configuration and then press reset to clear that configuration.
2. Enter the following settings, using the **+ symbol** to add additional loads as needed:

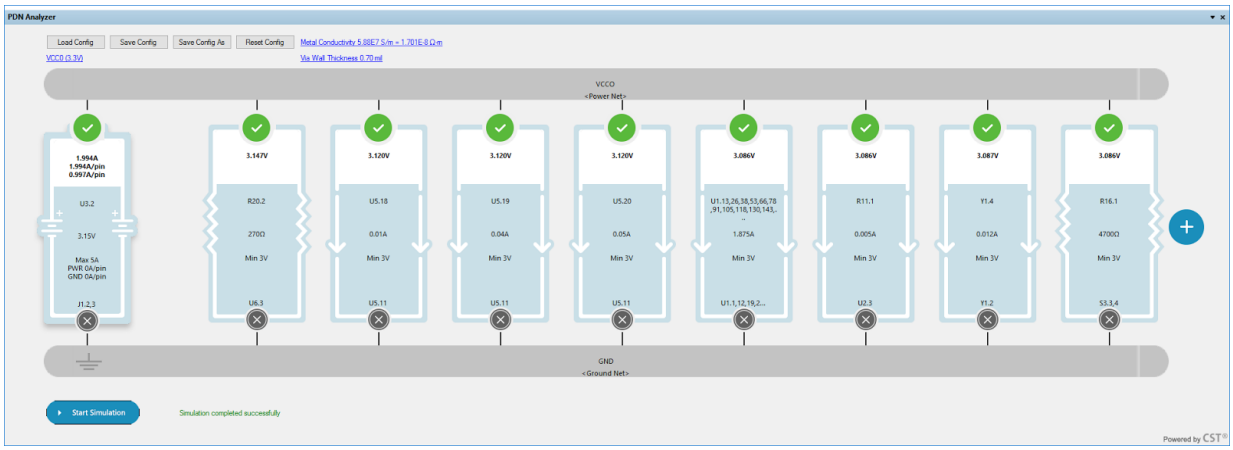
Power Settings	**PWR net (source and loads)**: VCCO **Ground net**: GND **Source**: U3.2 (power), J1.2,3 (ground) • 3.15V (3.3V – 5%), assuming 5% derating • Maximum of 5A through source and all source pins
Load Settings	**R20.2 (power), U6.3 (ground)**: Done LED • 270Ω • 3V minimum voltage (3.3V – 10%) **U5.18 (power), U5.11 (ground)**: JTAG VCCINT • 0.01A • 3V minimum voltage (3.3V – 10%) **U5.19 (power), U5.11 (ground)**: JTAG VCCO • 0.04A • 3V minimum voltage (3.3V – 10%) **U5.20 (power), U5.11 (ground)**: JTAG VCC • 0.05A • 3V minimum voltage (3.3V – 10%) **U1.* (power, use all available pins), U1.* (ground, use all available pins)**: FPGA 3.3V • 1.875A • 3V minimum voltage (3.3V – 10%) **R11.1 (power), U2.3 (ground)**: U2 current • 0.005A • 3V minimum voltage (3.3V – 10%) **R16.1 (power), S3.3,4 (ground)**: Y1 current • 0.012A • 3V minimum voltage (3.3V – 10%)



VCCO (3.3V) Configuration

Analyzing the Results

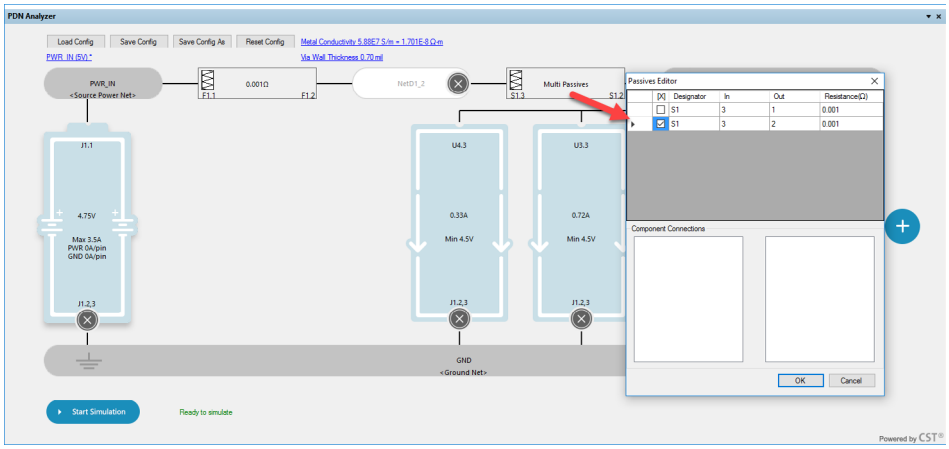
If you view the voltage on the ground plane, you'll find there is **5.3mV** on that plane, much more than the **1.17mV** due to **VCCINT**, due to the larger current of the **VCCO** net. Also note that resistors don't report voltage values and pass/fail of those values compared to parameters.



VCCO (3.3V) Results

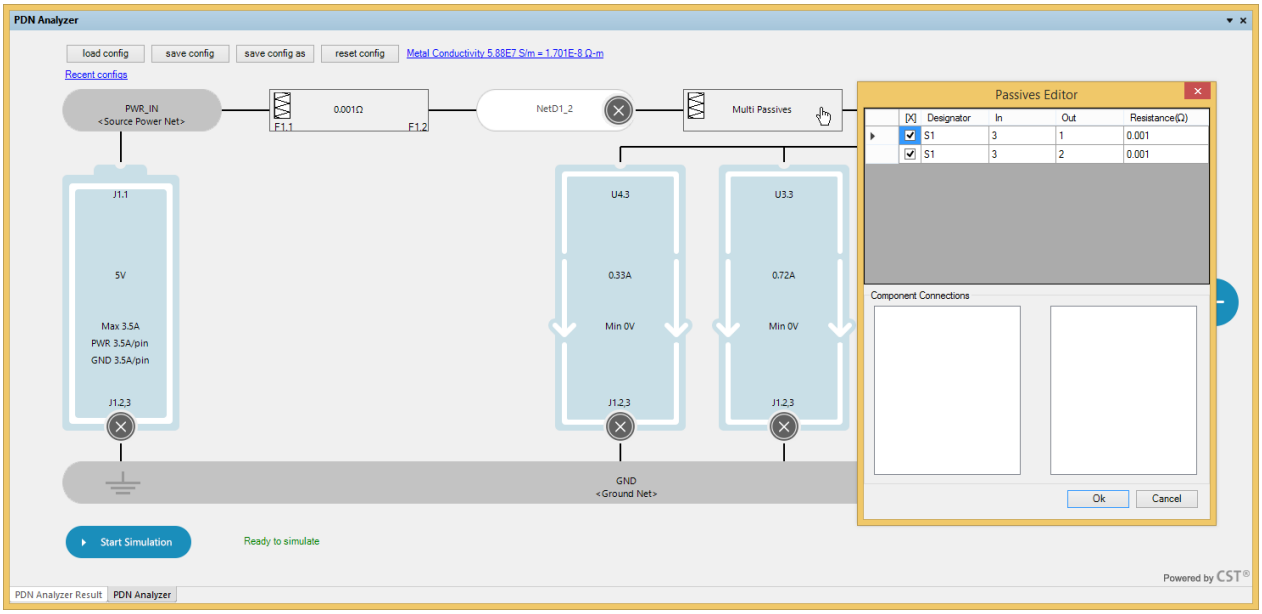
Example 3 Setup: PWR_IN (5V)

1. The **SpiritLevel 5V** (net name **PWR_IN** from the **J1** connector) can be easily analyzed by selecting **PWR_IN** as the source power net and **5V** as the load's power net. **PDN Analyzer** automatically constructs the DC path between the two nets, including the intermediate net **NetD1_2**.



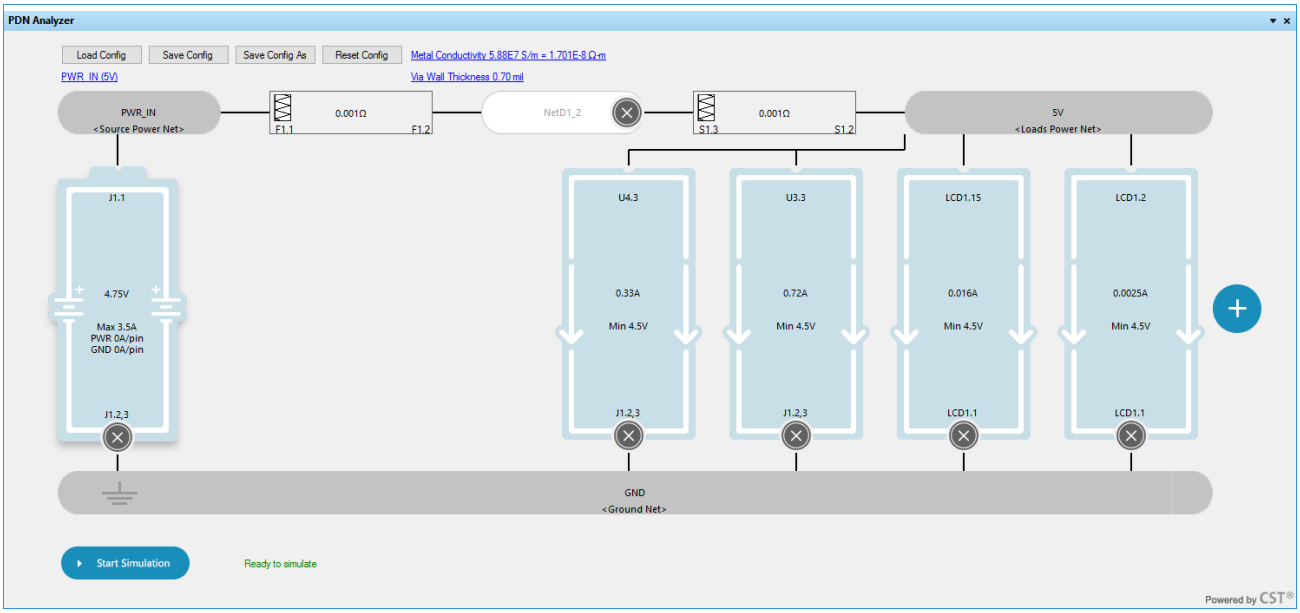
Proper NetD1_2 to 5V Path Settings for PWR_IN (5V)

2. Multi Passives (**S1.3-S1-2, S1.3-S1.1**) between **NetD1_2** and **5V** should be changed to only **S1-3** to **S1-2** to be precisely accurate and to arrive at the configuration shown in the figure below.

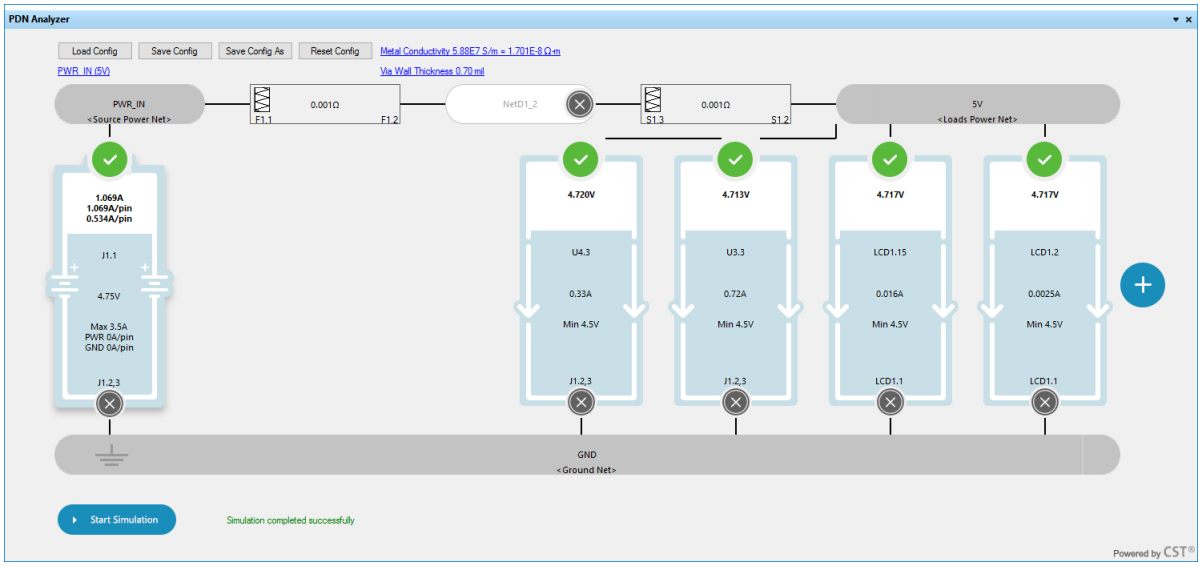


Changing multi passive designators between S1-3

Analyzing the Results



Final PWR_IN (5V) Configuration



PWR_IN (5V) Results

PWR_IN = 5V: demonstrates the ability to use a different net at the source and loads, going through passive components (those that can be modeled as a resistor only). Paths through active components need to have the input and output paths of those active components modeled separately. The path from the source and load nets is automatically derived.

Notice that the voltage on the ground plane due to **5V** current delivery is only a maximum of **11µV**, compared to **1.17mV** for **VCCINT** and **5.3mV** for **VCCO**. This is due to the large amount of ground shape between the source and the major loads, **U3** and **U4**.

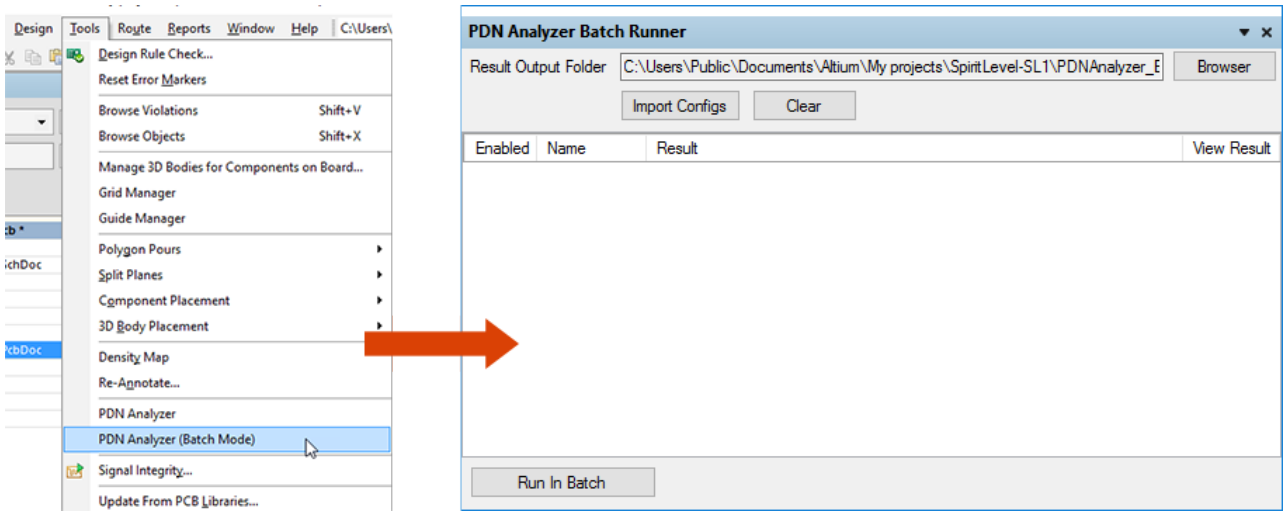
Batch Simulation Example:

Batch Mode allows the user to queue several saved configurations and run them in batch. The working files and results of these runs will be kept separately from other results, in the **PDNAnalyzer_BatchResults** folder and in a subfolder named after each configuration file.

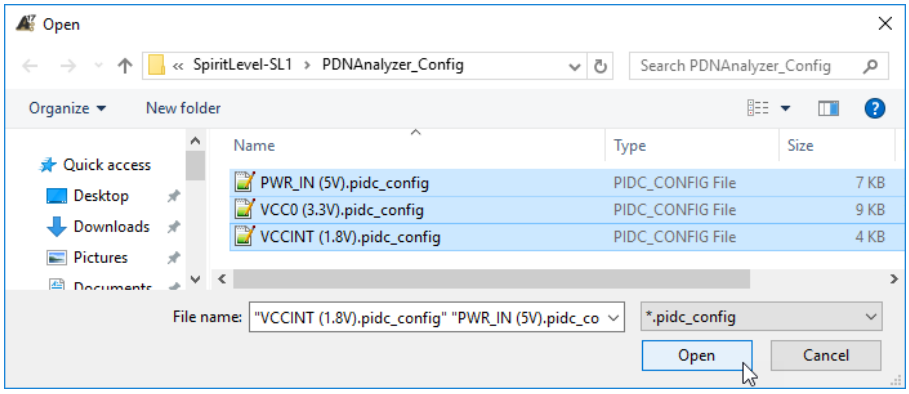
Batch Mode Launch & Setup

1. With the **PcbDoc** in front in Designer, choose **Tools >> PDN Analyzer (Batch Mode)**.

The **PDN Analyzer Batch Runner** interface opens. The **PDN Analyzer** and **Results** windows open as well if they were closed. Any open configurations are not relevant at this point, as they will be opened in an independent space. You should, however make sure you have saved any work in process.

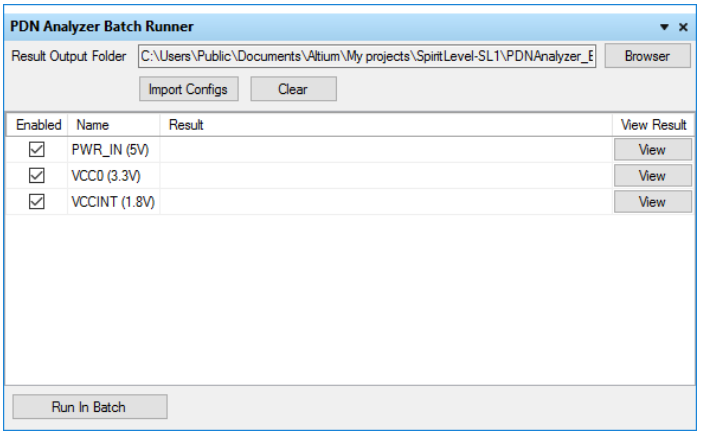


2. Select the **Import Configs** button in the **upper left** to open the file browser, and navigate to the **PDNAnalyzer_Config** folder. You should see your config files from this session in the browser window.



Selecting Multiple Config Files

3. Use Windows' **shift-select** or **CTRL-select** to select the configurations that are to be run in batch, then select **Open**. The selected configurations are loaded into the **Batch Runner**.

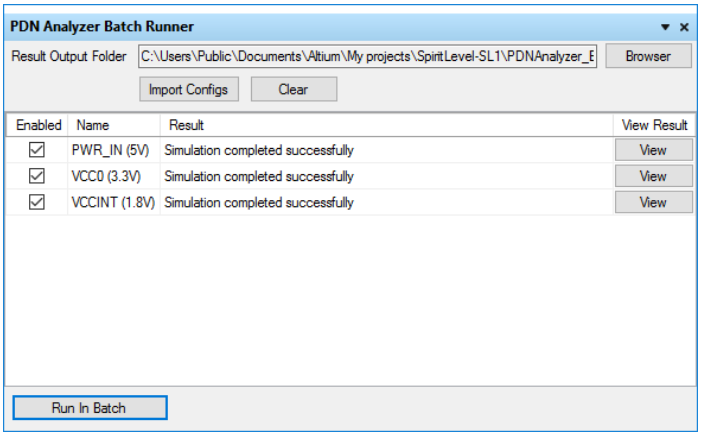


Multiple Configurations Loaded

Batch Simulation and Results

4. Select **Run In Batch** to kick of the series of simulations. The **Batch Runner** will keep you up-to-date on the progress through completion of the batch run. When done, the result should look similar to the figure above.

The working files and results of each run are stored in the **PDNAnalyzer_BatchResults** folder, in a subfolder named after each configuration file.



Batch Simulations Completed Successfully

5. To view the results of a given simulation, click on the **View** button next to that item. The configuration is quickly opened in the **PDN Analyzer** canvas and the **Results** window and **PcbDoc View** are updated per the options.

CONCLUSION

Having gone through these examples, you should now be familiar with setting up, saving, executing, and analyzing **PDN Analyzer** simulations within **Altium Designer**. The design process is a long road with many stops. The last thing you want to do is restart your design process for PDN issues. Incorporating PDN analysis into your design process makes the transition from concept to production simple. At the beginning of this guide we asked two questions:

1. How do you currently ensure that adequate copper has been provided from your voltage sources to your loads?
2. Are the planes providing the voltages wide enough to not starve the loads?

With **PDN Analyzer**, these questions will no longer go unanswered until you have you have a physical prototype or lengthy simulation process. Using robust simulation technology powered by CST®, the PDN Analyzer extension puts the power of advanced analysis technology in the hands of every PCB designer, regardless of experience level. **PDN Analyzer powered by CST®** makes it easy to identify **IR Drops** and **Current Density** in the **PCB Layout**. Optimizing your PDN at design time has never been easier with this new technology in the **Altium Designer** unified environment.

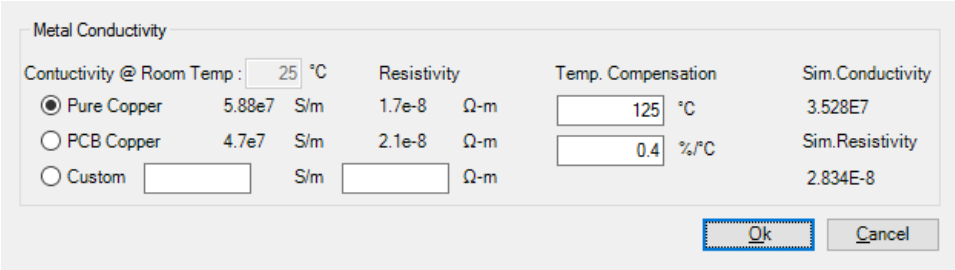
APPENDIX

Metal Conductivity Details

When the **Metal Conductivity** option is selected, it allows you to set the values for the conductivity (1/resistivity) of the metal used in a design. Keep the points below in mind when configuring your connectivity settings:

Metal Conductivity 5.88E7 S/m = 1.701E-8 Ω-m

- The default assumes **Pure Copper** which typically is assumed to have a conductivity of **5.88e7 S/m at 25°C** and a conductivity thermal coefficient of **0.4%/°C**. Notice that raising the Temp. Compensation temperature from **25°C** to **125°C** (**100°C delta**) will lower the simulation conductivity **40%**, to **3.53e7 S/m**, for instance.



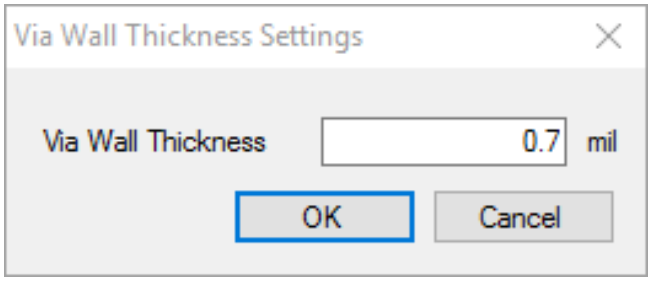
Configuring conductivity settings for various copper types

- **PCB Copper** reflects conductivity values reported in industry literature as more representative of the metal found in **PCB Electro-deposited** (**ED**) copper, measured to be **4.7e7 S/m** at **25°C**, with a thermal coefficient of **0.4%/°C**.
- The **base conductivity** (or **resistivity**), **temperature coefficient**, and/or **temperature** can be modified to reflect a design's metal properties. The **Sim Conductivity** represents the final conductivity value after taking into account all parameters.

Via Wall Thickness

When Via Wall Thickness button is selected, you have the opportunity to define the thickness of the barrel portion of the via.

1. The **barrel material** is the same as specified in the **Metal Conductivity** form.



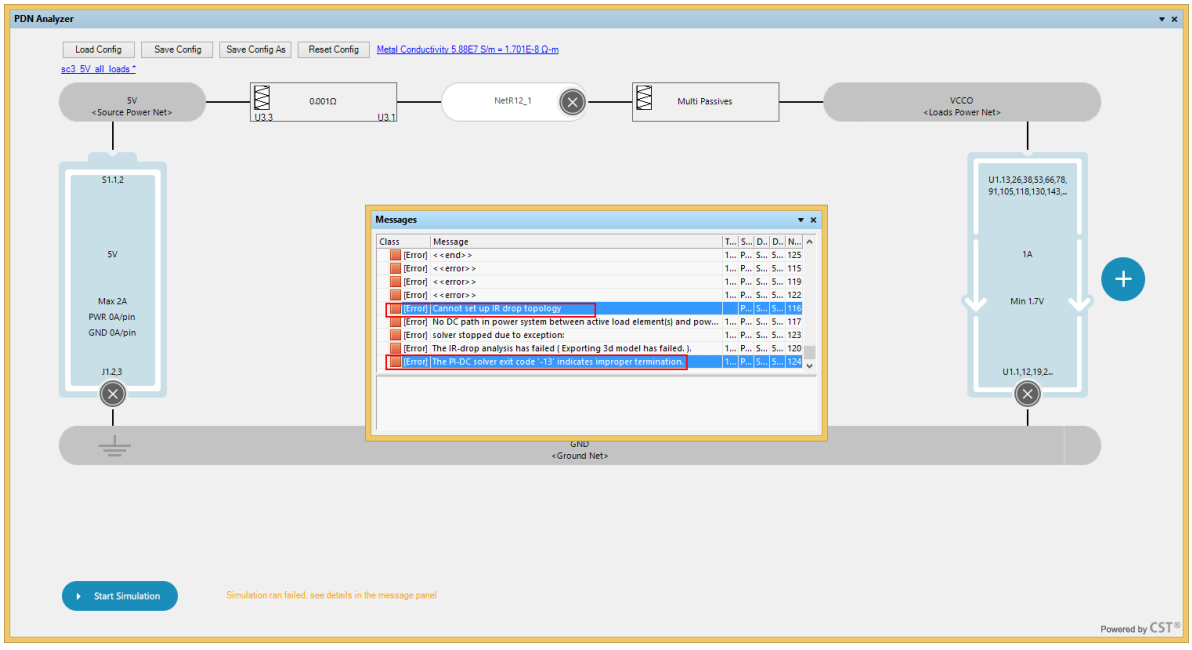
Via Wall Thickness

Common Errors and Warning Conditions

When the source and load are connected to different power nets, you will find that the signal path will automatically simulate the components that bridge the two nets. Typically you will have a series of passive components, however, unexpected active components in the path will result an ambiguous topology, multiple nets, or an invalid path. In such cases, you will encounter conditions where the topology or path cannot be correctly determined. This commonly results in the error class **Cannot set up IR drop topology**, followed by an **exit code -13**, or similar as shown below:

```
[Error]   PDN Analyzer   Cannot set up IR drop topology
[Error]   PDN Analyzer   The PI-DC solver exit code '-13' indicates improper termination
```

Should this occur, carefully reconsider the source and destination nets, as well as, components so that the proper path from the source to all loads can be recognized. An example of this is shown in Figure 27 below where the source to load path propagates through a voltage regulator. The simulation result will terminate early with errors as shown. The correct approach is to instead specify the voltage regulator output as the source, keeping in mind the analyzer is not intended to trace through active components.



A source to load path propagating through a voltage regulator, resulting in errors

Note: If you encounter similar error conditions with a different exit code number, please contact Altium Support for troubleshooting.