

Error Checking To Avoid Disaster



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ERROR CHECKING TO AVOID DISASTER

PCB design has become increasingly complex—now containing even more rules with regards to electrical requirements and configurations. The PCB Editor in Altium Designer® has some ways to verify that you are following these requirements, but if you manage to somehow step outside of them, you run the risk of creating an error. This paper highlights key tools that will help you keep track of violations in real time or identify where a violation may have occurred.

DESIGN RULES

Design rules collectively form an instruction set for the PCB Editor to follow. Each rule represents a requirement of your design and many of the rules, (e.g., Clearance and width constraints can be monitored as you work by the online Design Rule Checking (DRC). Certain rules are monitored when using additional features of the software, for example routing-based rules when using the Situs autorouter to route a design, or signal integrity-based rules used by the signal integrity analyzer when performing a detailed signal integrity analysis of a design.

ONLINE DESIGN RULE CHECKING (DRC)

DRC is a powerful, automated feature that checks both the logical and physical integrity of your design based on the rules configured within your design rules. Altium Designer takes it one step further with the online DRC, which checks your work against these rules in real time, as you are working within the PCB environment.

This is important because saves you hours of work and re-work. Without some real-time analysis, you could get down the road in wiring an 18-layer high-speed board and realize that you've had the wrong trace thickness on inner layers.

The online DRC can be turned on and managed from your DXP preferences by going to **DXP»Preferences»PCB Editor» General**. You may further manage and become familiar with the DRC Violations Display under **DXP»Preferences» PCB Editor» DRC Violations Display**.

The default examples in Figure 1 may help you quickly identify the source of the violation that is being displayed:

Some examples of graphical violations include net antennae, short circuit, room definition, layer pairs and Vias under SMD rules that do not have a value assigned to them; they are simply flaws in the design configuration and need to be reviewed. Many of these are turned on in Altium Designer but are managed in the design rules portion of the design.

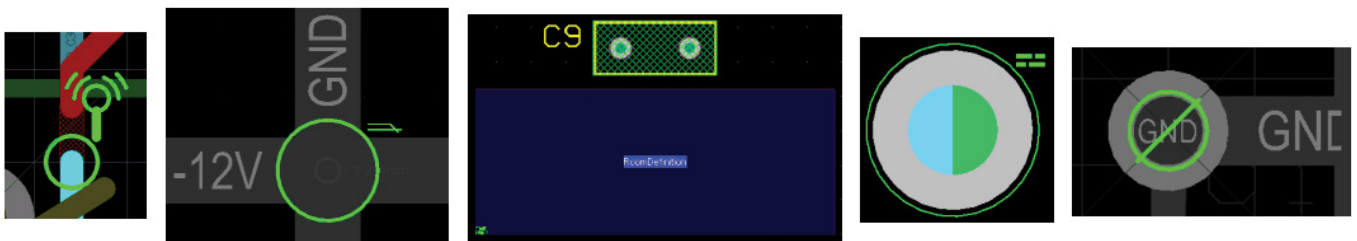


Figure 1. Graphical indications of violations occur as no definable constraint values are being violated.

ERROR CHECKING TO AVOID DISASTER

Figure 2 is an example where a defined constraint value is not being met. When this occurs, it helps to know which value is not met and identify which rule is being violated.

If you were to perform a task that creates a violation while the online DRC is active, then error markers are used to highlight an offending primitive. An example of this error marker is in Figure 3. This can be managed under **DXP»Preferences» PCB Editor» DRC Violations Display**.

METHODS USED FOR RESOLVING ERRORS

Some errors may occur that are not as visible as those described above. Sometimes, even when they are visible, it's hard to identify the cause of the error. The methods below may help to understand further why Altium Designer is indicating/reporting an error.

DRC

The standard operating procedure to verify your design is to run a DRC, which is done by going to **Tools»Design Rule Checking** and then clicking on **Run Design Rule Checking**. Running the DRC report (Figure 4) generates a couple of results.

It will create an HTML report that is linked to the PCB and contains hyperlinks directly to the violation. Also, the errors are reported in the messages panel, which opens by default. From the Messages panel (Figure 5), you can double-click a violation to jump to it in the PCB and zoom to have further review of the error.

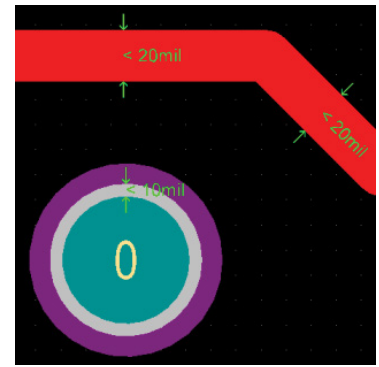


Figure 2: As you can see above, there is an indication that the expected width does not meet the design rule and a violation is shown. The trace width and paste mask do not meet the minimum width rule.

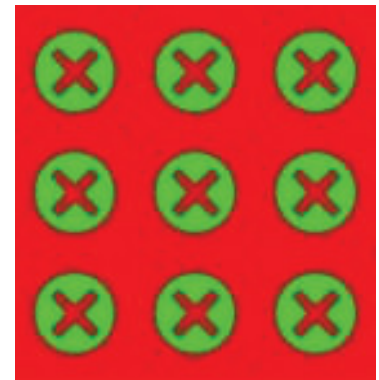


Figure 3

Warnings		Count
Total		0

Rule Violations		Count
Net Antennae (Tolerance=30mm) (All)		0
Silk to Silk (Clearance=0mm) (All)(All)		0
Silk To Solder Mask (Clearance=0.1mm) (IsPad)(All)		0
Minimum Solder Mask Sliver (Gap=0.1mm) (All)(All)		0
Hole To Hole Clearance (Gap=0.1mm) (All)(All)		0
Hole Size Constraint (Min=0.025mm) (Max=2.54mm) (All)		0
Height Constraint (Min=0mm) (Max=25.4mm) (Preferred=12.7mm) (All)		0
Component Clearance Constraint (Horizontal Gap = 0.2mm, Vertical Gap = 0.2mm) (All)(All)		0
Width Constraint (Min=0.1mm) (Max=0.5mm) (Preferred=0.1mm) (All)		0
Power Plane Connect Rule(Relief Connect) (Expansion=0.508mm) (Conductor Width=0.254mm) (Air Gap=0.254mm) (Entries=4) (All)		0
Clearance Constraint (Gap=0.1mm) (All)(All)		0
Un-Routed Net Constraint (All)		0

Figure 4: Design Rule Checking (DRC) Report

ERROR CHECKING TO AVOID DISASTER

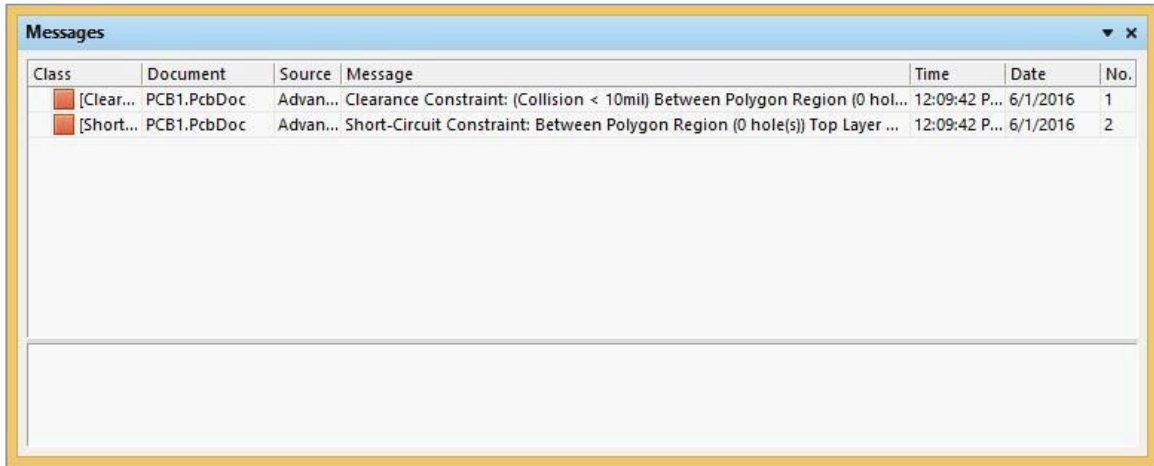


Figure 5: Messages Panel

Heads-Up Display

The **Heads-Up Display (HUD)** in Figure 6 is visible by default and can display violation details simply by hovering over a violation. The display reports the violated rule, the object or objects involved in the violation, and the layer of the violation.

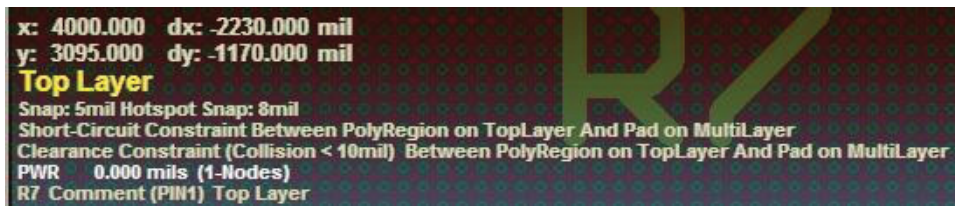


Figure 6

Board Insight Panel (Shift + V)

Another trick while hovering over the violation is to press the shortcut keys **Shift + V**, and this will load the **Board Insight** panel (Figure 7) to display the violation. The advantage of loading this panel is that the objects become selectable and you may view the object properties, select the object or zoom in on the object to take a closer look at the violation.

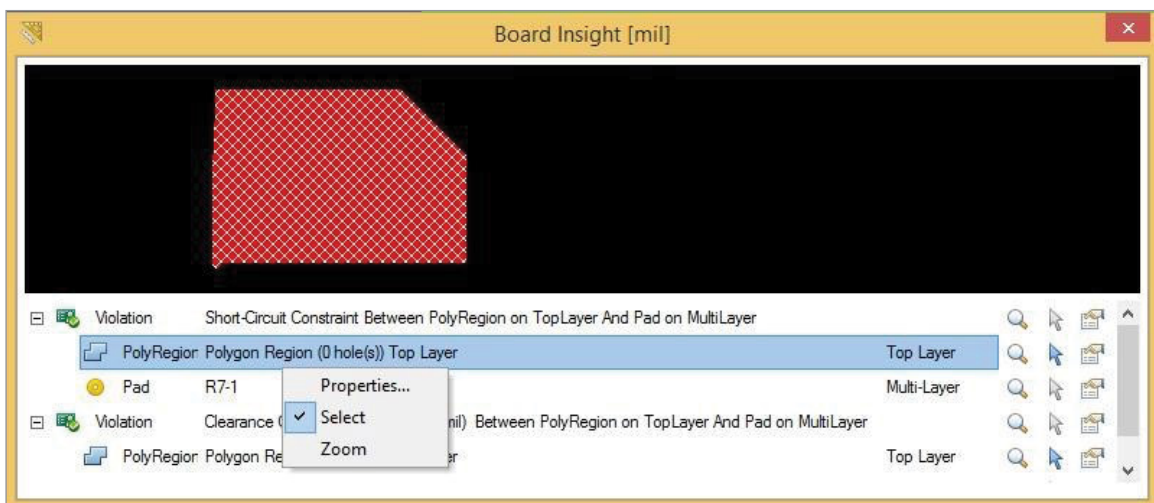


Figure 7

ERROR CHECKING TO AVOID DISASTER

PCB Rules and Violations

Alternatively, you can open the **PCB Rules and Violations** panel (Figure 8), which displays the violations in real time. The PCB Rules and Violations panel shows all the violations and allows you to jump to them by double-clicking the violation and choosing **Jump**. The panel displays the violation information, and also the X, Y location of violations, to provide more details about the violations and where they occur. Also, when you choose the violation and look at the **Violation Details** window, it indicates which rule is violated in the **Violated Rule** section, which is helpful if you need to review the rule.

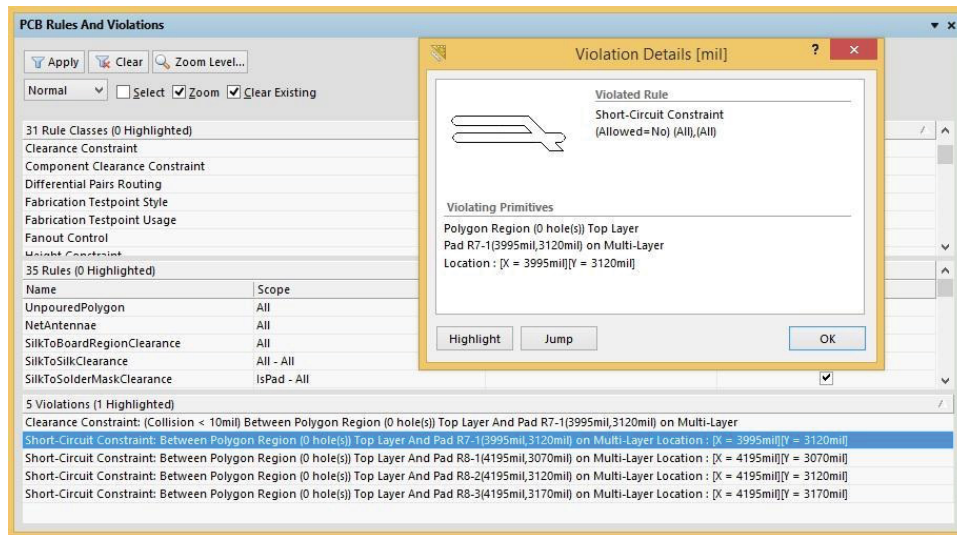


Figure 8

Applicable Unary Binary Rules

If you want to take a look at the rules that are applied to an object(s), you can use the right-click menu to check **Applicable Binary Rules** (Figure 9) and **Applicable Unary Rules** (Figure 10). If you are looking at the rules that are applied to an individual object or primitive, you would right-click and choose **Applicable Unary Rules** and then select **Object**. If you would like to compare the rules that affect two objects or primitives, you would choose **Applicable Binary Rules** and then select **Both Objects**.

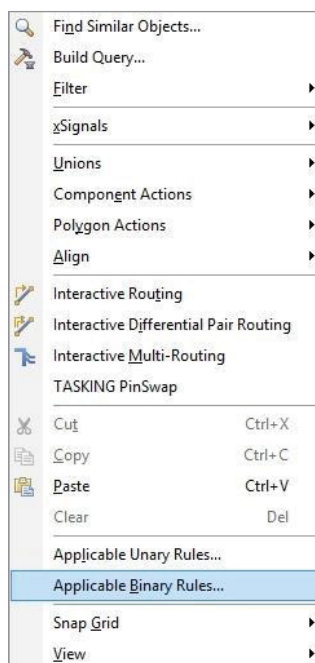


Figure 9

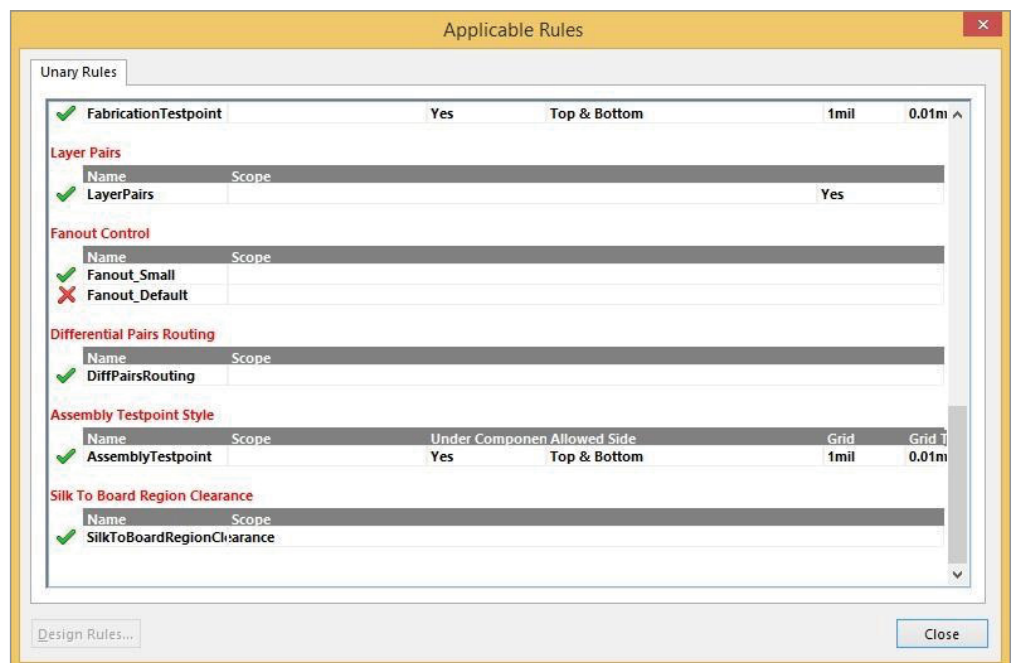


Figure 10

ERROR CHECKING TO AVOID DISASTER

The advantage to this is it shows all applicable rules and if there is a **green check** next to it, then it's valid. However, if there is a **red X**, then it indicates the rule is violated. Also, if more than one rule is available, the rule on top is the rule applied.

CONCLUSION

If we do not obey the rules of the road, or follow the signs on the freeway, we can miss our goal, or worse, experience a disaster. The rule system of Altium Designer allows you to reach your goal and avoid disaster. Managing and using these tools will help you keep on track to efficiently produce quality design. The Altium Designer error checking systems guide you on your way to success, so don't ignore the warnings!

USEFUL LINKS

Altium Tech Docs:

- **Design Rules**
<https://techdocs.altium.com/display/ADOH/Design+Rules>
- **Design Rule Checking**
<https://techdocs.altium.com/display/ADOH/Design+Rule+Checking>
- **Enhanced Display of DRC Violations**
<https://techdocs.altium.com/display/ADOH/Enhanced+Display+of+DRC+Violations>
- **PCB Rules and Violations**
[https://techdocs.altium.com/display/ADRR/PCB_Pnl-PCBRulesAndViolations\(\(PCB+Rules+and+Violations\)\)_AD](https://techdocs.altium.com/display/ADRR/PCB_Pnl-PCBRulesAndViolations((PCB+Rules+and+Violations))_AD)
- **Unary and Binary Rule Types**
<https://techdocs.altium.com/display/ADOH/Unary+and+Binary+Rule+Types>
- **Applicable Unary Rules**
[http://techdoc.altium.com/display/ADRR/PCB_Dlg-ApplicableUnaryRules\(\(Applicable+Unary+Rules\)\)_AD](http://techdoc.altium.com/display/ADRR/PCB_Dlg-ApplicableUnaryRules((Applicable+Unary+Rules))_AD)
- **Applicable Binary Rules**
[http://techdoc.altium.com/display/ADRR/PCB_Dlg-ApplicableBinaryRulesDlg\(\(Applicable+Binary+Rules\)\)_AD](http://techdoc.altium.com/display/ADRR/PCB_Dlg-ApplicableBinaryRulesDlg((Applicable+Binary+Rules))_AD)