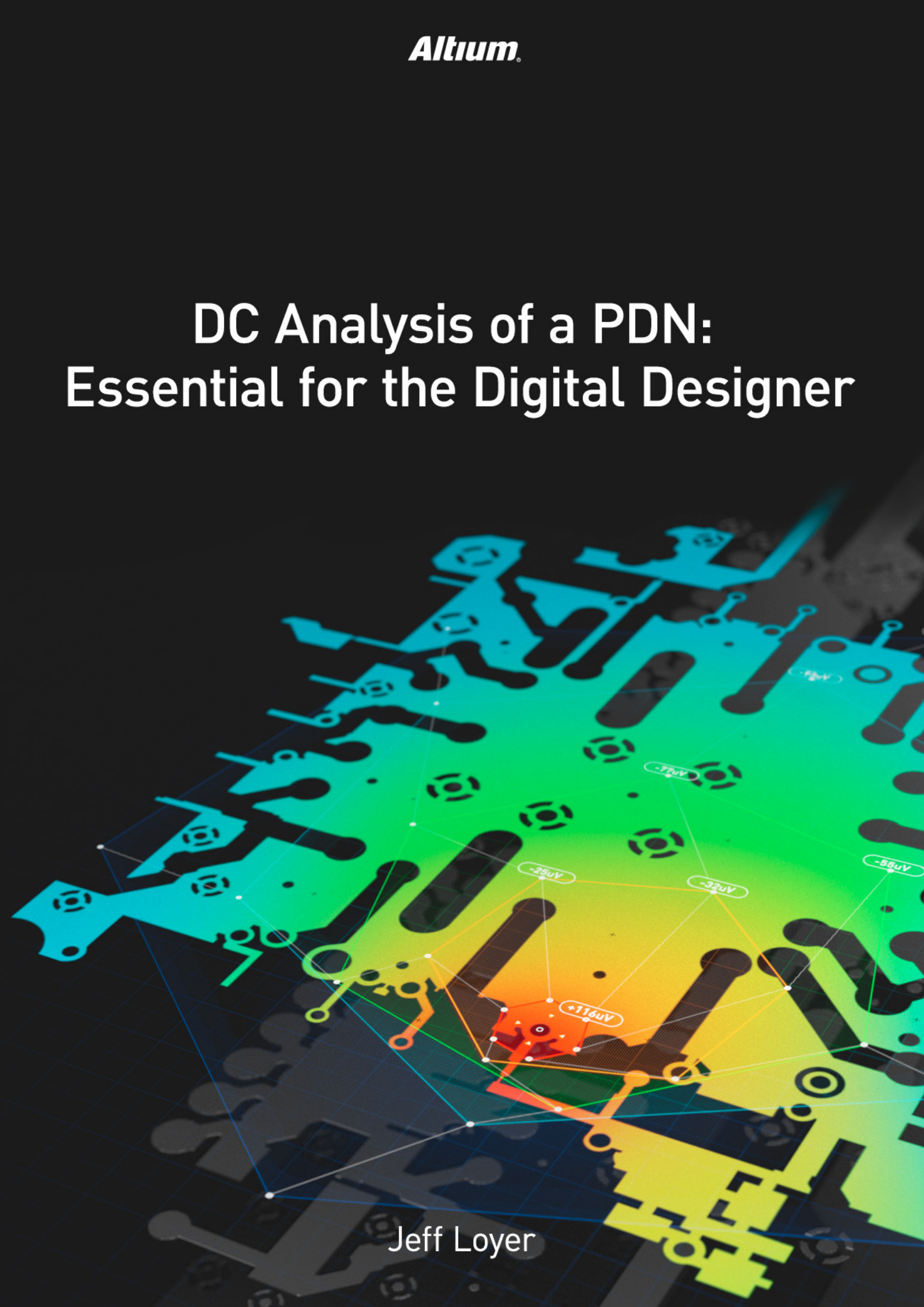
Altium

DC Analysis of a PDN: Essential for the Digital Designer



Jeff Loyer

DC ANALYSIS OF A PDN: ESSENTIAL FOR THE DIGITAL DESIGNER

INTRODUCTION

DC analysis of a power delivery network ("PDN"), commonly referred to as "IR drop", "DC power integrity", or "PI-DC", answers some fundamental questions that every digital (or analog) designer should ask and answer:

- Have I provided enough metal between my sources and loads to deliver adequate voltage to every load?
  - Enough power and ground shapes?
  - Enough vias, and are they large enough?
- Can I cleverly optimize my PDN shapes?
- What part of my design is most likely to heat (burn) up?
- Have I done something weird with my ground shapes?

Many digital designers are aware of the need for accurate signal integrity analysis, or how essential it is to understand the AC aspects of their PDN ("How many decoupling capacitors do I need?", for instance), but give little regard to their DC PDN ("PI-DC") analysis. PI-DC analysis is also critical, however, since it can provide critical insight into a design's quality and save valuable design real estate and layers, ensuring a cost-effective digital design. The fundamental question it answers is relatively straightforward – have I provided enough metal (in our case, almost exclusively copper) between my power source and all the loads to deliver adequate power to those loads? But, in today's world of small, integrated designs, answering that question accurately can mean the difference between success and failure.

Not long ago, digital design was dominated by large form factors – desktop personal computers and large servers, for instance. In those designs, entire metal layers could be dedicated to power delivery, ensuring minimal voltage drop between the source and loads. Conservative rules of thumb could be used to estimate how much metal was needed with little consequence if more than enough area was dedicated to power delivery. A digital designer only ensured the DC power delivery was "adequate," with little thought about optimizing the power delivery shapes to minimize their area and layers.

Those days are gone – even server designs are becoming incredibly dense and board real estate is a valuable commodity that can't be wasted with overly conservative design practices. Now all metal dedicated to power delivery must be "necessary", we don't have the luxury of additional layers or board size. PI-DC analysis provides a sophisticated means of ensuring the power delivery metal is not only adequate but necessary.

DATA PROVIDED BY PI-DC TOOL

The first data a PI-DC tool provides is the voltage drop from the source to the loads due to the resistivity of the power net. We can no longer assume it is zero due to an infinitely large power "plane." As we shrink designs, the concept of power "planes" may not apply. While we may have a layer primarily dedicated to power delivery, that layer will probably be broken up into many sections (nets) delivering unique voltages around the design. PI-DC tells us how much voltage drop is induced in each net, allowing us to allocate the proper area to each voltage net. **Figure 1** shows a typical 3-D voltage plot of a 1.8V power shape from its source (U4, a VRM) to the load (U1, an FPGA) along its 2-layer path (vias are hidden in this view). Careful scrutiny of the voltage plot would show:

- Only 10mV of drop between U4 (1.7V, was derated by 5% from the nominal 1.8V) and U1 (1.69V).
- The single track from U4 to the FPGA voltage ring is the largest source of voltage drop.
- There is voltage drop from some of the vias – the color of the net at the top of some vias is different than the bottom.
- There is no DC voltage drop between the source and the decoupling capacitor, C3, as expected. Capacitors are treated as "open" for DC analysis.

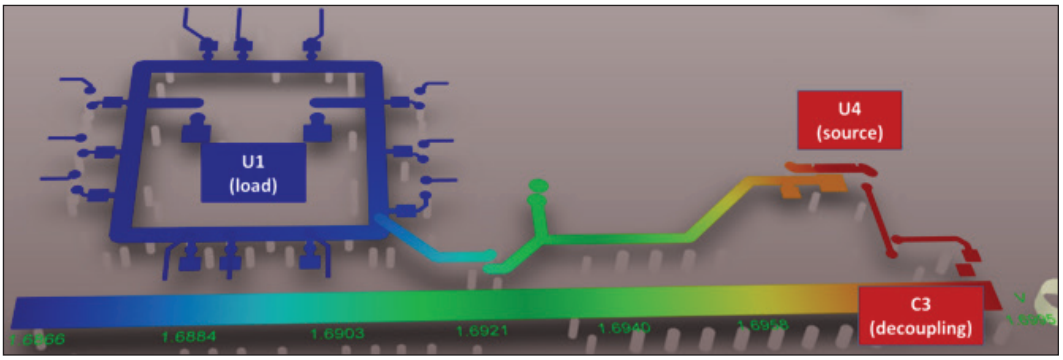


Figure 1: Voltage plot from power source (U4) to single load (U1, an FPGA)

A PI-DC tool will also report the current densities ("J") within the shapes of interest, allowing a designer to focus on making corrections to those areas with the highest current density ("pinch points" w/ Jmax), if necessary. Notice that this plot confirms what we concluded from the voltage plot, perhaps showing it in a more straightforward manner for some considerations. Unfortunately, there is usually no single threshold value to set as a limit for current density, so only relative values are often used. The thermal performance will depend not only on current density but the thermal dissipation of the system and even the cross-section of the shape, as demonstrated by Doug Brooks and Johannes Adam in their paper "Trace Currents and Temperatures Revisited" (Doug Brooks, n.d.).

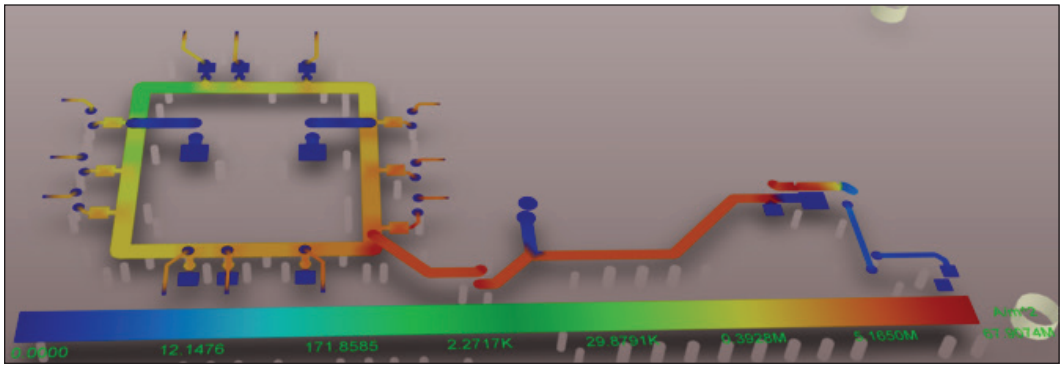


Figure 2: Current density plot of power net between power source (U4) and single load (U1, an FPGA)

Without a PI-DC tool, the designer will probably use conventional rules dictating a particular width, based on the current the power delivery shape is carrying. There are at least two problems with that approach:

1) Using the same minimum width independent of the distance between the source and load(s) doesn't often make sense – you don't use the same gauge wire for 6 foot and 100-foot extension cords, for instance.

2) Using that same width along the entire length of the shape not only wastes board real estate, but it also doesn't represent the most efficient design of the power delivery shape.

The results from a PI-DC tool will allow a designer to properly size their power delivery shape based on length, and narrow the power delivery shape for short distances where necessary and compensate for those constrictions by widening the shape where board real estate is more available. A PI-DC tool is critical for finding the optimum shape of power delivery nets.

Also, nowadays ground shapes can no longer be assumed to be infinite – today's designs usually force limits on how much area can be allocated to ground. Those restrictions on ground area can cause significant voltages on "ground", we can't assume it's zero any more. And, the problem of voltage on ground is more complex than for power nets – the actual voltage on any point on the ground net will be a superposition of the voltages induced by the currents from the various power nets.

For instance, a design may have both 1.8V and 3.3V being delivered to a device. While the voltages on the two power nets are theoretically independent, the device will see a voltage on its ground pins which is the addition of the voltages induced by the 1.8V and 3.3V currents. It's essential to understand and model that relationship accurately. The good news is that, for DC, the superposition is fairly straightforward, and mere addition (or subtraction, for supplies of opposite polarities) is adequate. But a designer should be aware that the ground shape size at any point will have to accommodate currents from multiple sources, whereas the power shape sizes are more straightforward.

A PI-DC tool should be capable of providing the DC voltage for a device using the ground voltage at that device as the reference voltage. The voltage relative to an arbitrary "ground" point (such as the voltage source) is often meaningless. The currents in the ground shape may induce significant voltage on the ground net, and this must be comprehended in the DC analysis of the power delivery network.

A PI-DC tool also gives valuable insight into how many vias are needed, and how large, for power delivery. While this seems a trivial exercise, power vias typically consume valuable real estate on all layers, blocking routing on layers above and below their assigned power layers, and using too many or excessively large vias is a luxury today's designs can't afford. An especially ironic result of being overly conservative in power delivery via allocation is that those vias may perforate another power or ground plane, causing more problems for the design than they solve.

COMPREHENDING TEMPERATURE EFFECTS

Something that most PI-DC tools won't directly provide are the thermal effects of your current – how much they heat up the metal. This can be critical given the I2R relationship between current and power – even a small resistance can dissipate large amounts of energy if the current is high, leading to local hot spots and associated failures of the dielectric materials or conductors. But, PI-DC tools do provide information on the current density of power and ground shapes, allowing designers to optimize for low current density and therefore lower power dissipation.

IPC spec. 2152 (previously 2221) provides guidance on avoiding issues by providing minimum trace widths for acceptable temperature rise. PCB designers often misuse this, entering very conservative temperature rise values (1°C, for instance) and then using the corresponding wide trace width as the minimum width for their entire PDN shape from source to all loads. Applying the spec. that way forces the designer to allocate more area to power delivery than is necessary, consuming valuable design real estate or requiring more layers for the design. In order to create the most efficient power delivery design, IPC-2152 should be well understood, not applied blindly. The designer who applies the spec. more thoughtfully, along with taking advantage of the information a PI-DC tool provides, can reduce the PDN area while ensuring a safe design.

Instead of using an arbitrarily low allowed temperature rise value when applying IPC-2152, the digital designer should use a value representing a temperature rise that the dielectric material and metal can accommodate without risking damage or failure. For instance, **Figure 3** demonstrates how allowing a 45°C temperature rise instead of only 1°C permits the designer to reduce their minimum trace width from 0.3" (red) to only 0.02" (blue) for a 2A current on 1-oz. copper. A PI-DC tool can then be used to ensure that the voltage requirements of all the loads are met when that minimum width is used.

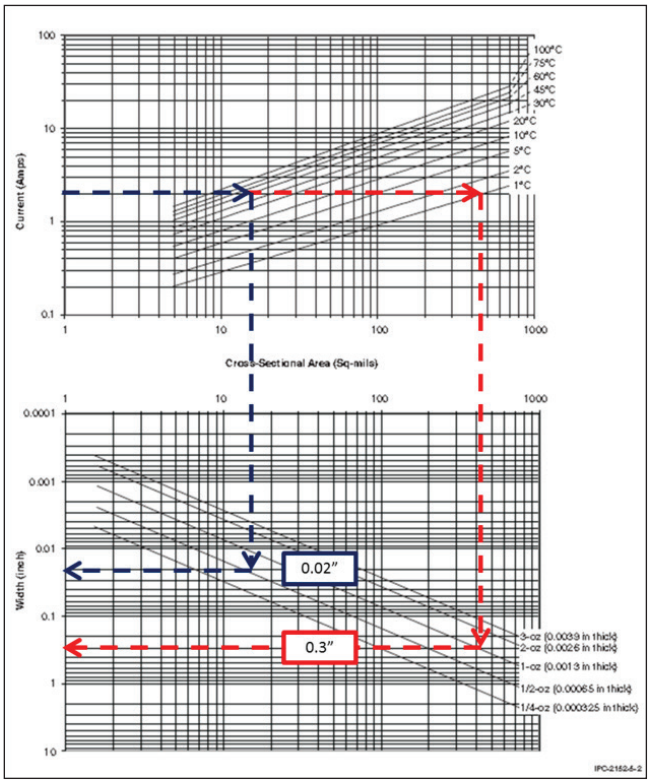


Figure 3: Reducing trace width from 0.3" to 0.02" using IPC-2152

Unfortunately, the thermal issue is very complicated and even having a thermal simulation tool available might provide only limited insight due to the complexity of the problem[1]. An accurate answer requires accurate models for the myriad of components contributing to the thermal performance of the system such as PCB material, numbers of layers, copper density, heat generation and dissipation of the various components, airflow around the design, ambient conditions, etc. A digital designer will generally be forced to be conservative, but should take some critical aspects into account when considering thermal effects:

- Not all designs are the same thermally. A design known to reside in a cool environment with low power components should require less accommodation for thermal effects than one consuming lots of power in a very hot enclosure, for instance.
- Not all areas in a design are the same thermally. Special care should be taken where heat dissipation is poorest – on outer layers and under or near very hot components, for instance. Areas far removed from hot components will typically be less subject to thermal effects since the power is more efficiently dissipated. Feeding a power-hungry device with narrow tendrils through its breakout is a recipe for disaster.
- How much is the current density increased? Heating is a function of the power consumed by the shape, proportional to IR^2. Special care should be taken of the current density plots and copper should be added where current density is maximum. As mentioned earlier, it is probably not possible to set a "maximum current density" limit since thermal effects depend on so many other factors, but PI-DC allows the designer to highlight the most likely areas of problems and gauge the relative "badness" of design areas.
- Is the shape on outer or inner layers? IPC-2152 data indicates that inner layers (stripline) dissipate heat more readily than microstrip layers (though this may depend on the amount of airflow on the trace which will increase convection cooling – there may be some microstrip traces which dissipate heat well).
- Thermal requirements will depend strongly on the material used. Flex designs (especially those which are actively flexible) will typically be less tolerant of high temperatures than rigid PCBs, for instance.
- Is there relatively cool copper nearby which will dissipate the heat better than the dielectric material(s)?

HOW TO AVOID PI-DC GIGO ("GARBAGE IN, GARBAGE OUT")

Of course, the PI-DC tool must provide accurate results if it's going to be useful. The accuracy of the tool is not only a function of the sophisticated 2 or 3D modeling engine used, but of the assumptions fed into the simulation. It is imperative that anyone using these tools be very familiar with the critical assumptions and parameters fed into the tool.

The first parameter to "get right" is the conductivity of the metal used in the design. While this seems straightforward, it is much more involved than most people realize. Most power and signal integrity tools, for instance, assume printed circuit boards (PCB's) use "copper" for their metal, with a conductivity of 5.88e7S/m. Industry data[2,3] indicates, however, that the electro-deposited "copper" used in PCBs is significantly less conductive than pure copper, only 4.7e7S/m at 25°C. If validation and simulation results differ, metal conductivity should be verified.

That conductivity must also be adjusted for the actual operating temperature of design. The conductivity of copper, for instance, drops 0.4% for every degree centigrade. The metal of a copper design operating at 125°C is 40% less conductive than the 25°C value. That difference must be comprehended in the simulation – it doesn't do any good to have a highly sophisticated simulation engine if it's operating on flawed assumptions. (Note: for designs operating at extremely low or high temperatures even the linearity of the temperature coefficient, 0.4%/°C, must be examined for the expected ranges).

Another fundamental assumption easy to "get wrong" is the size of the vias. Many PCB design tools use only a single value to represent the size of a particular via and exactly what that number represents is ambiguous. Vias are usually assumed to be solid columns, but that's often not accurate – they might not be completely filled and thus may be hollow columns, with both inner and outer diameters (I.D. and O.D., respectively). The actual cross-sectional area of the via depends on both of those dimensions – a large, but very hollow, cylinder can have less cross-sectional area than a filled smaller cylinder. For vias typically used in power delivery, most people assume that if only a single value is given for a via, that value represents the drill size (outer diameter). The via is assumed to be completely filled, or best represented by a solid column. That assumption may not be valid, giving a flawed result.

In order to understand exactly how to properly model vias, the user must know how the via dimensions are specified and what the actual implementation of those specifications will look like (what will the via look like when cross-sectioned?). Most tools won't allow a user to provide both an inner and outer diameter and only allow solid vias. If that is the case and the vias are known to be hollow in actual implementation, the via outer diameter must be adjusted to represent the proper cross-sectional area. Fortunately, finding the proper diameter for a solid column that has the same cross-sectional area as a hollow column with an O.D. and I.D. is a trivial mathematical exercise – it's merely the difference of the two, O.D. minus I.D. The challenge is to scale the vias properly when doing the simulation without having unintended consequences in the physical design.

If PCB outer layers are used for power delivery, they represent an especially troublesome item to model. The thickness of the copper on PCB outer layers is a function of the plating thickness, and that can vary significantly across the board. Be sure to measure the thickness of outer layers if they are used for power delivery and simulation results don't match lab measurements.

And finally, properly representing the loads seems straightforward at first, but is not. A designer might assume that, for a passive load like a resistor or diode, the load is best modeled as a resistor, and active components such as FPGAs should be modeled as current sinks. When they model the active components as current sinks, however, they might be tempted to probably use the maximum current (Imax) as the current draw. When performing PI-DC simulations to gauge the voltage drop of the PDN, this is hard to justify and may lead to overly pessimistic results. Maximum current draw will probably only occur when maximum voltage (Vmax) is applied. We typically simulate at the lower limits of the voltage range and the current draw should reflect that in order to get accurate simulation results. A more reasonable model for an active load during voltage drop simulations might instead be a resistor whose value is a function of the device's nominal voltage and current, Vnom/Inom.

[1] *Doug Brooks, Johannes Adam. Articles on Trace Current/Temperature/Power/Resistance. From UltraCAD: http://ultracad.com/article_temperature.htm*
[2] *Loyer, Kunze, Burkhardt. Accurate Insertion Loss and Impedance Modeling of PCB Traces. DesignCon 2013. San Jose, CA.*
[3] *Loyer, Kunze. Humidity and Temperature Effects on PCB Insertion Loss. DesignCon 2013. San Jose, CA.*

On the other hand, some designers might have maximum current density values that they are trying to avoid for thermal considerations (instead of minimum voltage levels for electrical consideration). For maximum current density simulations using PI-DC (for thermal considerations), Vmax should probably be used for sources, Rmin for passive loads, and Imax for active loads. This will give a more accurate representation of possible maximum currents.

When using a PI-DC tool, it is critical to understand all the inherent assumptions that went into the simulation and to validate those assumptions are accurate, else the results might be meaningless.

VALIDATING RESULTS

It is critical that any design is properly validated to ensure the accuracy of the simulation and the parameters fed into it. Fortunately, that is fairly straightforward for PI-DC. The voltage at each load can usually easily be measured, including using a local ground for reference. Perhaps the most challenging aspects are to: 1) find a means of ensuring all loads are consuming their maximum power when measurements are taken if the voltage on the ground shape might be a significant factor, and 2) properly comprehend the thermal effects on resistivity. Superposition might be necessary if exercising all loads simultaneously at their limits is not practical. In this case, the challenge will be to measure the voltage on "ground" at each load, relative to the same reference used in simulations. For the thermal aspect, it will be necessary to have an idea of the actual temperature of the power shapes in order to calculate the correct metal conductivity, which varies as a function of temperature. This requires instrumentation not ordinarily found in most validation labs, such as thermocouples, infrared thermometers, or IR temperature sensors.

If the measured voltages don't match simulations, each of the simulation assumptions and results must be verified. We have tried to provide enough information into how to ensure proper assumptions, but how to check the results? The most fundamental data a PI-DC tool must get right is the resistance between the source and loads, and that usually isn't directly provided. It's fairly easy to construct a test circuit that will provide a value you can compare to an actual ohm-meter measurement of a bare design, however. If the source is modeled as a 0V battery and a load is modeled as a 1A current sink, the voltage at the load directly represents the resistance between the source and load (ignore the sign of the voltage). For instance, the example below (**Figure 4**) demonstrates the results of determining the resistance between the source (U4 pin 2 for power, J1 pins 2 & 3 for ground) and the load (U1) using a PI-DC simulator.

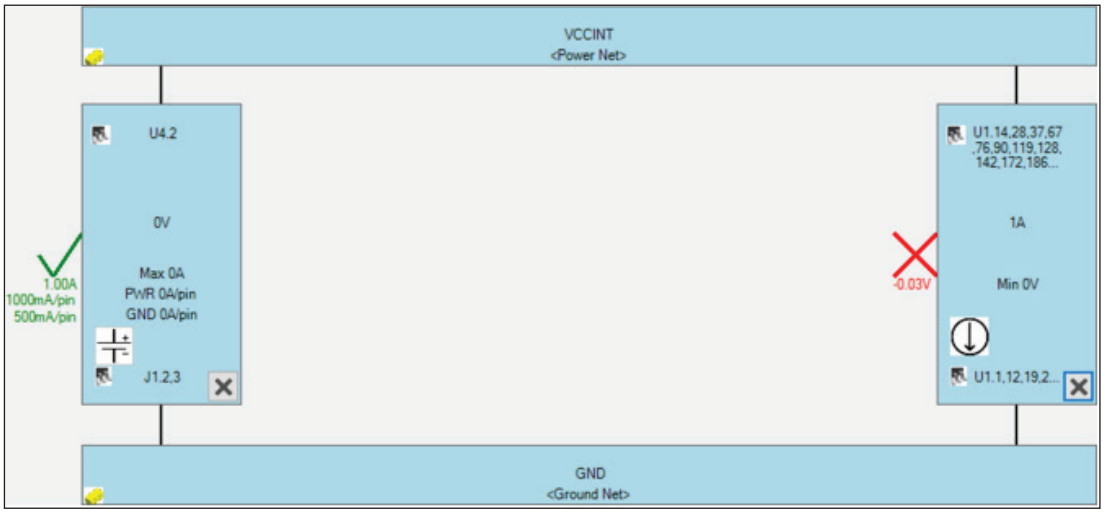


Figure 4: PI-DC setup for measuring resistance (1V = 1Ω)

The results indicate there is 30mΩ of resistance in the PDN for U1 (note the 30mV at U1 in **Figure 4**, shown as "**-0.03V**"). To confirm this in the lab, you would place a 0-ohm "short" between U4 pin 2 and J1 pins 2 & 3 (a large piece of metal, for instance), and measure the resistance between the power and ground pins of U1. A reading other than 30mΩ indicates an error in the simulation (you might have to use special techniques such as 4 terminal sensing to measure these low resistances).

If it's necessary to distinguish between the resistance of the power and ground planes, that can be done by analyzing the voltage on each in this test circuit. Notice in **Figure 5** that there are 27mΩ on the power shape (dark blue represents 27mV, = 27 mΩ) and that in **Figure 6** there are 3mΩ on the ground shape (represented in red).

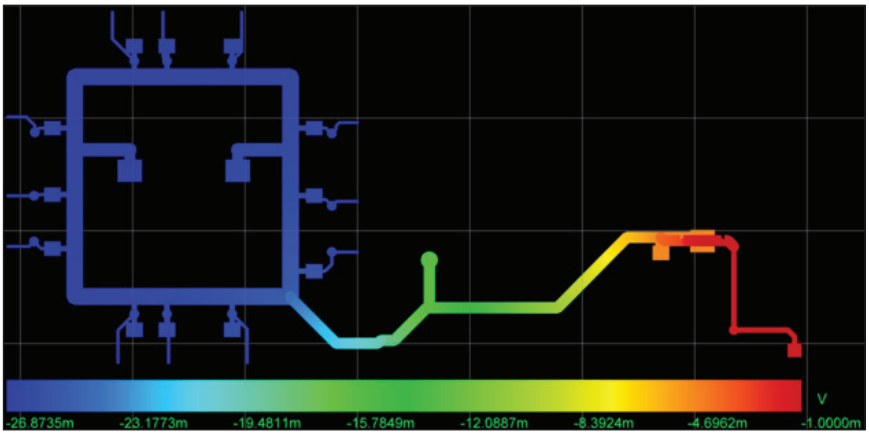


Figure 5: Power shape voltage plot results of measuring resistance (1V = 1Ω)

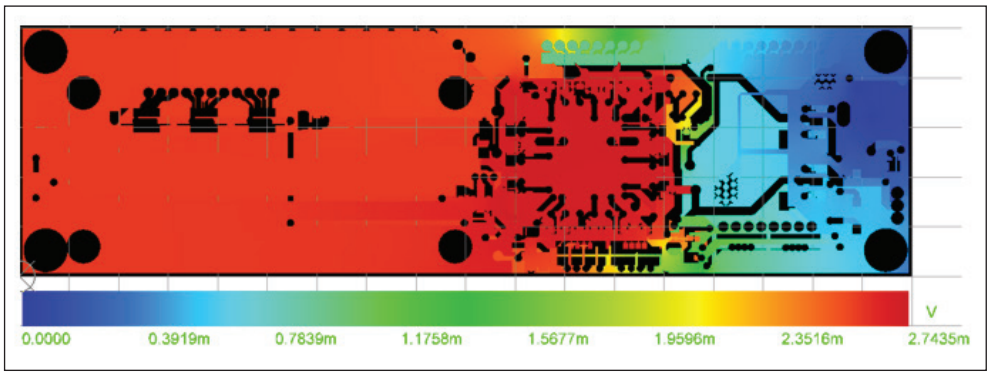


Figure 6: Ground shape voltage plot results of measuring resistance (1V = 1Ω)

One critical factor to take into consideration during validation is the difference in resistivity due to temperature. The resistivity of copper, for instance, typically increases by ~0.4% per degree centigrade. The resistance of a PDN can increase 20% for a design running at 75°C, compared to room temperature of 25°C. This can also be an advantage – if the voltage of a system meets expectations when running hot under full load, the designer has assurance that the copper isn't much hotter than expected, reducing the possibility of catastrophic failures due to unexpected temperatures in that shape.

OTHER PI-DC RESULTS

Running PI-DC on designs can also reveal many imperfections that wouldn't be otherwise apparent. Plotting the current density of power and ground shapes, for instance, makes "peninsulas" and "islands" of those shapes readily apparent. **Figure 7** shows the current density plots of a 2-layer design after running PI-DC. Notice the dark blue "peninsula" on the top layer and the "island" on the bottom layer. This unique PI-DC view highlights aspects of the design that aren't otherwise apparent. Note that care has to be taken before assuming a shape that is unused for PI-DC of a particular voltage isn't needed, that shape might be used for another voltage, or for AC power delivery (attached to capacitors). Putting small resistors in place of the capacitors during a PI-DC simulation and checking the corresponding current distribution allows a designer to see if an island or peninsula in a power shape is used for AC power delivery (note that the DC results will be invalid for this simulation). Current "islands" and "peninsulas" are especially troublesome in that they will have specific resonant frequencies, possibly causing failures only when certain conditions exist. The failures may appear random and thus extremely hard to troubleshoot – a recipe for delayed validation.

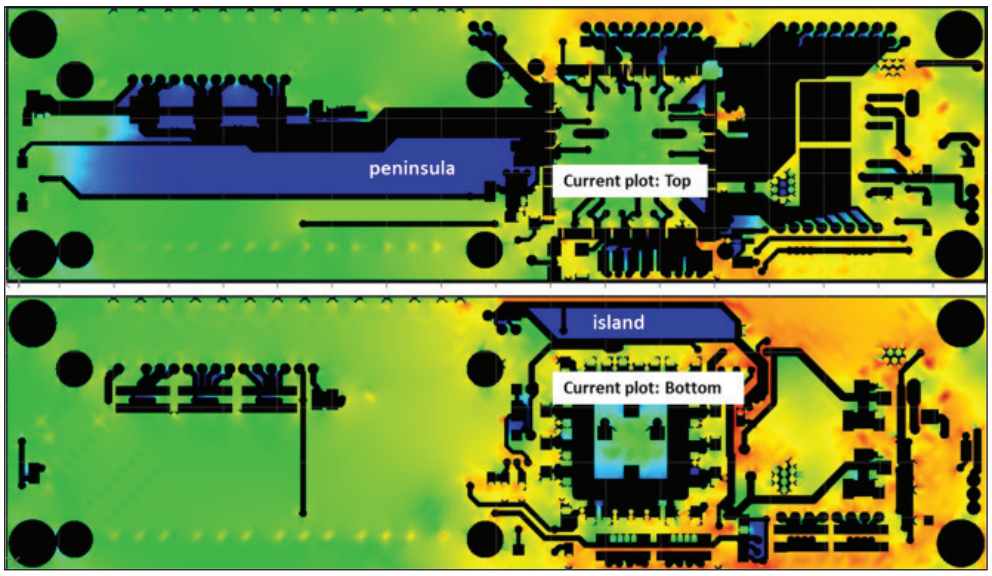


Figure 7: Ground shape current density plots showing "peninsulas" and "islands"

The current density and voltage plots of the power and ground shapes can also reveal problems with their design in efficiently channeling current between the power source and load(s). The voltage plot of the top ground shape in **Figure 8** makes the inefficiency of the paths between the sources (the voltage regulators, or VR's) and the load (FPGA) very clear. There may be valid reasons for not having a straightforward path between the VR's and FPGA, but PI-DC will highlight the inefficiencies so that they can be addressed, if possible. As a side note, it should be pointed out that this shape is problematic for AC power delivery, possibly inducing excessive inductance into the ground path and corresponding "ground bounce" (inductance increases with loop area).

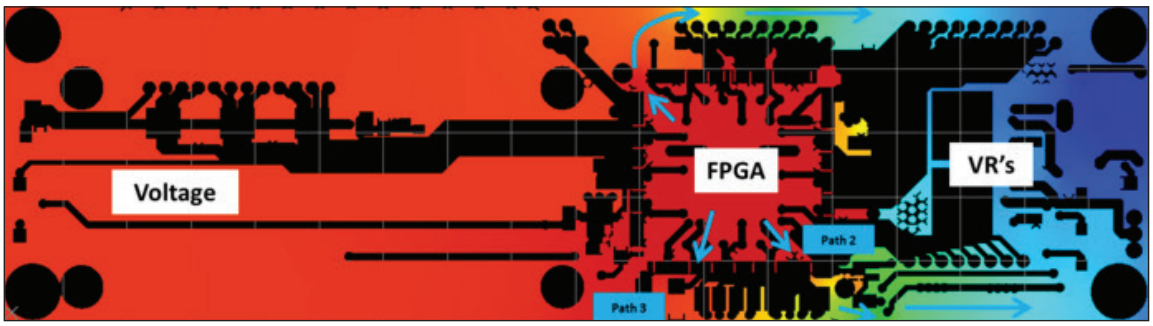


Figure 8: Ground shape voltage plot showing return current paths

Of course, the designer has to take care to also view their ground shapes in the context of its use as a return path for high speed signals, which may not overlap with its function as a DC return path. Ground (and some power) shapes that look unnecessary for DC power distribution purposes may be critical for signal integrity. But even in that context, "islands" and "peninsulas" should be avoided and only designed in when no other option exists. PI-DC often nicely highlights these unwanted shapes where they exist.

Another example where a PI-DC current density plot can be uniquely insightful is shown in **Figure 9**. In this example, a small break in a ground plane is very obvious – the current density color abruptly changes from green to blue at the break. This makes a profound difference in the DC power delivery of that shape, it's doubtful the problem probably would be identified without using this PI-DC results view.

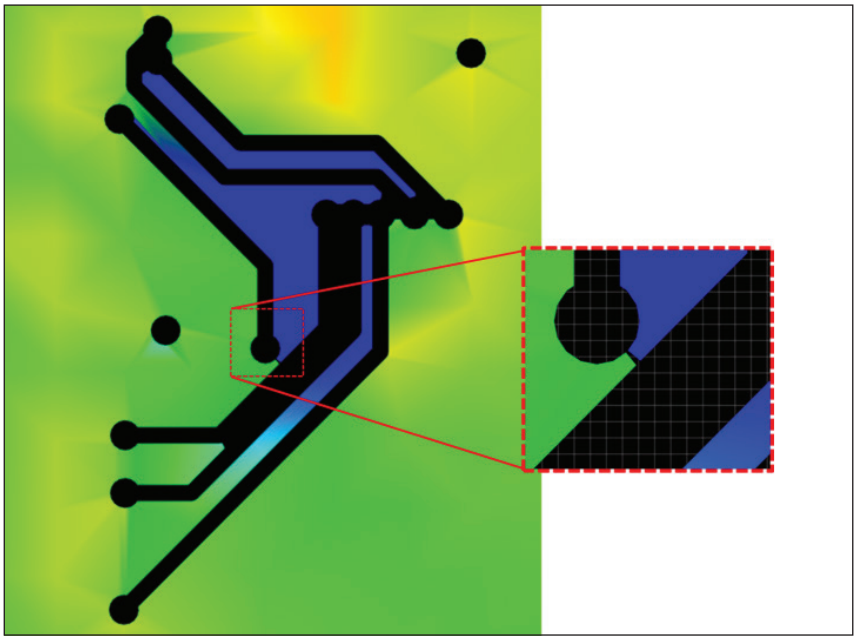


Figure 9: Small break in a ground plane apparent in PI-DC current density plot

There are some non-intuitive aspects of PI-DC that are worth noting. The DC resistance of a path depends not only on the width of the path, but the length also. A DC path can be narrow if it isn't too long without significant effect on the power delivery. For instance, paths (b) and (d) of **Figure 10** have the same resistance. To understand the DC resistance of shapes the concept of "squares" is valuable, as shown in **Figure 10**. This will allow the designer flexibility – they may be able to constrain a DC path to a narrow width if it's only for a short distance, and widening the path as much as possible in wide open spaces can compensate for necessary restrictions. Using the same width for a power delivery net along its entire length is inefficient, doesn't give the best power delivery available, and uses unnecessarily large power shapes.

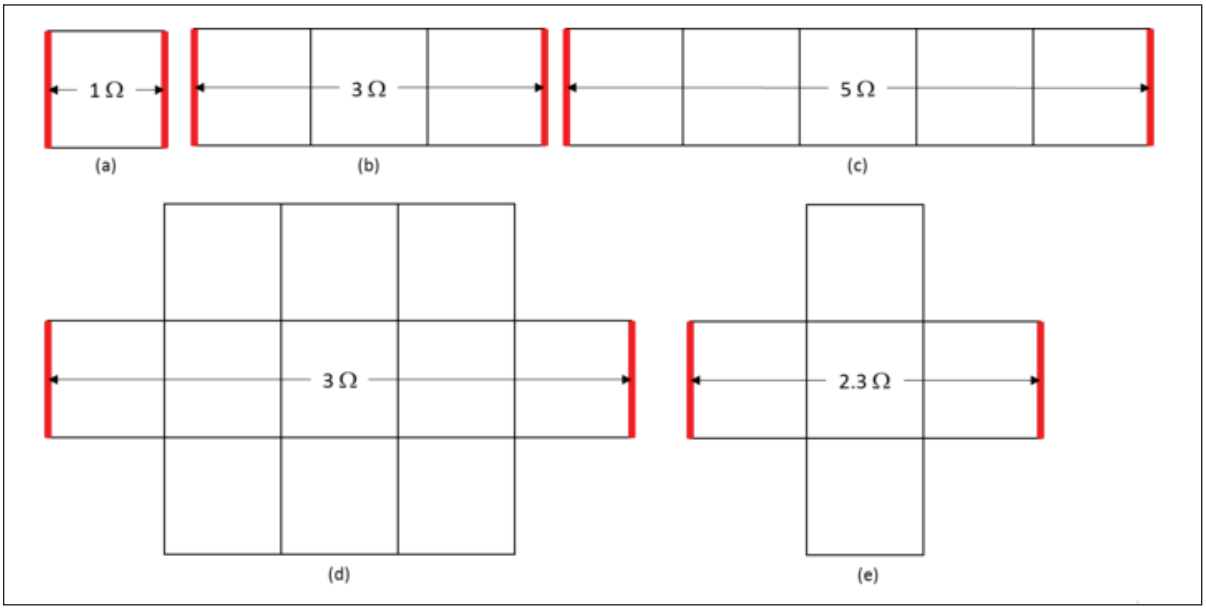


Figure 10: Resistance of power shapes as "squares"

Figure 11 illustrates 4 power shapes with very different forms, all having the same overall resistance. PI-DC gives designers options to modify the PDN shapes to meet the power delivery requirements in the most efficient manner.

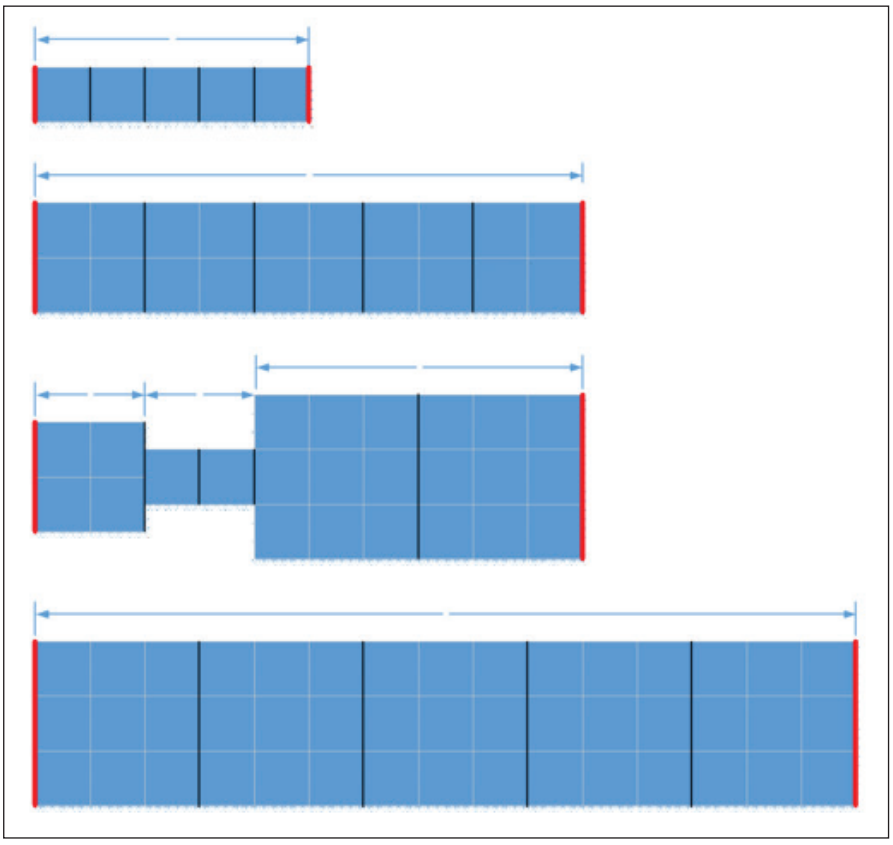


Figure 11: Various power shapes having the same resistance

WHY DO DESIGNS WITH ERRORS WORK FINE?

Something that will inevitably occur when you run PI-DC on existing designs is that you'll find many "errors" in the designs. Some people have remarked that they find errors with virtually every design they analyze with PI-DC – "How do they work if they're so broken?" There are 2 primary factors allowing faulty designs to function, even with flaws in their PI-DC construction:

1) DC power delivery has historically been conservative. To determine the correct width of a conductor for a given current, IPC specifications call out the width, dependent on the allowable temperature rise. Digital designers typically don't have reliable data on how much temperature rise is appropriate so they use conservative values, probably based on past experience, or they provide "as much copper as is available". If they have doubts as to whether it's enough, they count on checking the voltage(s) during validation. If the design meets the requirements, that adds to their experience and they use that as a guideline for future designs. In the absence of failing designs, there is no way for a designer to know if they can reduce the amount of copper dedicated to power delivery, so they grow conservatively. There is enough margin in the design to accommodate flaws, even significant ones.

2) "Peninsulas" or "Islands" don't negatively affect the **DC** power delivery, but can affect AC power delivery and/or signal integrity in a seeming random manner. They are an indication that a design can be improved, but may not cause a design to fail for DC power delivery. They do present other especially problematic issues for **AC** power delivery and **signal integrity** in that they can "resonate" at particular frequencies. If those frequencies are excited in the shape, excessive AC noise can be induced on the PDN or, if there are signals adjacent to the shape, it can introduce significant noise on those signals at its resonant frequency or frequencies, causing logic failures. In either case, the failures will depend on the existence of the particular resonant frequencies and may appear random, or only occur in very particular circumstances, making them extremely hard to replicate, trouble shoot, and correct. It is much wiser to take steps to preemptively mitigate these particularly mischievous issues.

Perhaps "imperfections", "areas for improvement", or "non-idealities" would be better terms to use than "errors", but... In these days of emphasis on battery life and cost savings, being overly conservative or allowing flaws in a power shape such as peninsulas can make the difference between a failed or successful product and can no longer be ignored. PI-DC not only gives information about whether a PDN is adequate, it can inform about whether power delivery shapes are necessary.

BE SURE TO LIMIT THE CURRENT SOMEHOW

An important consideration in the design of a PDN is providing for unplanned circumstances. The designer has to be aware that, in the case of a catastrophic increase in current (a short to ground, for instance), an optimized power shape might not be able to absorb that extra current and cause a failure in the design. Some means of limiting current flow in the case of catastrophic errors needs to be provided if those might be encountered (power going to any connector that might be shorted during installation, for instance).

DETERMINING THE SIZE AND NUMBER OF VIAS

A rule of thumb commonly used for power delivery is to have enough vias such that their cross-sectional area is the same as, or larger than, the power shapes they are connecting. Experience indicates this is sufficient, but a PI-DC tool can tell you whether this is necessary. Using excessive vias, or excessively large vias, causes routing restrictions in all the layers above and below the transition, and should not be done lightly in most of today's designs. Unnecessary vias in one power shape may impact another power shape on other layers. A PI-DC tool allows you to gauge the effect of vias on the PDN. **Figure 12** shows 7 vias (circled, labelled "a" to "g") in a power delivery design. Careful examination reveals that there is a significant color change in 3 of the vias, "a", "b", and "d", indicating a corresponding voltage drop due to each of these three. Probing the exact voltage at the top and bottom of these vias (a common capability of PI-DC tools) allows the designer to determine if the via size and number are adequate and necessary. As previously explained, there is some ambiguity in the exact dimensioning of vias in simulations, so care must be taken to account for plating thickness effects, for instance. Note that vias are typically represented as "lumped elements", assigned a resistance as a function of the vias' diameter and length, and are typically not "solved" as complex columns within the solver, making simulations much faster while not sacrificing significant accuracy.

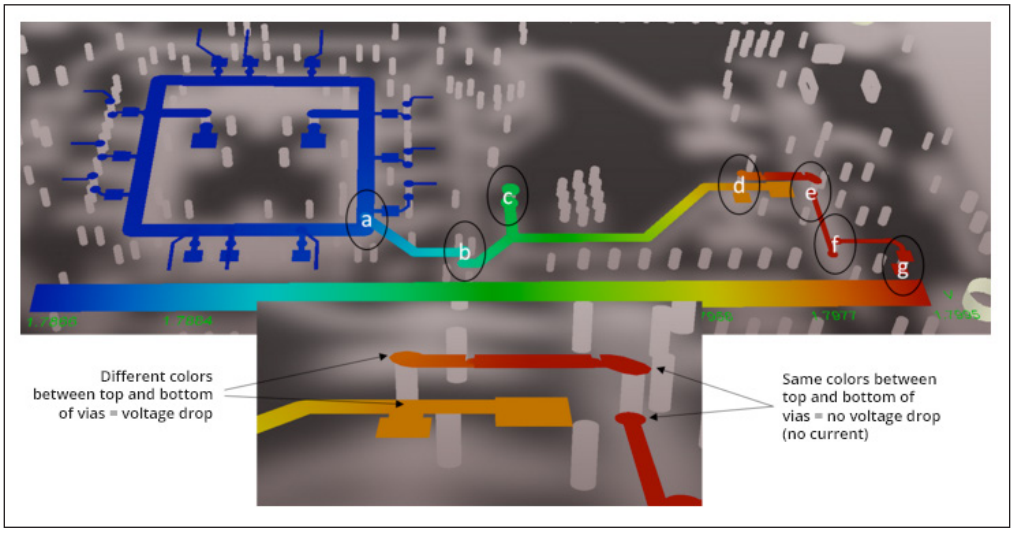


Figure 12: Voltage plot, showing voltage drop of vias and shape

CONCLUSION

A PI-DC simulator is an essential tool for any digital designer's toolbox, providing valuable insight into how to reduce a design's size and complexity while improving performance. Optimizing the power delivery network can save precious design real estate and layers, resulting in lower cost with increased performance and reliability. PI-DC simulation is an essential capability for every digital (and analog) designer.