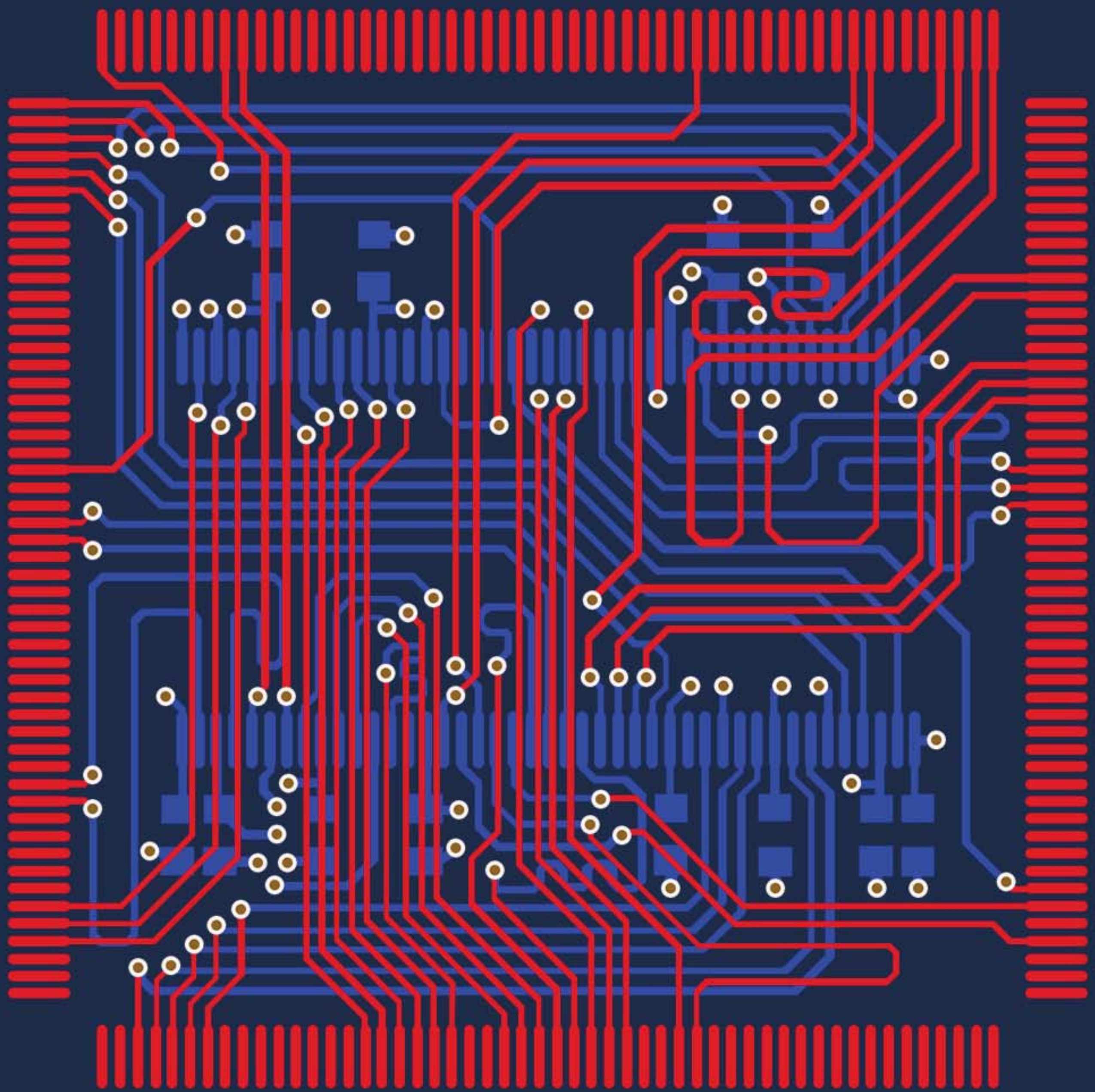
Altium®

Pack More Complexity into a Smaller Footprint Using HDI



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As the world of technology has evolved, so has the the need to meet the increasing demands of end-users to have better devices packed into smaller packages. PCBs designed using high-density interconnect (HDI) techniques not only creates a more compact footprint, but improves the functionality as well. HDI accomplishes this using blind, buried and micro vias, vias in pads and other routing options. In this paper, you will learn the basics of HDI design flows and how Altium Designer® can meet these needs.

INTRODUCTION

The demand for smaller mechanical housing just continues, leading to more complexity in the electrical design process to generate a PCB to keep up with the shrinking form factors. To achieve the size and density necessary, engineers turn to HDI. Using HDI, however, means dealing with different routing workflows, and denser parts, while using the same area or less. The methods described here outline the options available to you.

HDI CHALLENGES

Today's design process often requires engineers to pack as much as they can into as little space possible. Basic design workflows hinder this in a number of ways. Primary among these concerns are the costs of fabrication. Now, it is important to point out, that the fabrication process for HDI designs costs more than a conventional PCB.

Taking processes used for simple through-hole vias simply will not work when creating boards of higher density with higher numbers of connections and components. It seems a bit counterintuitive to expect the design to have more complexity but less workspace to work with.

Here is a basic list of challenges you may run into when designing an HDI board:

- Limited board workspace area
- Smaller components and denser spacing
- Larger number of components on both sides of PCB
- Longer trace routes creating longer signal flight times
- More trace routes required to complete the board

DESIGN TOOLS SOLVE CHALLENGES

HDI Design is defined by the IPC-2226 standard and creates options to overcome these design obstacles, allowing you to create better, more efficient boards with less real estate. With HDI design, you can increase or decrease layer counts, improve trace routing options, place vias in pads, improve signal transmission, and reduce signal loss or delays.

Although it may be more costly to produce these boards, there are also methods to the design process that can help to reduce some costs in terms of layer count and board size. You can place more components in the same area and still have the same functionality or better. The smaller board, coupled with reduced layer counts, can reduce the effective cost.

FINER, SHORTER LINE TRACES

More components on a smaller board demands the use of both finer and shorter line traces. Not only does this allow for increased density on the board, but shorter trace routes and finer line widths improve high speed performance. Overall, the design has less weight, for lighter, smaller and better products.

VIA STYLES

At the center of HDI design is the via. Using vias in a different way generates options for routing topology and layout design. Blind, buried, and microvias all have distinct and useful functions in routing an HDI board and Altium Designer supports all of these. A traditional through-hole via is drilled all the way through the board. The hole is then plated with copper and used for connectivity between layers. These vias then connect to planes, traces, and polygons on the different layers.

Taking this simple concept and now creating vias that start and stop on specific layers, you open up routing options. Another nice option is that if you're have ample real estate on the top and bottom layers, but would like to consolidate the board to have fewer layers, it may be possible using different via styles Let's take a look at some examples of how this would work.

First, Altium Designer allows you to manage the drill pairs in the Layer Stack Manager (see Figure 1), assigning the start and stop layers for different via types. Starting a via on the top or bottom layer and end the via on an internal plane or signal layer is a *blind via*. Connecting directly from one internal layer to another internal layer using a via is a *buried via*. It is also possible to have an isolated layer strictly for routing that is only accessed through buried vias.

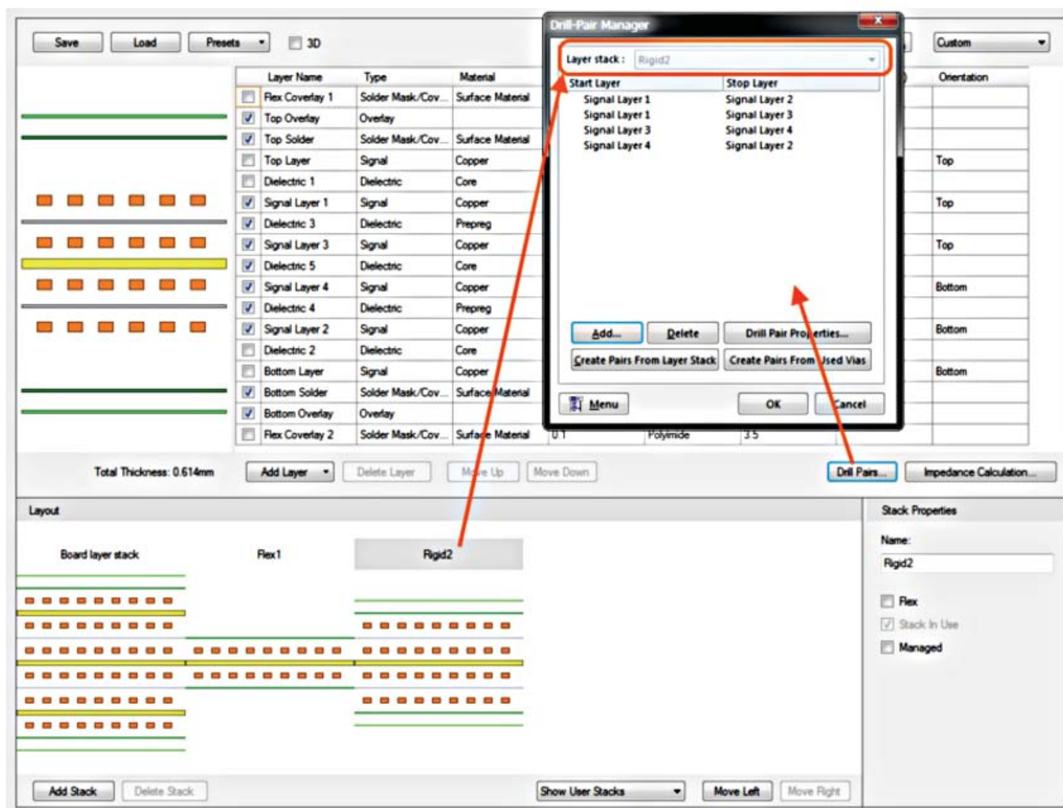

Figure 1: Drill pairs dialog found in the Layer Stack Manager

Microvias

Not only are microvias different in size, but the fabrication process is a bit different as well when compared to through-hole vias. A microvia, by definition of IPC-2226, is a via with a diameter of ≤ .15mm or slightly less than 6 mils. Due to the smaller size the IPC standards define that the pad size must be at least double the diameter of the via, and the hole is laser drilled to maintain connection integrity. Blind and buried microvias are also allowed.

Microvias are also single layer vias. Microvias can connect multiple layers by stacking or staggering them. All holes are laser drilled and then plugged so that solder doesn't penetrate into the hole during fabrication.

Here are examples of these different via styles in use. A 6-layer board design is illustrated with the via dialog in Figure 2 and the resultant cross-section of the completed board in Figure 3. Several via styles are shown with their associated dimensions.

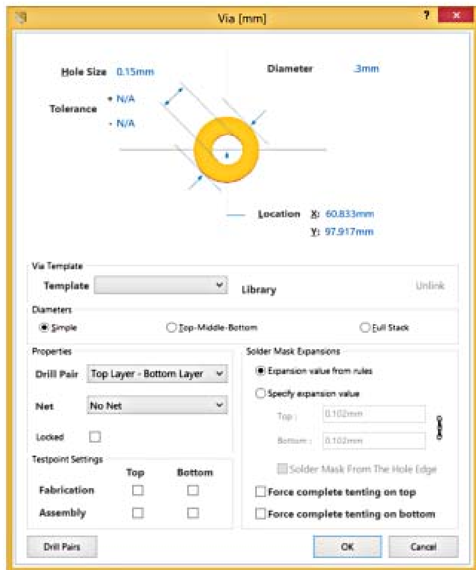

FIgure 2: Via Properties Dialog

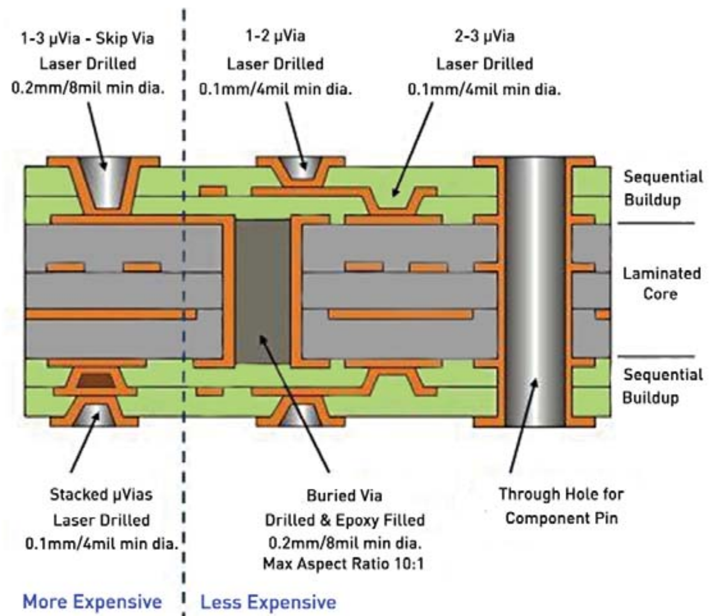

Figure 3: Example of Via Styles In this example, you can see a 6-layer board. — Illustration courtesy of www.fedevel.com

The example in Figure 4 has 4 layers. Traditional routing methods would use through-hole vias to connect the top and bottom layers for routing and connection purposes. These vias can connect to internal layers on the way, using thermal relief connections on plane layers and polygons. However, for routing purposes, the via would require a connecting pad on that layer before continuing the route. The mid-layers offset additional routing needs where the top and bottom layers did not have room. A blind or buried via can connect to the necessary planes or an additional layer for more routing options.

As you can see, the challenge with through-hole vias is that routing takes up real estate on the top and bottom layers, as well as the internal signal layers. Anywhere a via is placed, you are connecting to the other layer(s) but you lose routing area on these layers due to the via placement and clearance rules.

Figure 4: An example of a through hole via connected to top and bottom layers, and one internal plane layer.

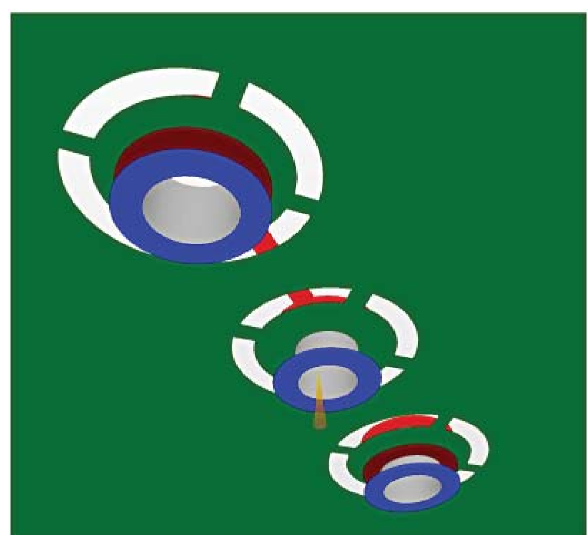

Figure 5: Through-hole via style.

Now, if we choose to use a microvia to connect from the top layer to the plane layer, we open up that space underneath. If we need to, we can use the space underneath for routing. This is a small example of how a microvia may help, not to mention space opened up on the layers the microvia actually connects to.

What if, in Figure 6, the connection from the top layer to the internal plane layer is made using a blind via. If the internal signal layer is used only for routing, why to go through the layer if it's not necessary. Theoretically, we could push all our connections down to the internal signal layer and do all our routing on this layer, leaving the top and bottom layers for component placement, illustrated in Figure 7. You can stop the blind via on the plane layer without taking up real estate on the additional signal layer.

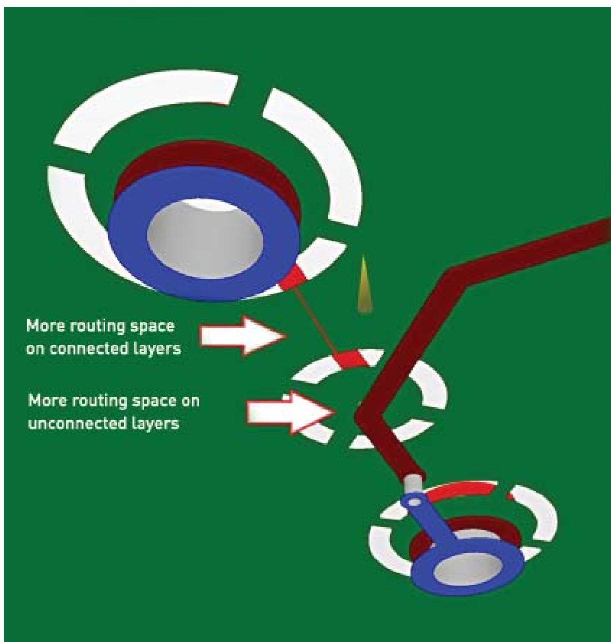

Figure 6: Microvia Routing Style — Better Workspace Management.

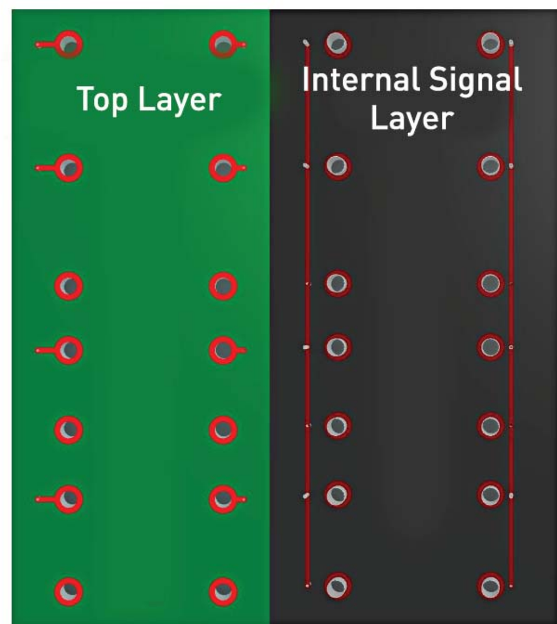

Figure 7: Routing on Internal Layer – Simple Version
Note: Stacked Microvias In Use

Vias In Pads

Another method for increasing routing options is placing vias in pads. As long as you maintain the connection integrity, you can place vias directly in pads and drop the connections to other layers without routing on the top or bottom layers with components.

The example in Figure 8 shows a top layer pad without a hole and a via placed in the pad. This becomes much more advantageous as you can design a PCB footprint with these properties and the component already has the vias connected to the pad to connect directly to other layers.

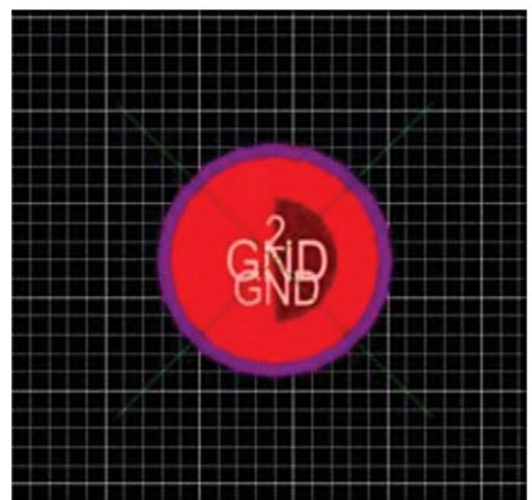

Figure 8: Via in pad

THE FABRICATION PROCESSES

Always check with your board house to determine their fabrication methods for HDI. There are processes that some board houses will use and not use, and it's good to have an understanding of these methods. Also, you may need to include documentation notes to help provide understanding in some areas that are not straightforward. This is a good check to ensure congruity and know that your design is able to be supported by your board house.

CONCLUSION

Generating an HDI board can be fairly simple, yet is a powerful method for designing next-generation technology and board design processes. This is a high level explanation of how the process is used and supported in Altium Designer.

You can see that this process is not only doable, but may be advantageous in making your next design much more competitive and user-friendly. Configured and used correctly, HDI boards can give your company a competitive edge.

USEFUL LINKS

Altium Tech Docs:

Design Rules

https://techdocs.altium.com/display/ADOH/Design+Rules

Via Dialog

http://techdocs.altium.com/display/ADRR/PCB_Dlg-Via((Via))_AD

Via Object

http://techdocs.altium.com/display/ADRR/PCB_Obj-Via((Via))_AD

Drill Pair Manager

http://techdocs.altium.com/display/ADRR/PCB_Dlg-DrillPairManager((Drill-Pair+Manager))_AD

Drill Pair Reference

http://techdocs.altium.com/display/ADOH/Drill+Pair+Reference

Routing Via Style

http://techdocs.altium.com/display/ADRR/PCB_Dlg-RoutingViaStyleRule_Frame((Routing+Via+Style))_AD

PCB Layer Stackup Technology and Terminology

http://techdocs.altium.com/display/ADOH/PCB+Layer+Stackup+Technology+and+Terminology

Articles:

EE Times: Reduce Your PCB Costs with Blind Vias, Buried Vias, and Microvias

http://www.eetimes.com/author.asp?doc_id=1320862