ALTIUMLIVE 2018:

# Overcoming the Challenges of HDI Design

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# HDI Challenges

- Building the uVia structures
- The cost of HDI (types) boards
- Stackup types for uVias
- Some Pros and Cons of stackups
- Getting all the signals out of the parts – patterns and grids
- Planning the flow from layer to layer
- Manufacturing issues
- *There is a learning curve for using HDI, but once understood, there is creativity in routing*

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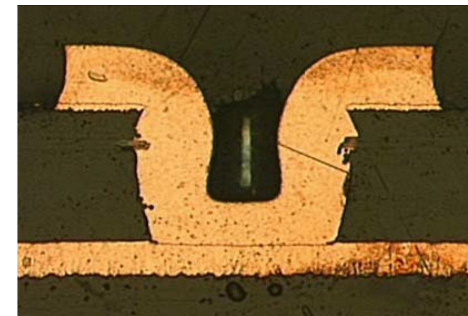
# Building the uVia Structures - Microvia Pads

- The microvia built in CAD software will result with a normal pad/hole/pad scenario
- Landing pad slightly larger if possible, but at least the same size
- Recommended pad diameter is drill + .006”. More pad helps prevent  breakout



- The smaller pads, drills, and depth of HDI opens major channels for routing

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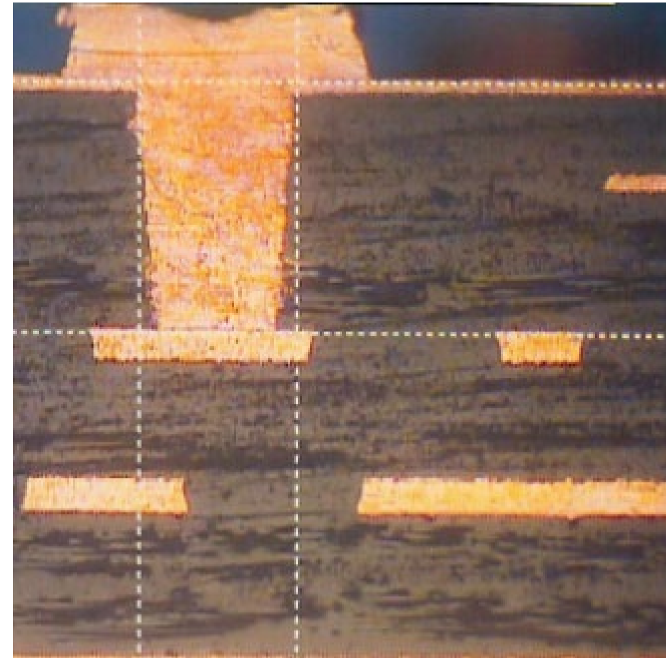
# Variable Depth Blind Vias

- Formed with a laser drill that penetrates Two dielectric layers
- Good for getting signals down 2 layers when (for example) pwr/gnd are desired on outer layers
- May connect at one or more layers
- Will need antipad if not connected to a layer



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# Variable Depth Blind (Skip) Vias

- May be used on any (IPC) Type of HDI board or layer
- Be careful of aspect ratio*
- MUST have larger pad and hole size than standard uVias because of another dielectric layer to drill through
- Fewer fabricators do multiple depth vias
- Extra cost

*Aspect Ratio = A) Board (or layer) Thickness divided by B) Drill Diameter

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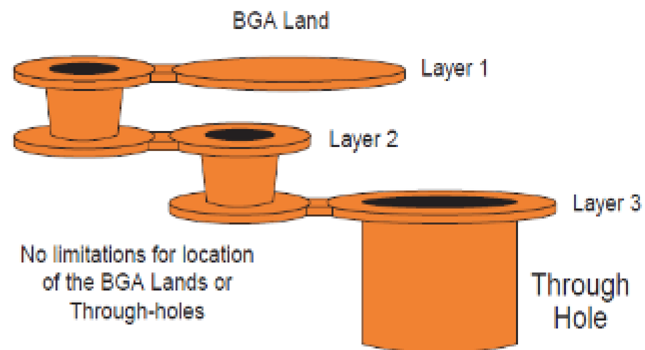
## Staggered Vias

- IPC – A uVia on one layer connected to a uVia or TH via on another layer
- Easier to manufacture than stacked vias, but use a bit more space
- Most common way to move signals from layer to layer



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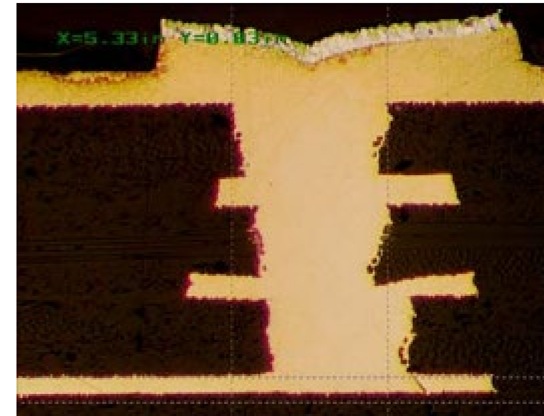
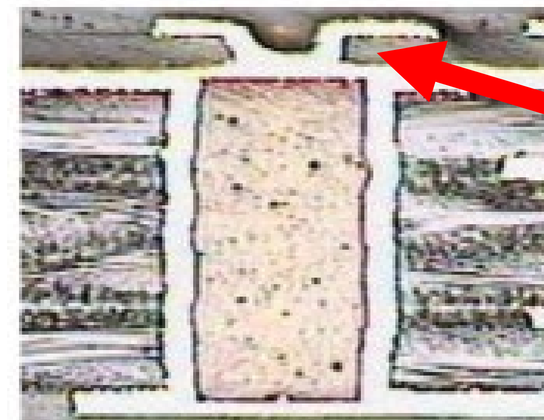
## Stacked Vias

- Stacking of microvia on microvia probably OK
- Must be filled – conductive material for uvias, and generally non-conductive for buried TH vias
- Prefer No uVia on TH via
- Complex registration
- More chance of failure





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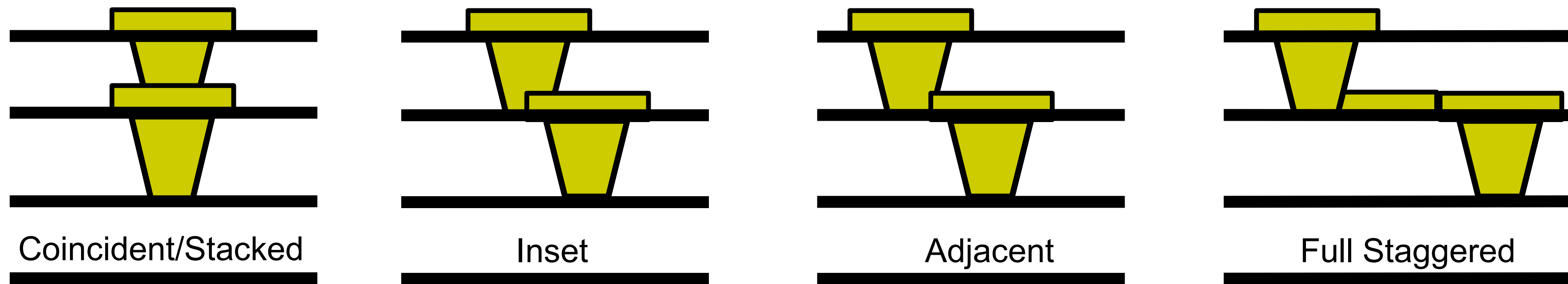
# Configurations of vias in a Stackup



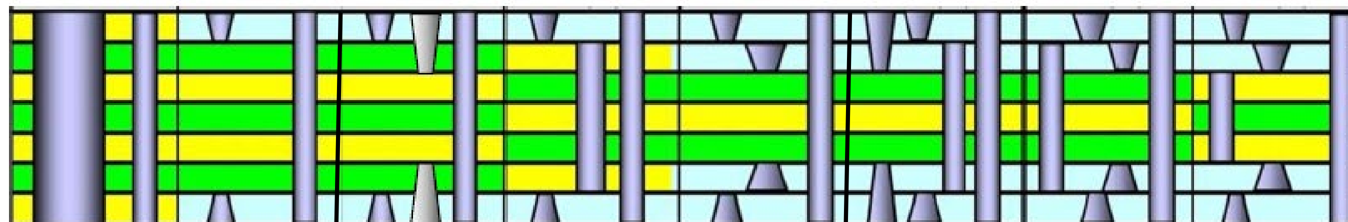

- Vias can be combined in various com-binations to create stacked or staggered vias
- Stacked; Inset; Adjacent; Full staggered
- May need slightly larger pads or fillets
- Check with fabricator

# Cost Advantages and Disadvantages -

## HDI Cost Is Complex

- If your TH board is 10-12 layers, then HDI may be able to reduce your costs*
- Three manufacturing processes that dominate PCB cost - Lamination, Drilling, & Plating*

| Construction | TH | 1+n+1 | 1+n+1 | 1+n+1 | 2+n+2 | 2+n+2 | 2+n+2 | 2+n+2 |
|---|---|---|---|---|---|---|---|---|
| Laminating ($$) | 1 | 1 | 1 | 2 | 2 | 2 | 2 | 3 |
| Drilling ($) | 1 | 3 | 5 | 4 | 5 | 6 | 6 | 6 |
| Plating ($$$) | 1 | 1 | 1 | 2 | 2 | 2 | 2 | 3 |



*Happy Holden in “Current PCB Cost Drivers”

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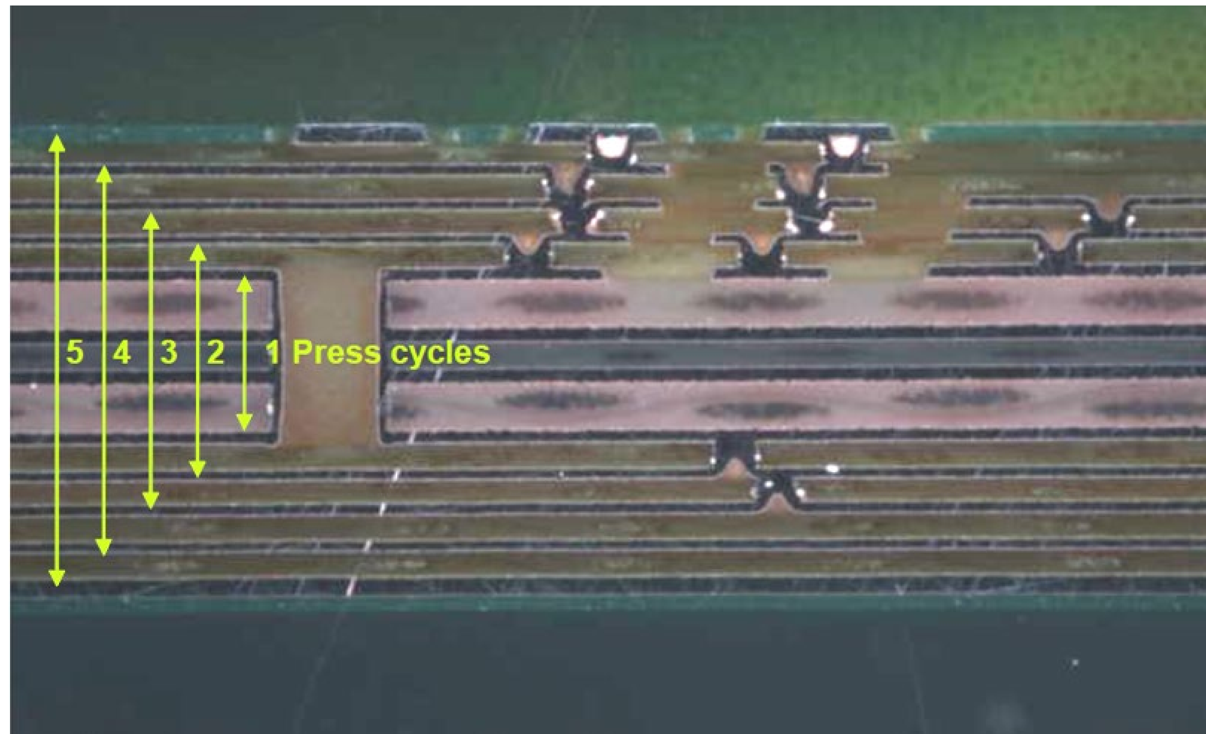
# Be Aware of Lamination cycles

- Board with 5 press cycles and staggered vias
- Lamination/heat cycles are hard on joints and materials






Picture published by Somacis

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## Sequential (Build up) lamination

- 2 or more pressing cycles for multilayer board
- Sub boards are laminated, drilled and plated, then other layers are laminated to first, then drilled and plated again. (Additional cost and stress on laminate material)
- Basically building multiple boards
- Each plating cycle will need from .0005” to .001” added to small traces, pads, and even antipad openings for etch compensation

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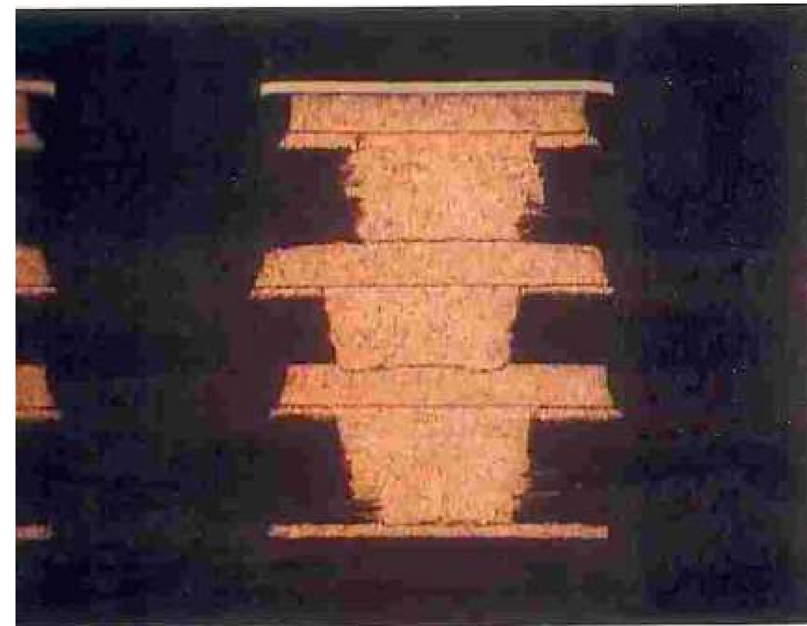
# Plating, Fill, and Planarization

- Hole depth is limited by plating aspect ratio
- Fill can be conductive or non-conductive for connectivity
- uVias preferred filled if via in pad, or stacked
- Plating and planarizing eliminates dimples, reduces voids and creates a flat ‘cap’ for soldering part

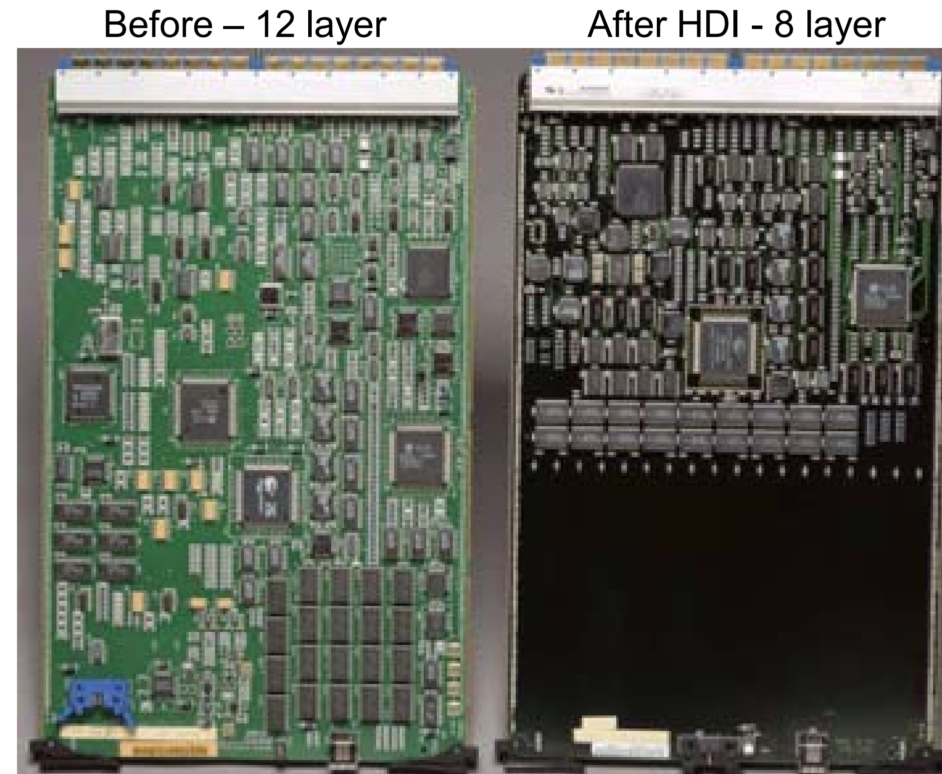


# Cost of HDI



## HDI may cost more but…

- Enables more routing
- Narrow traces/small holes and pads
- Uses fewer routing layers
- May enable smaller board
- Parts closer together




- Less board material needed for array – lower cost

*Picture - Happy Holden – “HDI/Microvia Technologies”, PCB East 2009

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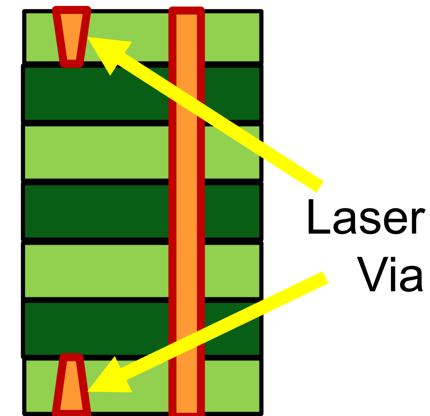
## Stackup Types for uVias -
## What is needed for an HDI Stackup

- Early considerations by fabrication, assembly, testing and thermal departments
- Decide general size and depth of laser vias to be used
- Dielectric layers must be thin enough to laser through
- Impedance controlled trace widths that are manufacturable (with thin dielectrics)
- Maximum size of board and panel used
- Ability to move signals to/through as many layers as needed

# IPC Type I HDI Stackup

- **Type I** is a through hole board with planned blind drill from top down one layer, or bottom up one layer, or both
- Single Lamination
- No build-up
- Easiest and cheapest HDI
- Requires fewest processes and registration issues



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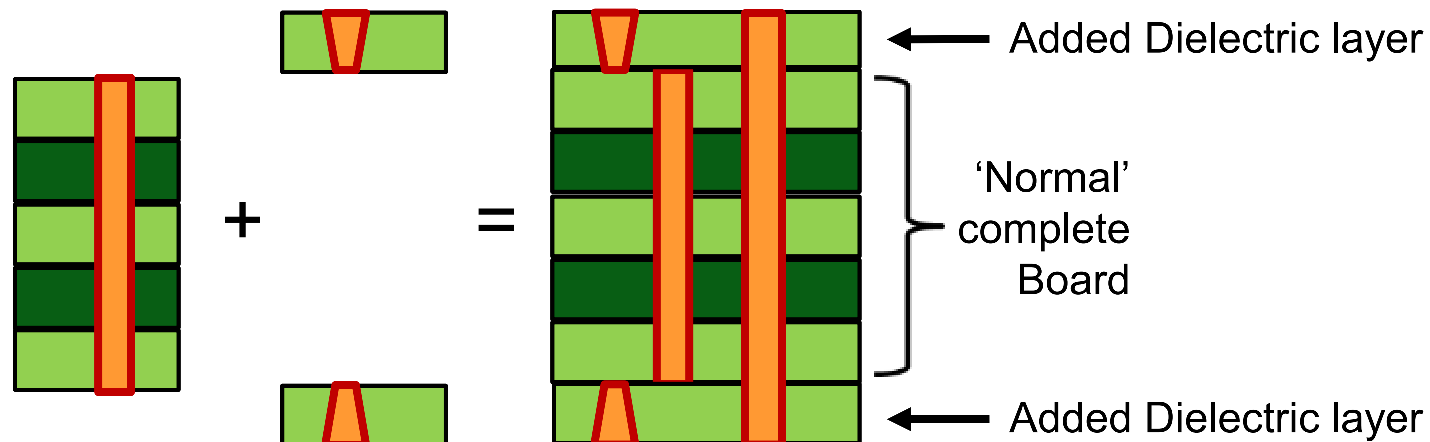
# IPC Type II HDI Stackup

- **Type II** is a complete (drilled) board with planned dielectric layers added to one or both sides for TH and laser drilling down/up one layer, and buried vias



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## Advantages of Type I and II over other

- Minimal complexity for designer to design and fabricator to build
- Increased routing density over TH
- Better for routing miniature parts than TH
- Lower HDI cost than other types
- No stacked or staggered vias, which require extra registration efforts
- No stacked vias that may require fill and planarization at EACH sub-build within stack

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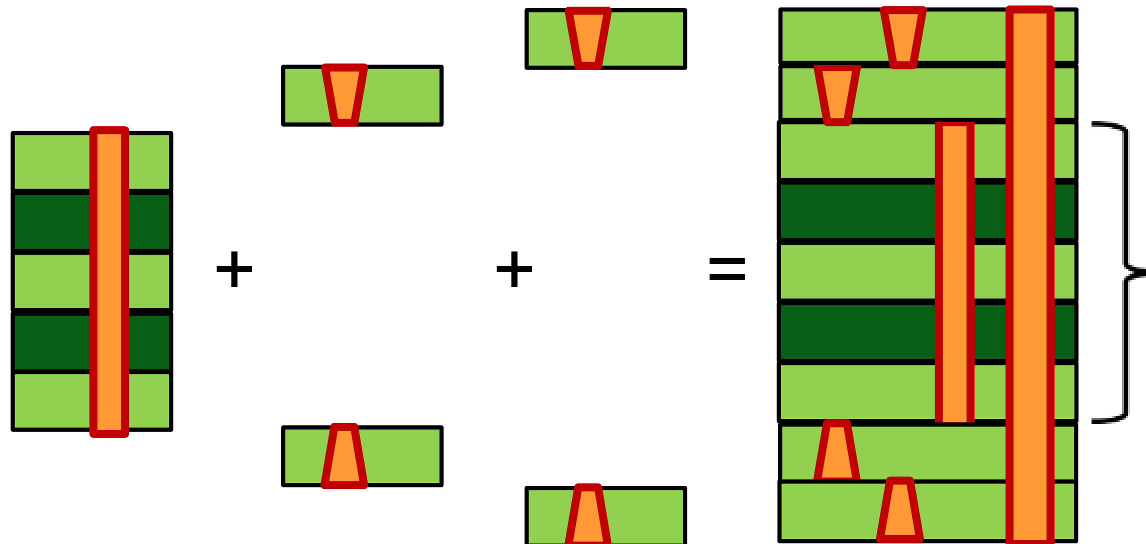
# IPC Type III HDI Stackup

- **Type III** is two HDI layers on one or both sides of a substrate 'core' board
- Commonly called 2-N-2



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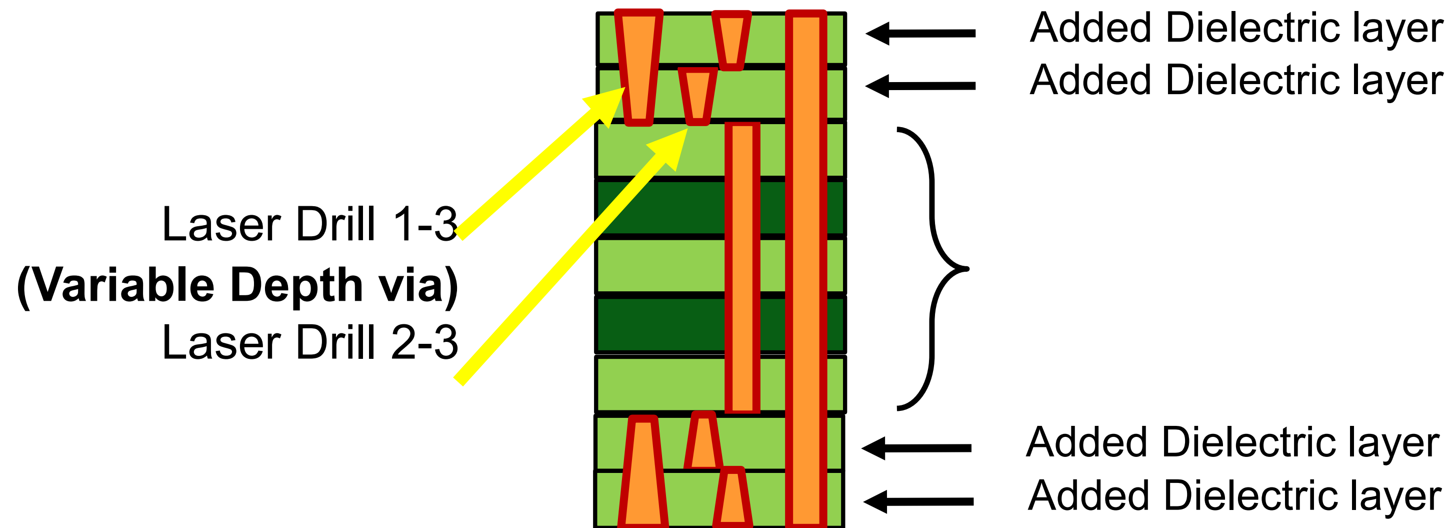
## Another Type III Stackup

- Two HDI layers with TH vias, buried vias, and/or Variable depth (or skip) vias



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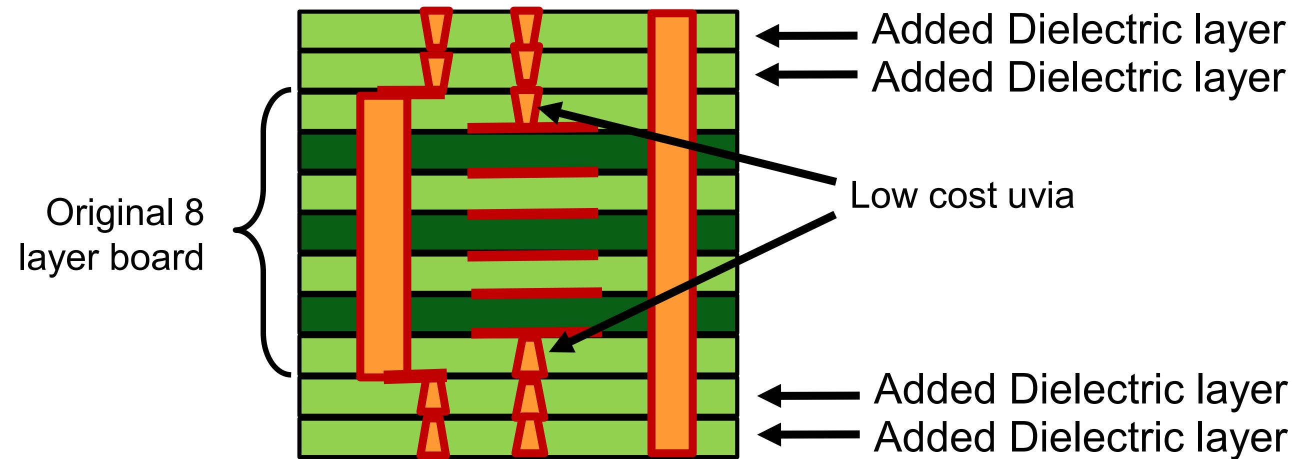
# Another Type III Stackup

- Two HDI layers with TH vias, buried vias, stacked and staggered laser vias



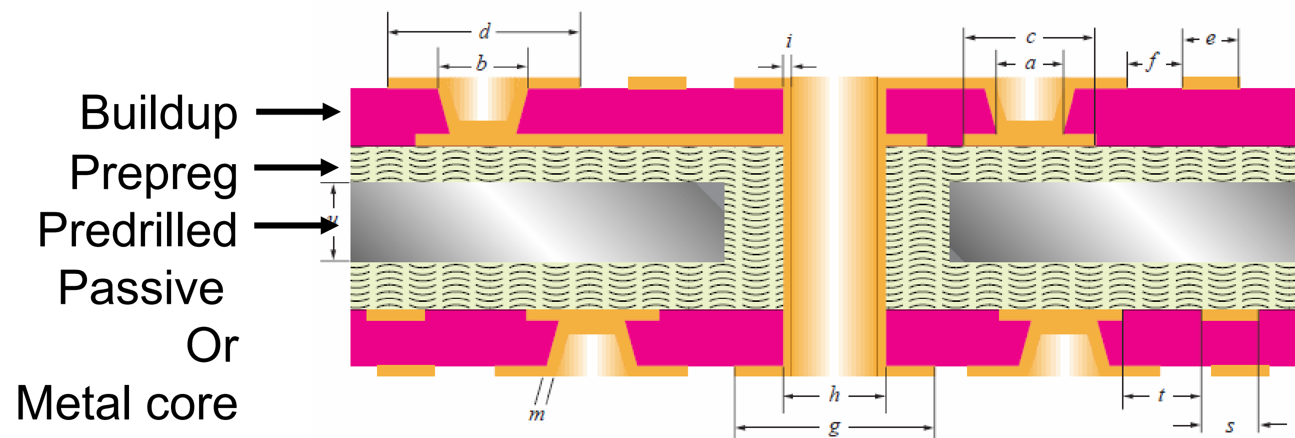

- Most designs are a variation of Type III or less

## The Advantages and Disadvantages of a Type III HDI Stackup

- Will handle ever increasing large and complex designs
- Design fanout and routing may be quite creative
- More ways to get signals through the stack
- Easier to get signals down to buried TH vias in the stack
- More fab steps than Type I or II

# More Complex HDI per IPC

- **Type IV** is a set of microvia layers over passive core substrates with no electrically connecting functions
- Core may be for thermal, CTE or shielding
- Requires multiple laminations



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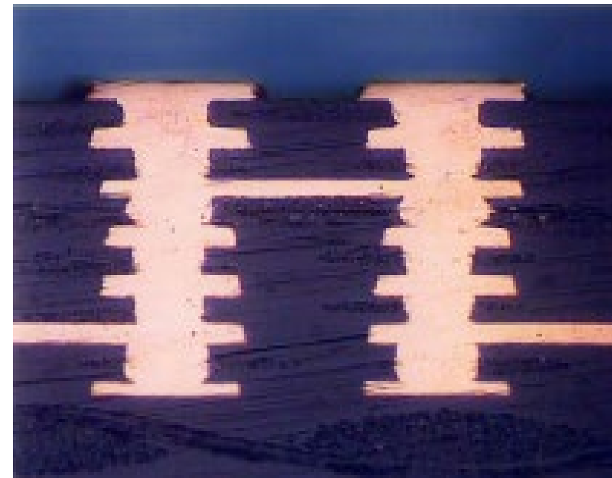
## Sometimes a uVia "type" is forced on us

- Example: If board and routing are extremely dense
- Many layers connect to many other layers
- **Type V-VI** uVia board per IPC 2226
- "ELIC" or "ALV" - every layer interconnect
- Registration issue
- Single lamination
- No inner layer plating



# The Advantages and Disadvantages of a Type IV, V, and VI HDI Stackup

- Will handle the most complex designs
- Even more fanout, stackup and routing possibilities
- Microvia layers are used as redistribution layers for the signals
- Much more complex for designer and fab
- Higher cost in US
- Type V and VI can be lower cost & higher yields with processes in other countries

# Stackup

- Most boards of all types are foil construction
- It is recommended to drill microvias into prepreg dielectrics
- **Design to IPC Class II, whenever possible**
- Very thin dielectrics (.002" or less) may be used (check price)
- Thin dielectrics may add up to thinner boards than traditional .062" or .093", if desired
- Balanced stackup much preferred

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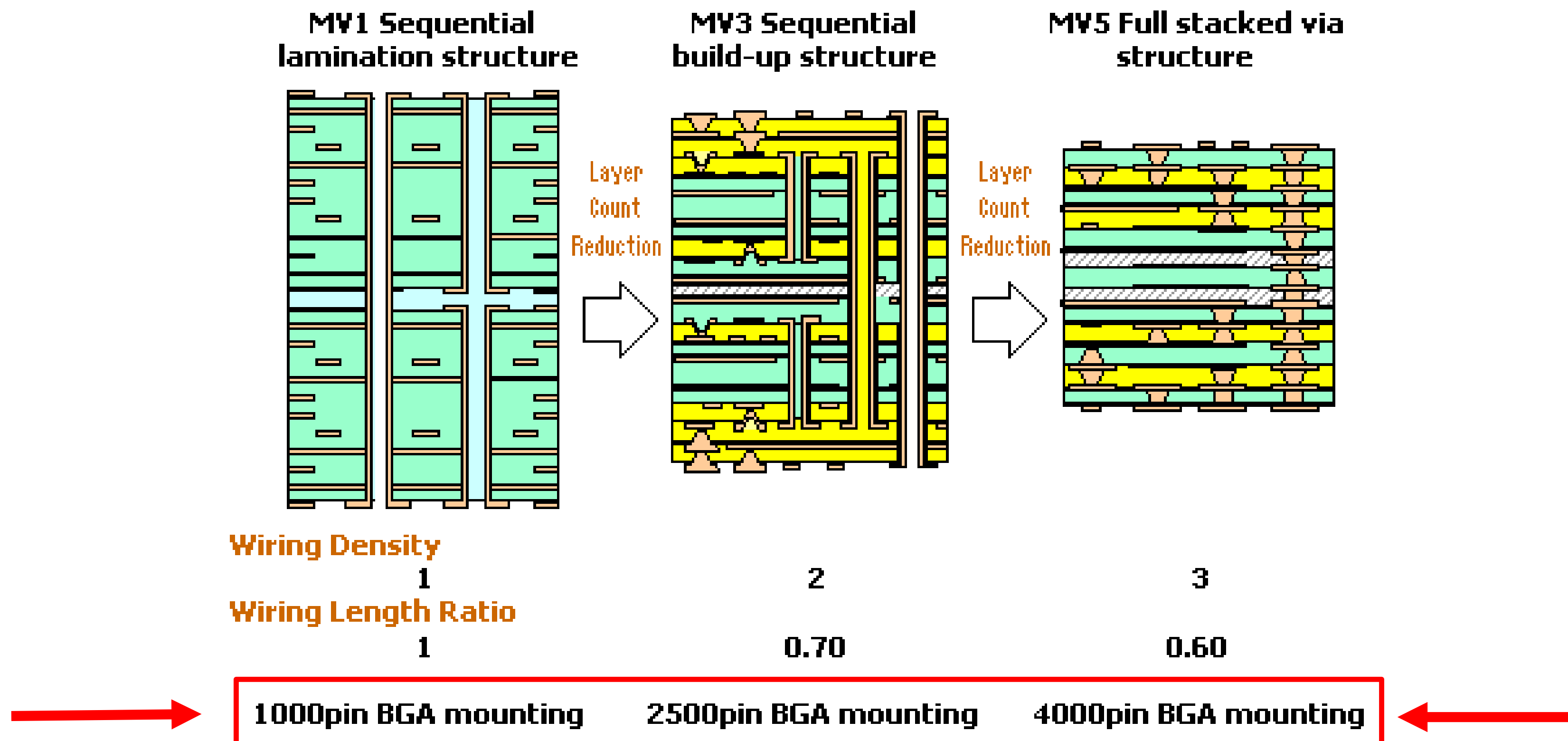
# Knowledgeable fabricator may give pros and cons for planning different stacks




My apologies, I don't have the source of this picture from 2013

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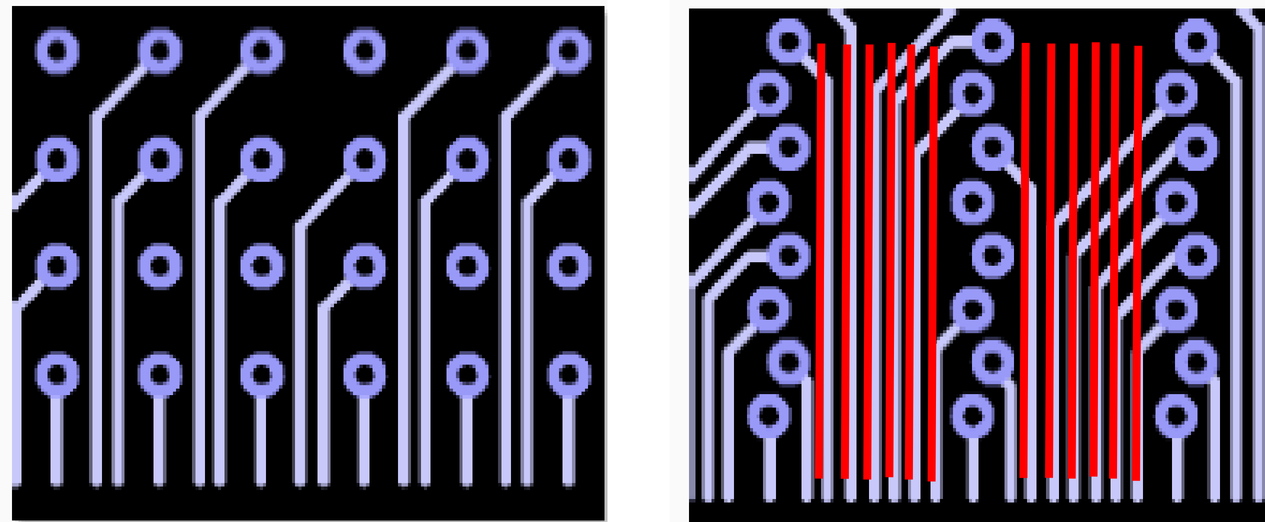
# Getting all the signals out of parts - HDI Via Channels Improve Efficiency

- Routing might be set up very differently for small and large parts
- Small parts may just need a path for each signal; Large parts may need channels for many signals



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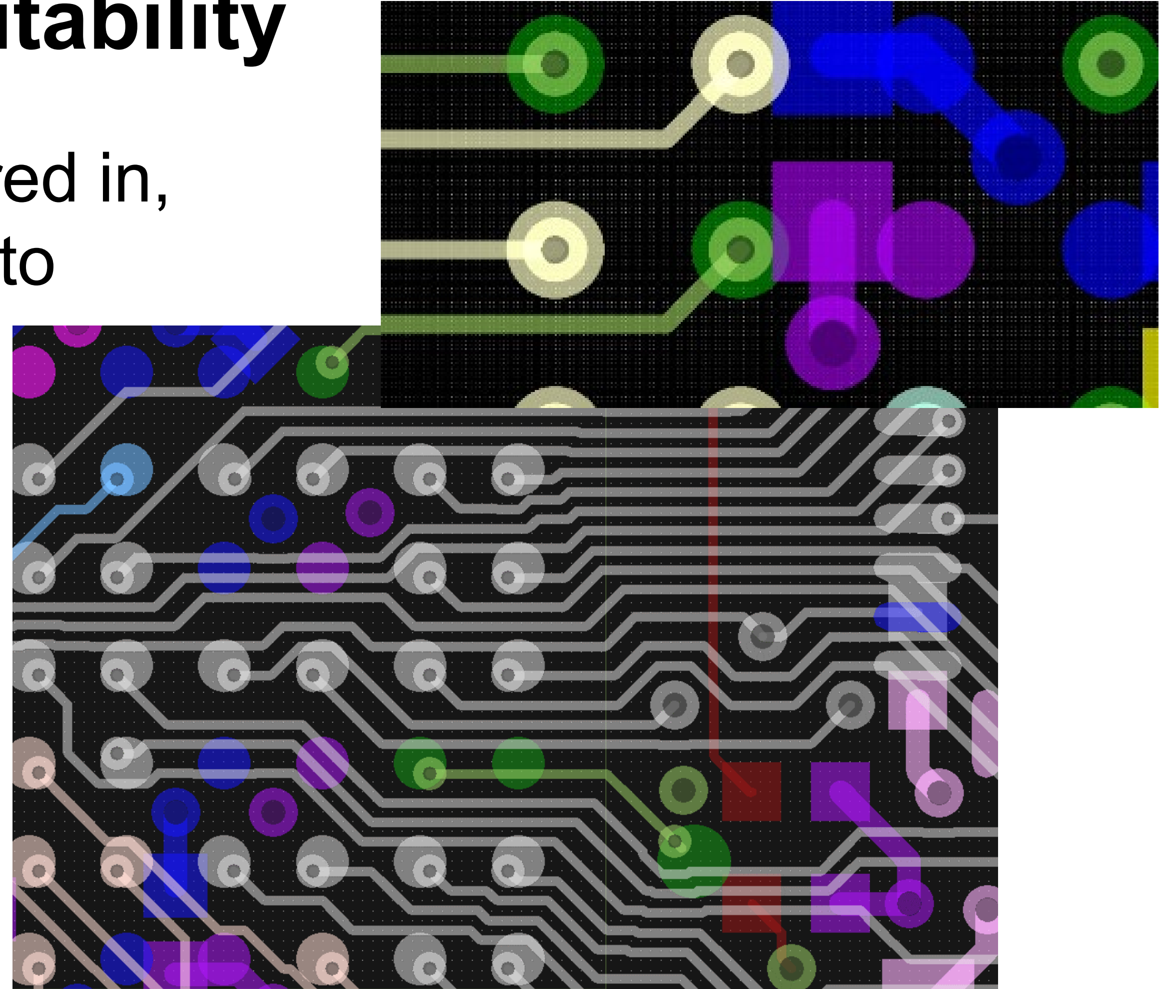
# A uVia placement grid can help any size parts' routability

- HDI vias can be centered in, offset from, or tangent to surface mount pads to set up routing channels
- Set up patterns that best use the area given



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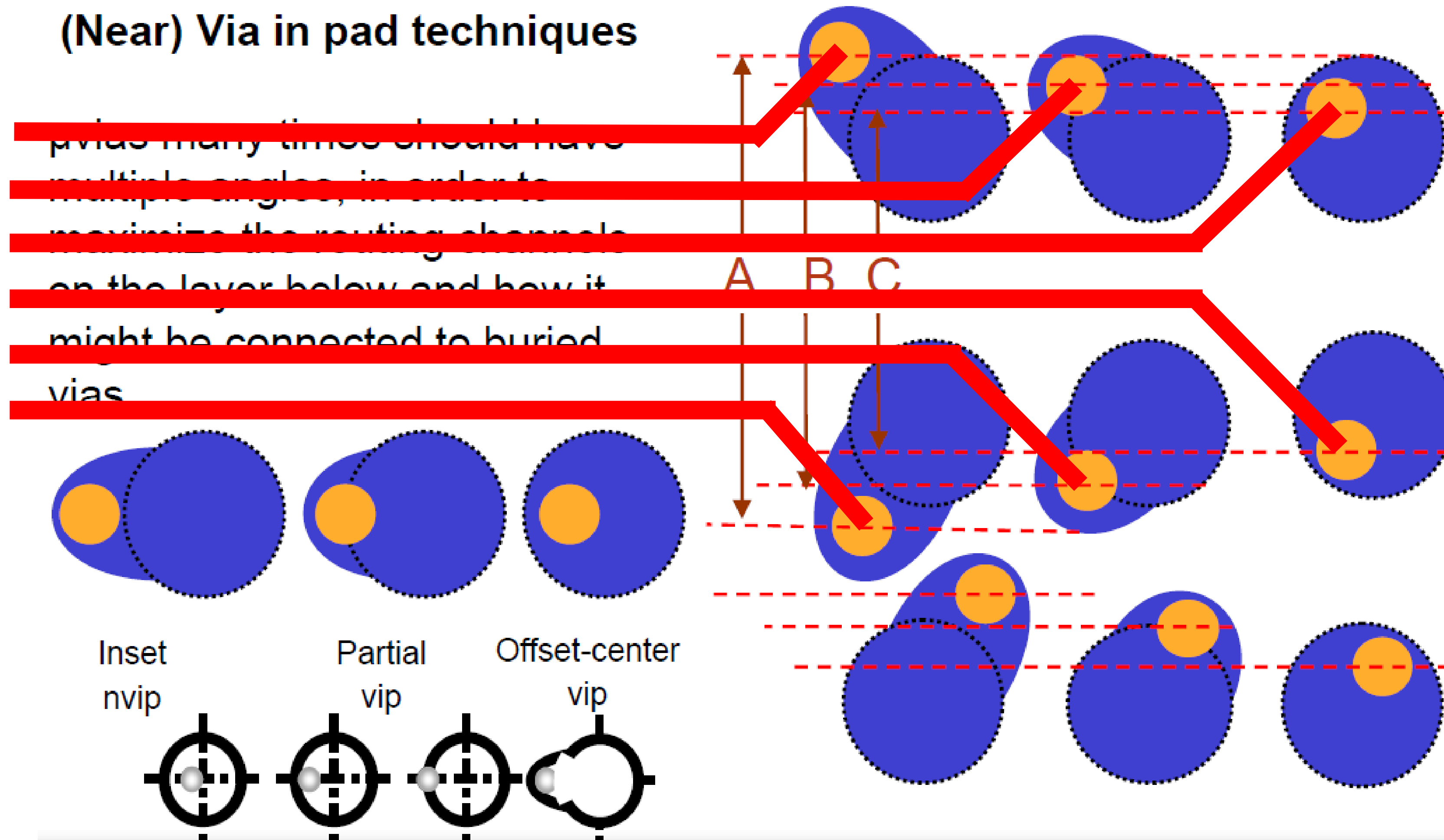
# uVIA Set up Tangent to pads in a Grid Pattern

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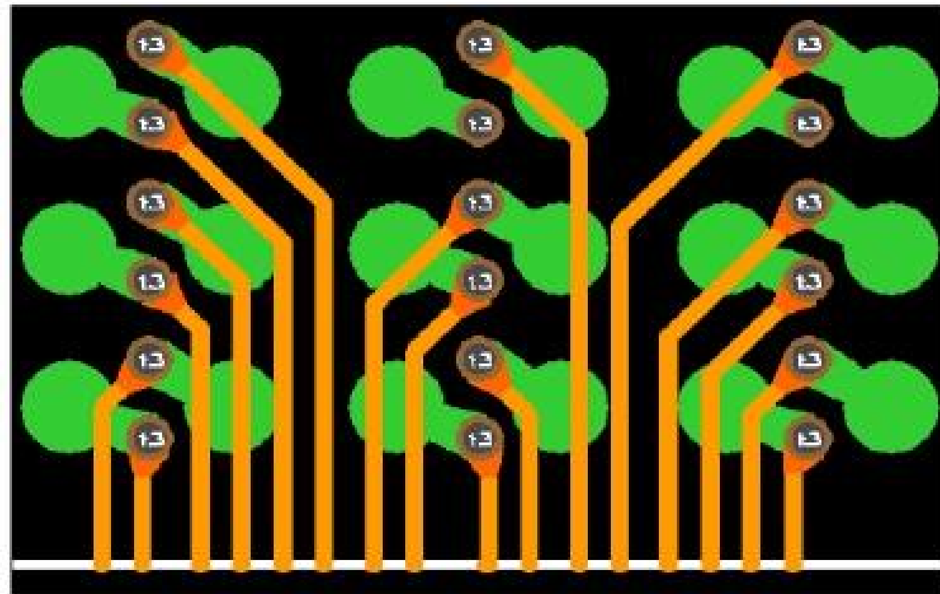
# Swing uVias improve large part routing as shown in this .8mm BGA

- Vias aligned for good channel routing - (note the fillets)



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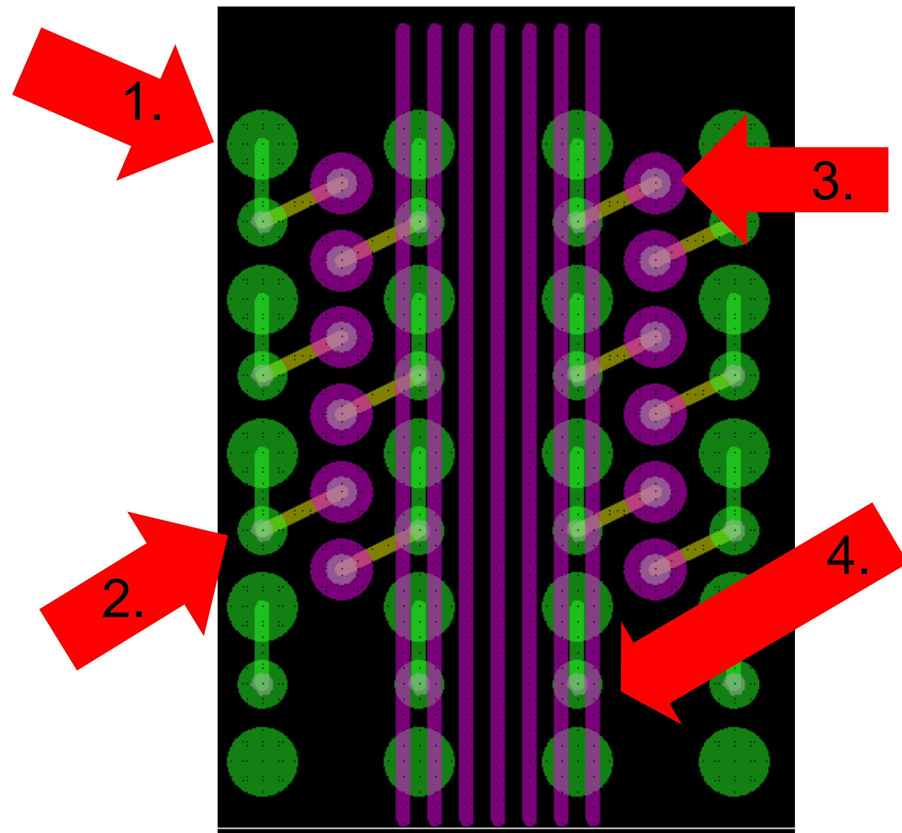
# Combination uVias and Buried Via Patterns

- uVias and buried vias may be used in any combinations to set up routing in Type II or higher boards




1) 1mm pitch BGA pad
2) uVia from pad to layer 2
3) Buried Vias (lined up) from layer 2 to layer N-1
4) Allows for many routes through the channel on several layers

*Patterns can be the same or different all around a part*

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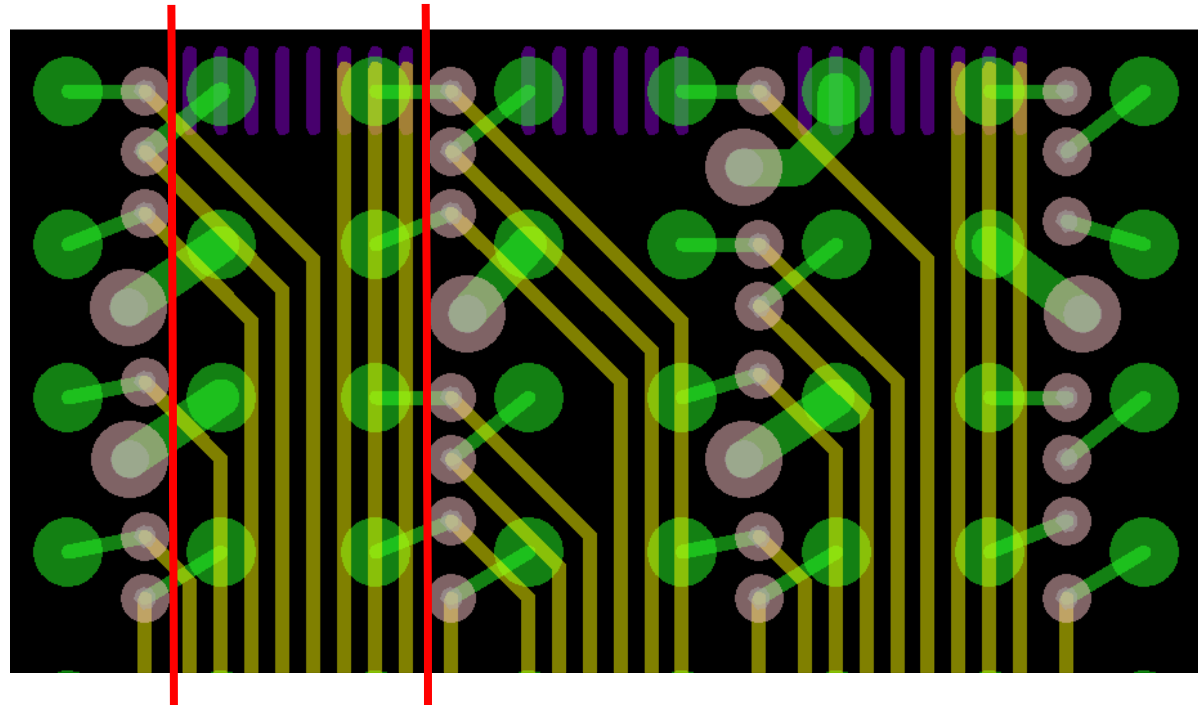
# Add some TH Vias to pattern for Power & Gnd

- Line up the edges of the different sized vias
- Routing on layer 2, plus pwr/gnd, AND good for routing on all other layers



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# Moving signals layer to layer - How will signals, powers and ground move from the fanout to other layers

- ***Make a plan!***
- “Once you leave TH designs, the goal is to find the via combination that maximizes routing channel density at the lowest cost”*
- Possible combination use of routing, uVias, TH vias and BB vias
- Part of any plan will include the percentage of pins on the parts that are actually being used

* “Integrating Advanced Microvia Structures in Complex Circuits”
Tom Buck, Senior Technologist, Viasystems Group

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# Moving Signals Through board

- A return plane is needed for each routing and power layer
- Need power/ground connections that join all like plane layers together
- Stacked and staggered uVias help get signals to move layer to layer, but require multiple laminations
- Other signals may use TH vias or buried TH vias to get signals to deep internal layers
- “Rough-in” routing may help decide a plan

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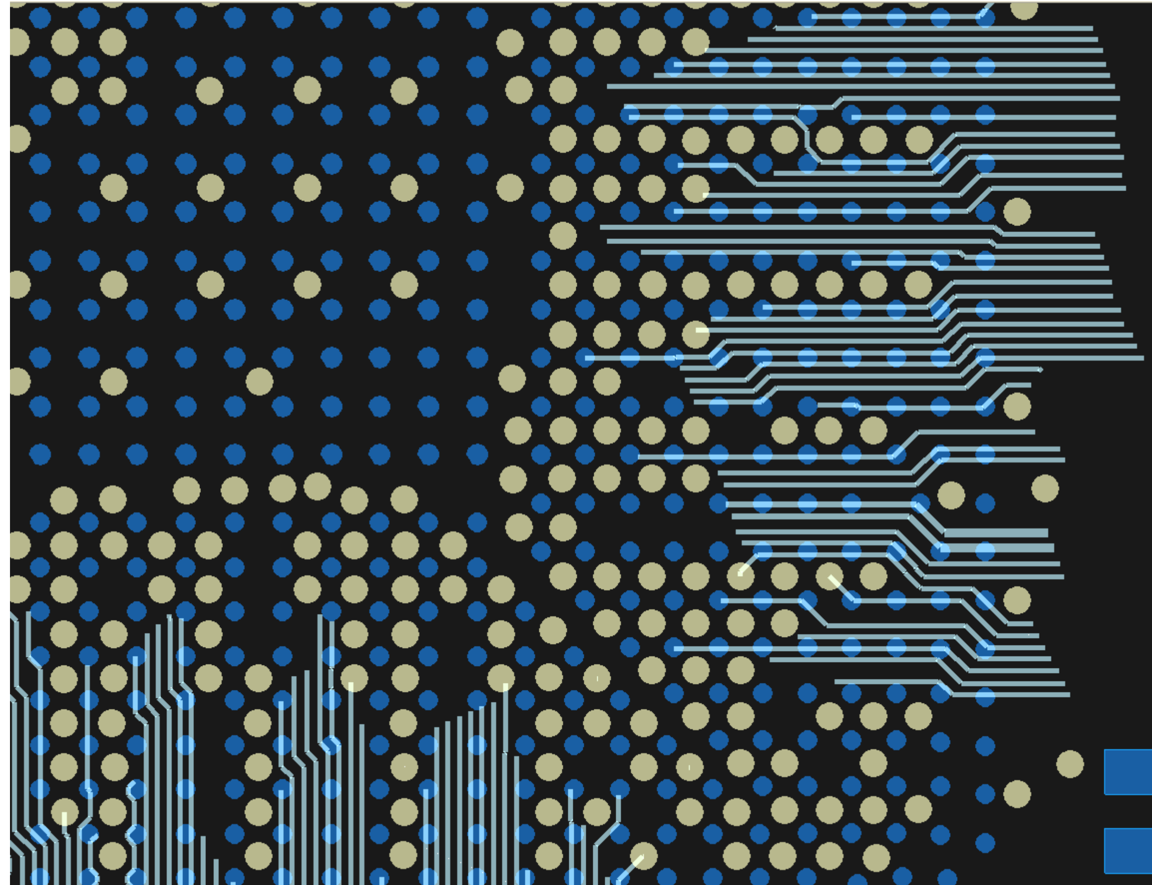
# ‘Rough-in’ route to see how many traces will fit in an area; connect later as needed



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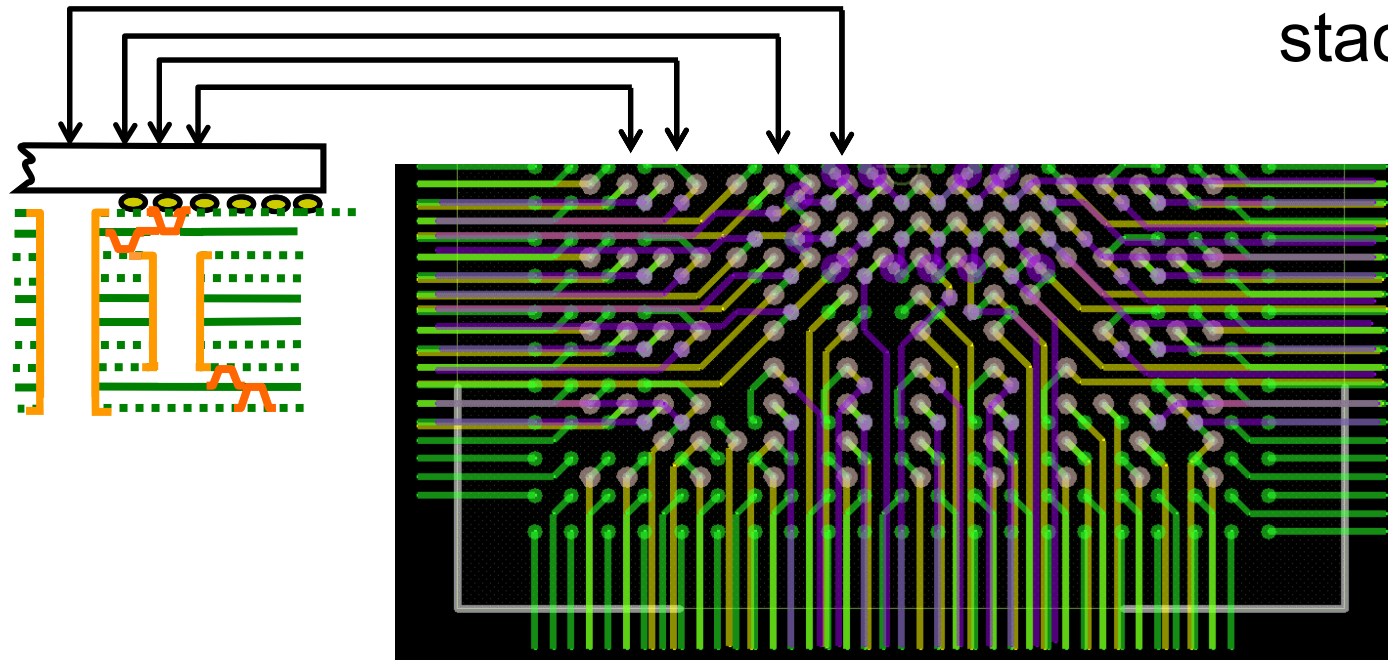
# Plan for design with ‘rough-in’ routing, for a BGA with several types of vias

- Type III stack



# Sketch a flow diagram plan for how signals/busses may flow layer to layer

| | BUS #1 | BUS #2 | BUS # 3 | Critical Signal group #1 | Critical Signal group #2 | Power and Ground |
|---|---|---|---|---|---|---|
| layer 1 - Signal w/ poured gnd | | | | | | |
| layer 2 - Gnd | | | | | | |
| layer 3 - Signal | | | | | | |
| layer 4 - Signal | | | | | | |
| layer 5 - Gnd | | | | | | |
| layer 6 - Pwr | | | | | | |
| layer 7 - Signal | | | | | | |
| layer 8 - Signal | | | | | | |
| layer 9 - Gnd | | | | | | |
| layer 10 - Signal w/ poured gnd | | | | | | |

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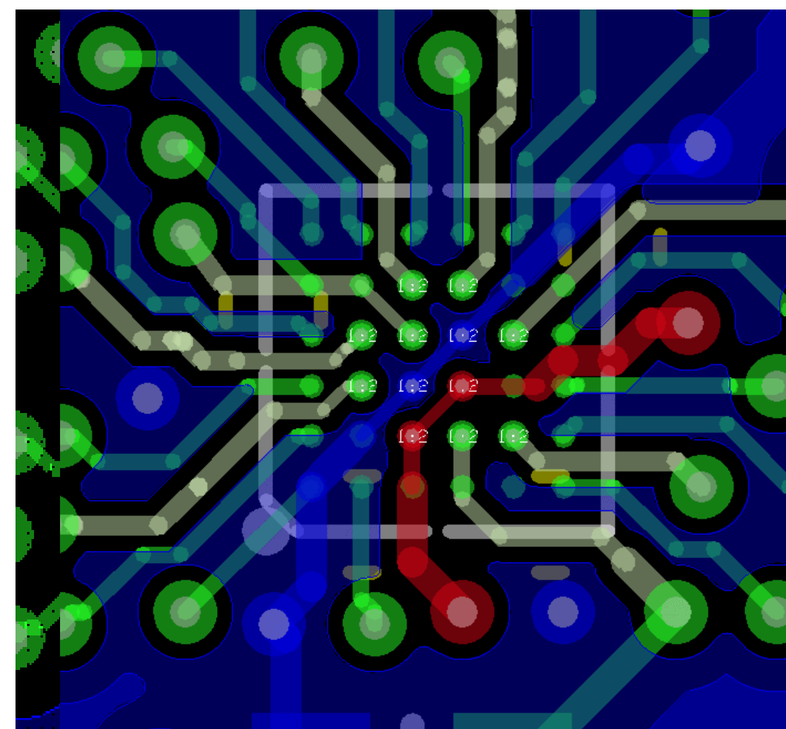
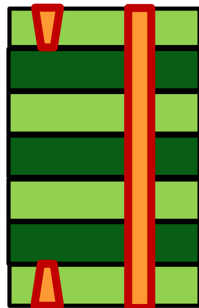
# Routing for SMALL parts – May use a combination of routing from pads and Via in Pad (Type I)

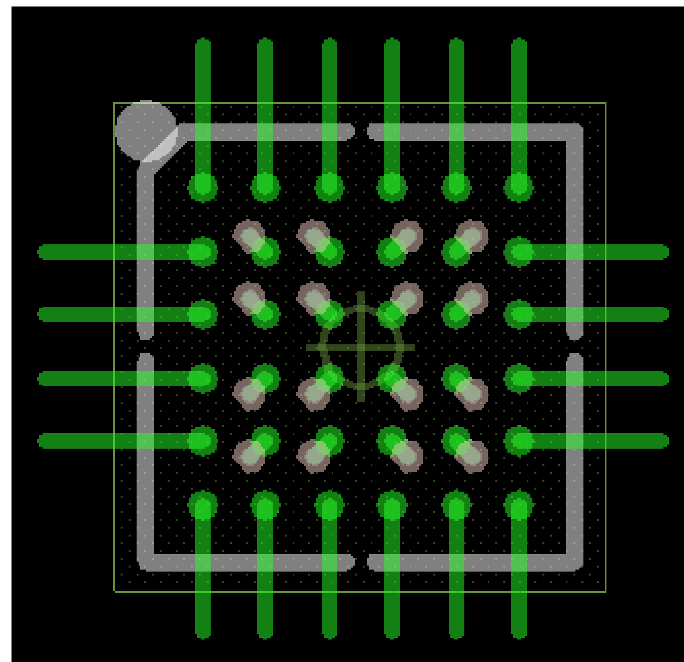
- Because routing is on layers 1&2, return may need to be routed or poured manually to get enough copper return for the signals on each layer

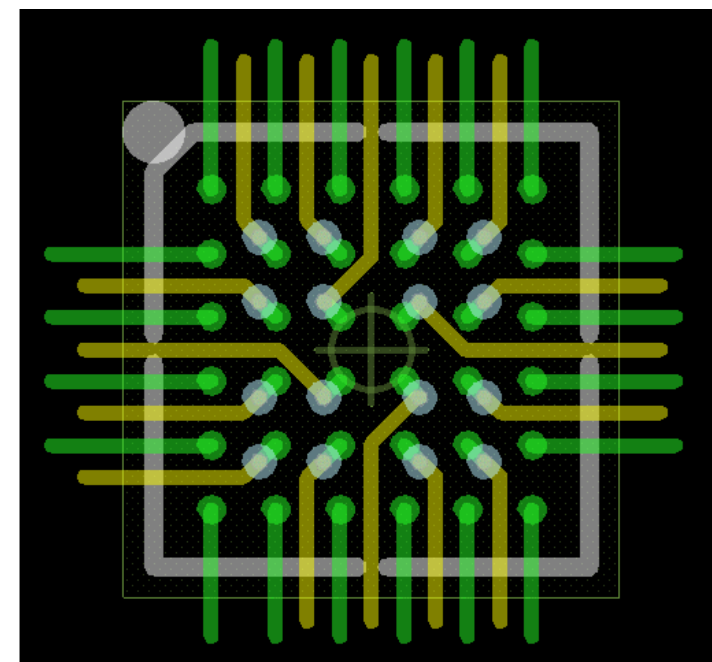


# SMALL parts – May use offset pattern of vias to get all signals out of part on 1-2 layers (Type I)

- Consideration may be needed for pwr/gnd connections in center (buried vias)
- Signals don't overlap each other, but plan the return on layer 1 or 3







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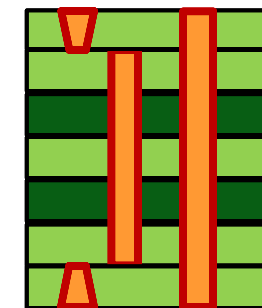
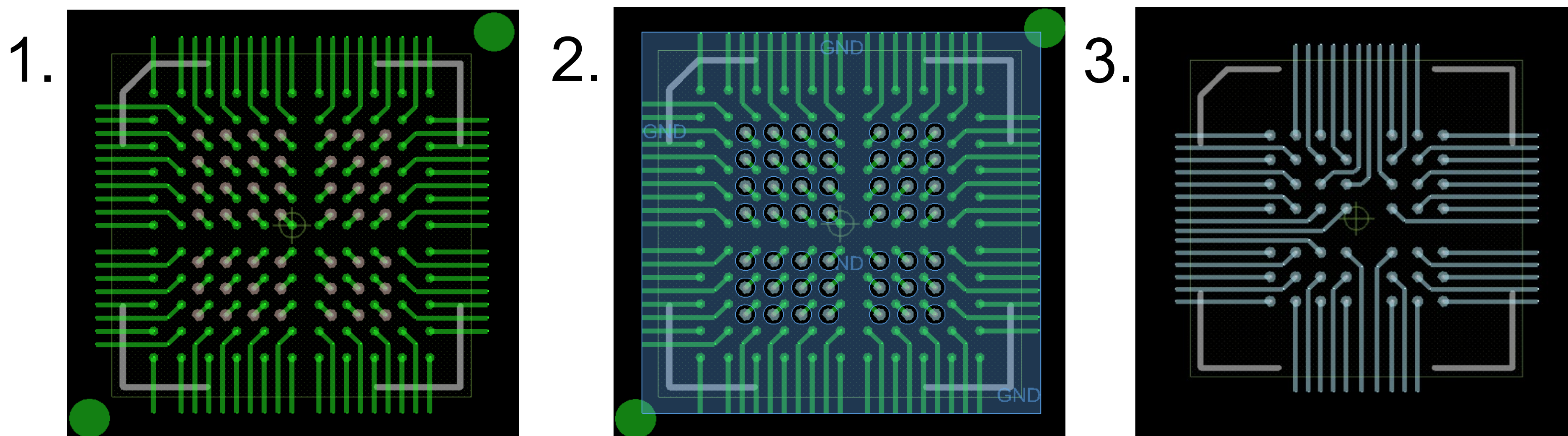
# SMALL parts – uVias can be tangent to pads (Type II)

1. Fanout center area to uVias to layer 2, Gnd pour on layer 2
2. Stagger signals to Buried vias
3. Route remaining signals on signal layer 3



Type II

121 pins .5mm .2mm pad, .1mm traces



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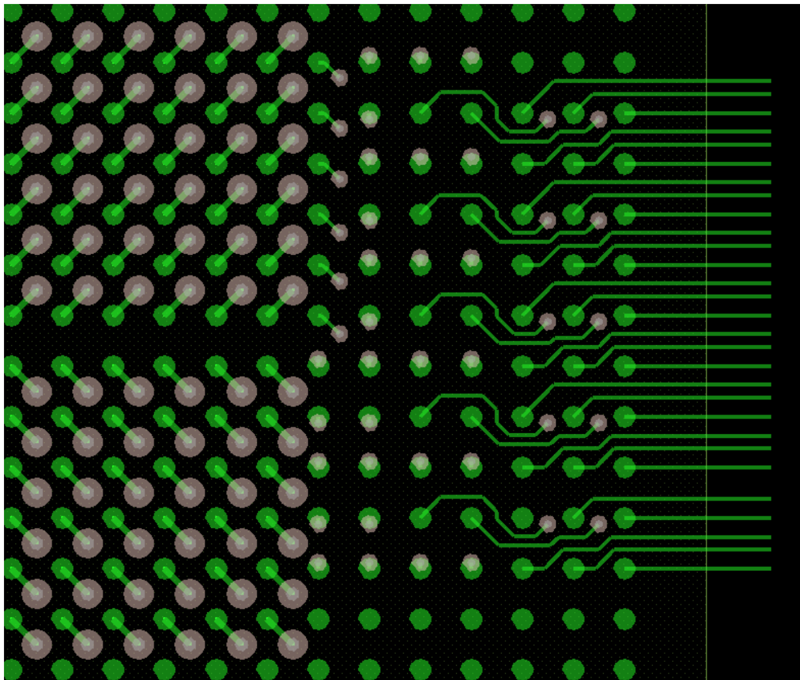
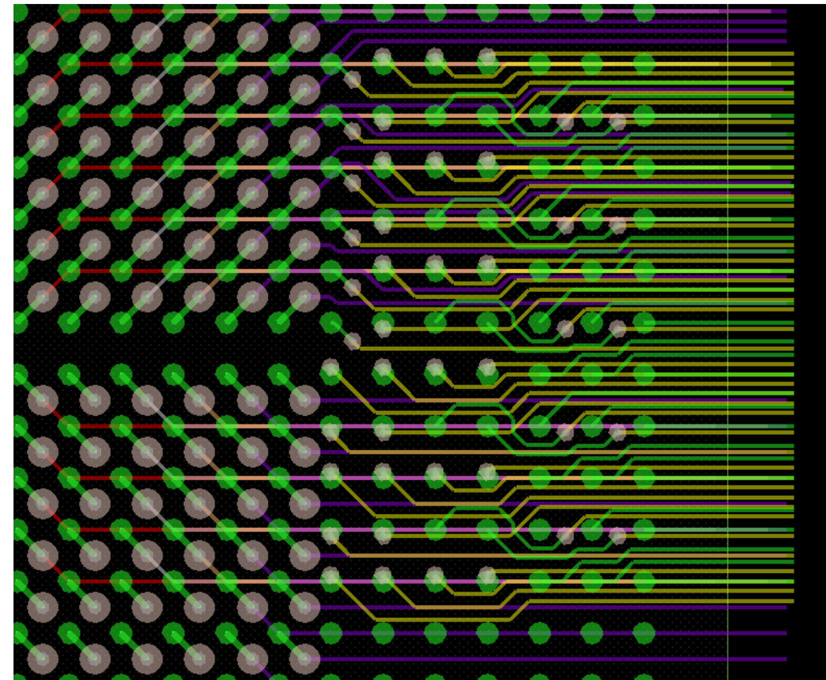
# LARGE parts - Pick a section and try different patterns

- Assume all pins are used
- Place power ground vias first
- Consider return plane for every signal
- HDI stackup on .8mm BGA

Top layer and vias only





7 routing layers

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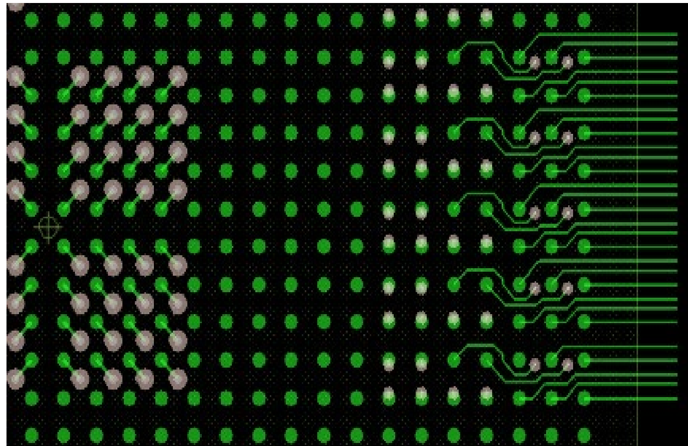
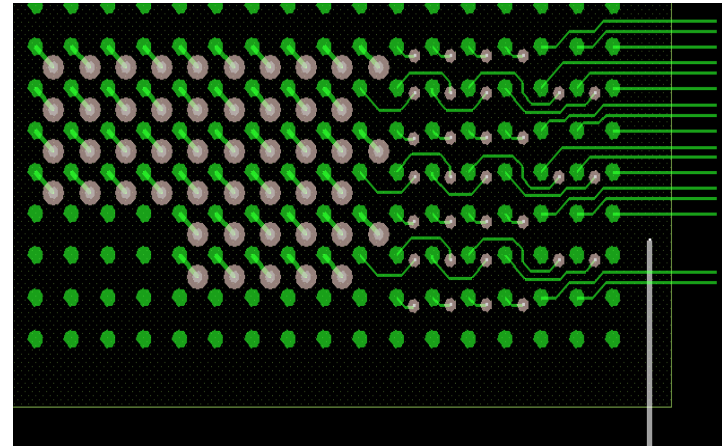
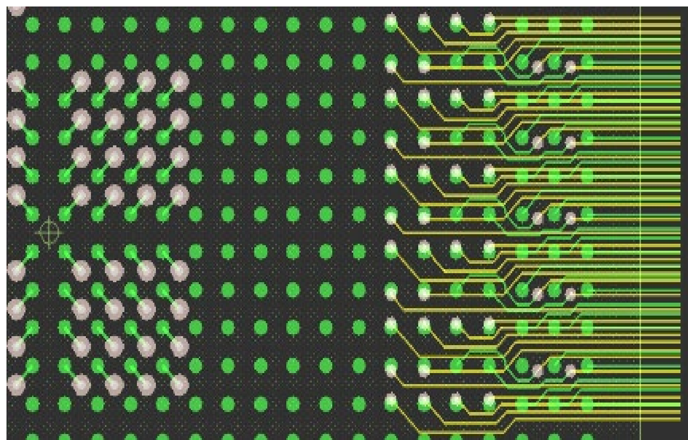
# LARGE Parts – Extended

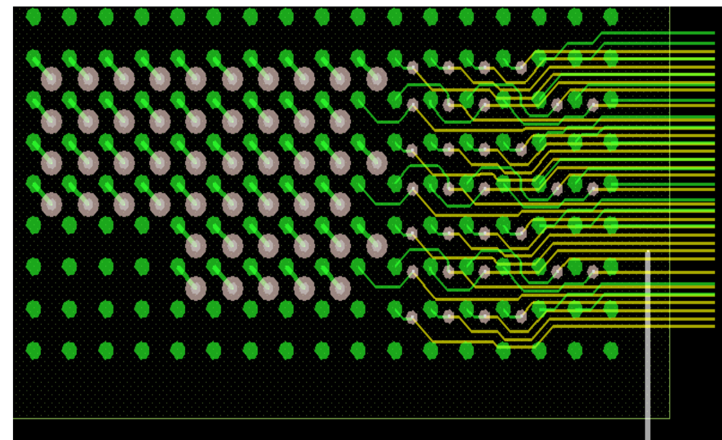
To get more routing, even more of the uVias might be 'worked' forward into layer 1 routing area





Original Example





Extended Example

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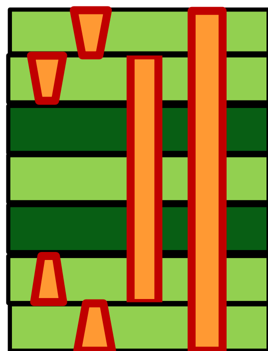
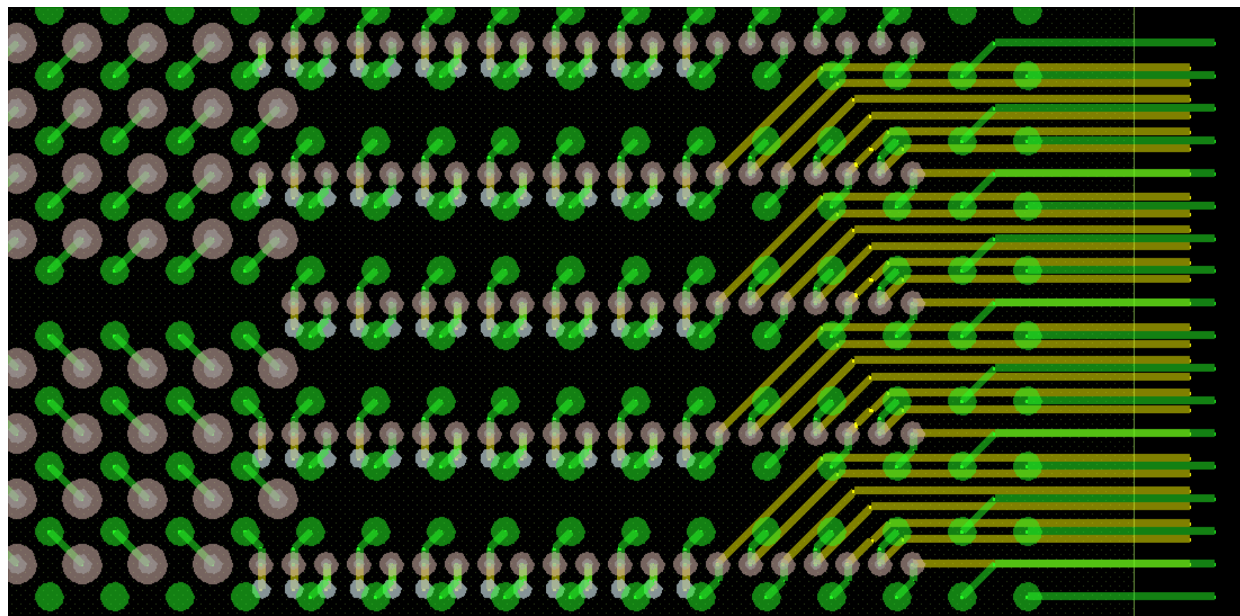
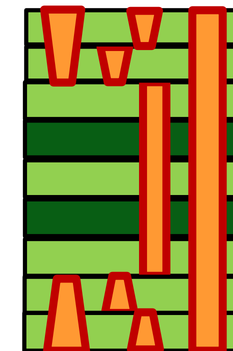
# LARGE parts - Pick a section and try different patterns - Type II or III HDI stackup, .8mm BGA

- Type II if uVias are drilled in both layers 1&2
- Type III if two layers of buildup
- Lots of routing on many layers



Type II





Type III

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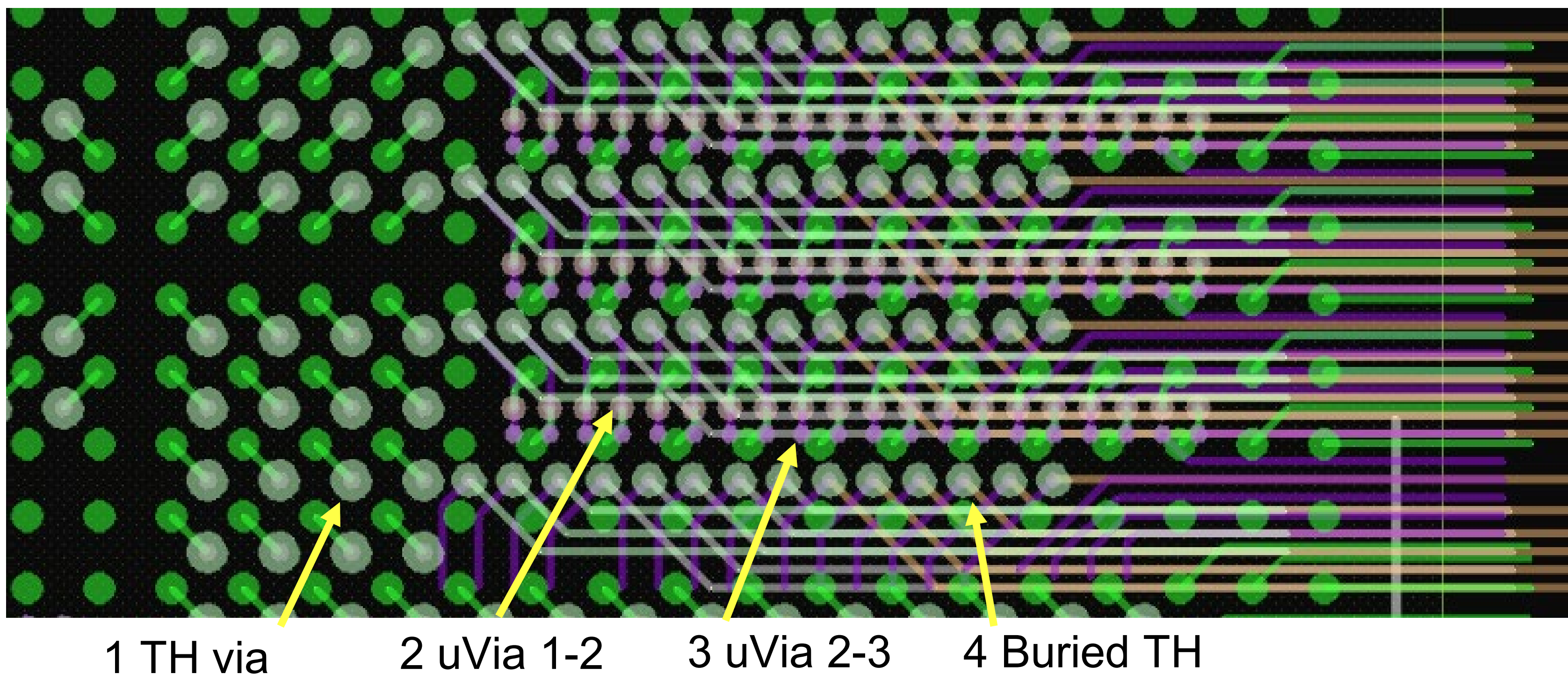
# LARGE parts - Pick a section and try different patterns - Type III HDI stackup

- uVias can greatly reduce the number of routing layers
- Part went from 15-16 TH routing layers to 5 - 6 routing layers depending on qty of overall pins used and number of pwr/gnd pins; Fewer planes too



1 TH via 2 uVia 1-2 3 uVia 2-3 4 Buried TH

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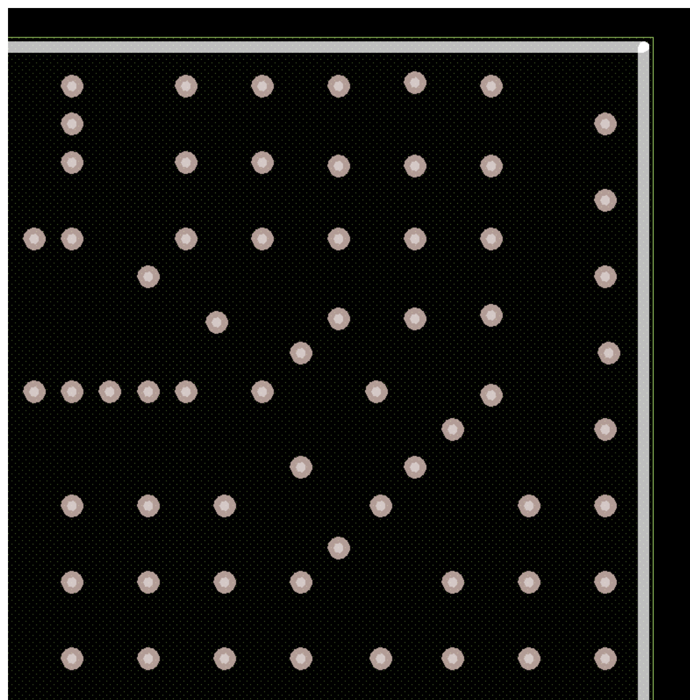
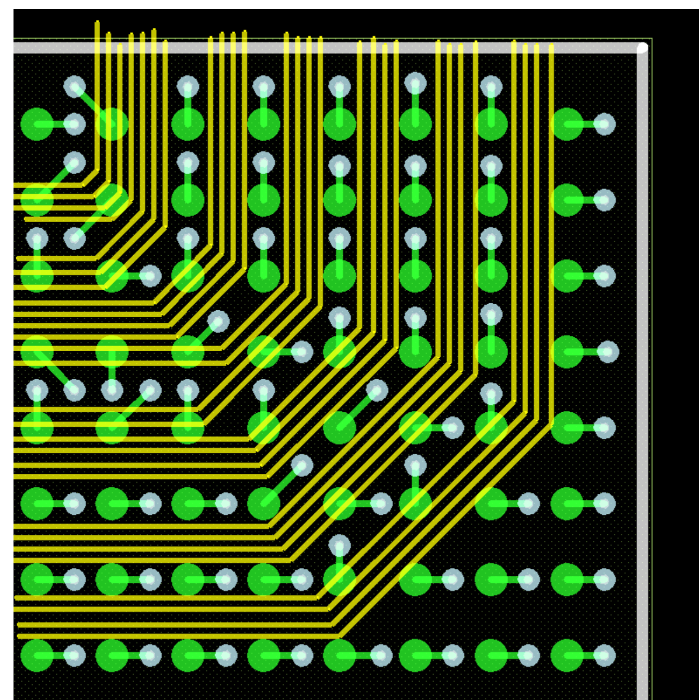
# LARGE parts - It may help to set up directional patterns

- uVia pattern set to open up areas of rows and columns to create large directional route channels





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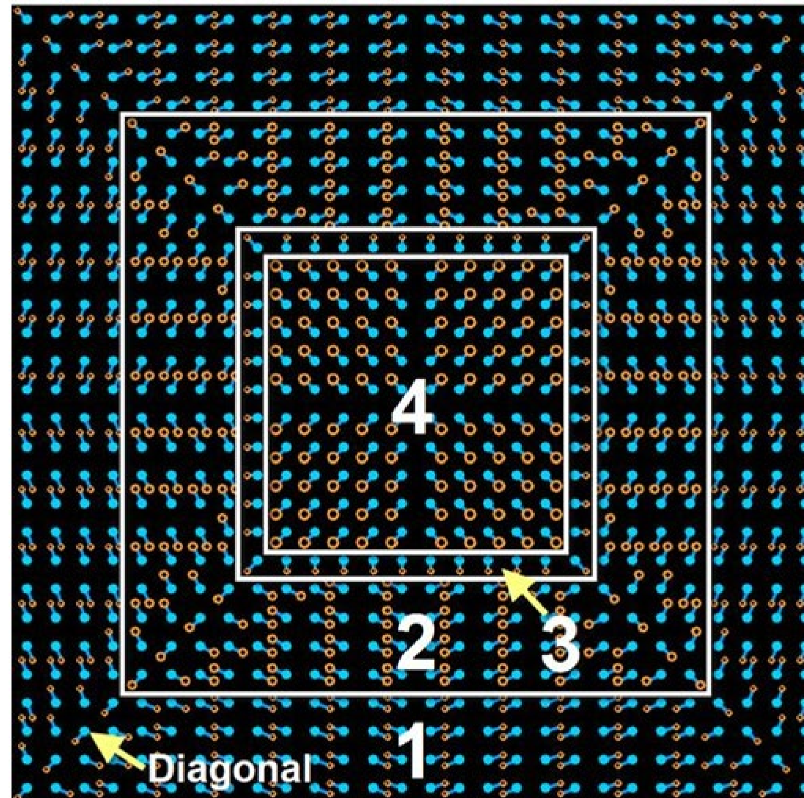
# LARGE parts, setting up Regions or Zones helps find effective routing in each area

- Use your imagination to think of channels!

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## HDI Manufacturing

- Control aspect ratio for all holes to @ 0.5:1 up to 0.7:1
- Higher aspect ratio may drive down yield and drive up cost
- Traces are typically 4/4 or 3/3 – extra spacing preferred
- Thinner copper to start is recommended for below 3/4
- Normal Cu thicknesses apply – ¼ oz, ½ oz, 3/8, etc (.5 oz plated up to @1.5 for outer, .5 inner)
- Check with fabricator for his norms before starting a board - capabilities, up-charges, turn times, etc.

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# If you want a low cost board:

- Use parts with as large a pitch as possible
- If HDI is used on an area of a board, it usually does not cost extra to use everywhere
- Minimize need to push the edge with anything in the design or manufacture
- Match CTE of large parts to board material to help with warping
- Use common board materials where board will be built
- Design for best fabrication yield whenever possible!

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# Thank you!

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